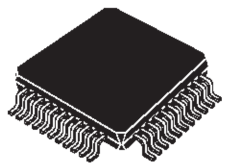
TDA7400

ADVANCED CAR SIGNAL PROCESSOR

- FULLY INTEGRATED SIGNAL PROCESSOR OPTIMIZED FOR CAR RADIO APPLICATIONS
- FULLY PROGRAMMABLE BY I^2C BUS
- INCLUDES AUDIOPROCESSOR, STEREO - DECODER WITH NOISE BLANKER AND MULTIPATH DETECTOR
- SOFTMUTE FUNCTION
- PROGRAMMABLE ROLL-OFF COMPENSATION
- NO EXTERNAL COMPONENTS



TQFP44

ORDERING NUMBER: TDA7400

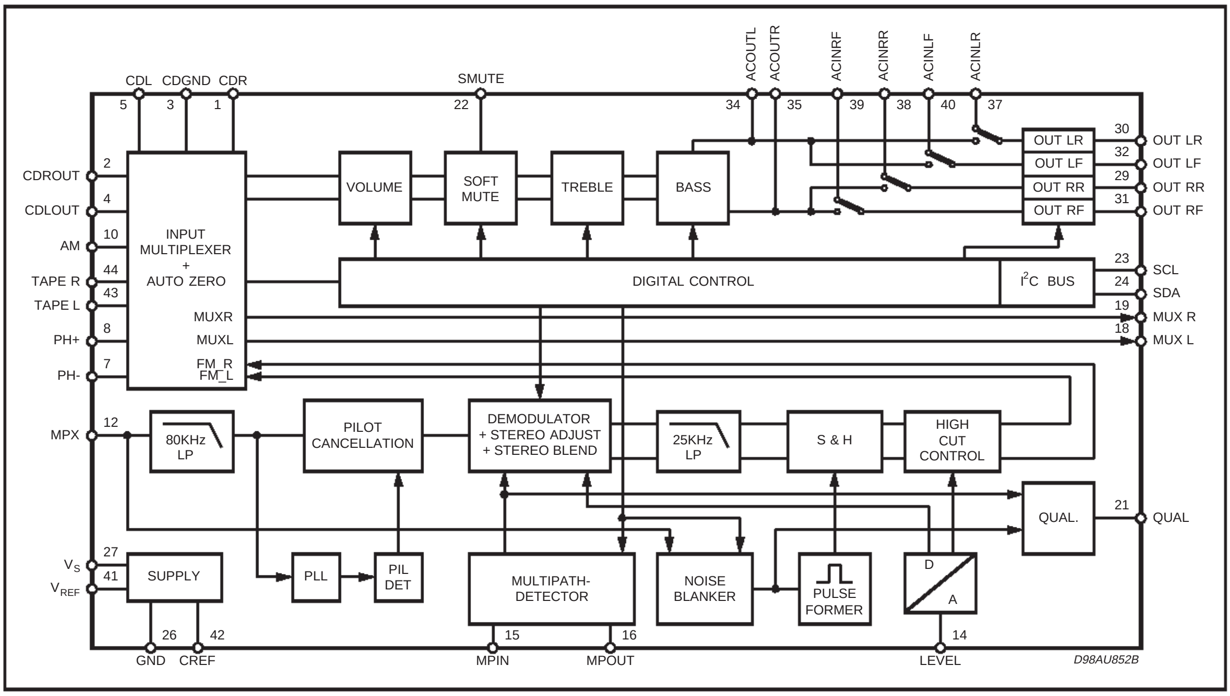
DESCRIPTION

The TDA7400 is the newcomer of the CSP family introduced by TDA7460/61. It uses the same innovative concepts and design technologies allowing fully software programmability through I^2C bus and overall cost optimisation for the system designer.

The device includes an audioprocessor with configurable inputs and absence of external components for filter settings, a last generation stereodecoder with multipath detector and a sophisticated stereoblend and noise cancellation circuitry.

Strength points of the CSP approach are flexibility and overall cost/room saving in the application, combined with high performances.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_S	Operating Supply Voltage	10.5	V
T_{amb}	Operating Ambient Temperature Range	-40 to 85	°C
T_{stg}	Operating Storage Temperature Range	-55 to 150	°C

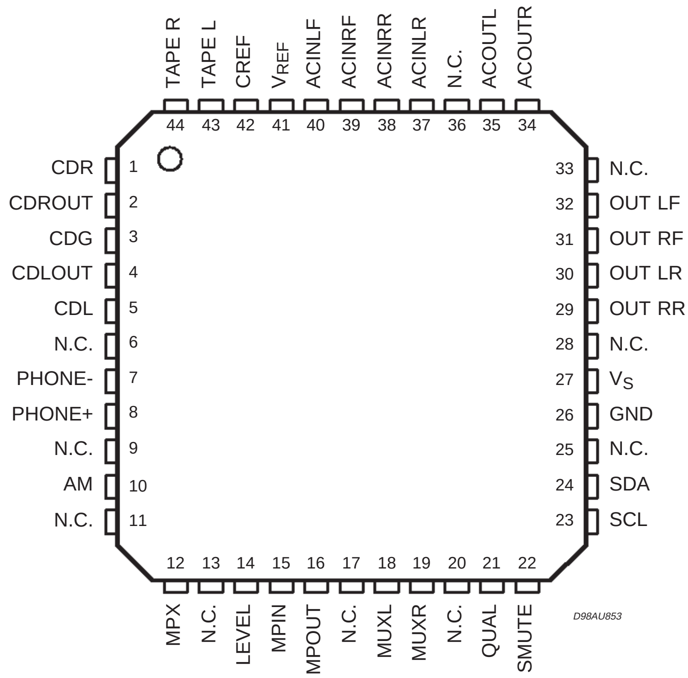
SUPPLY

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_S	Supply Voltage		7.5	9	10	V
I_S	Supply Current	V_S = 9V	25	30	35	mA
SVRR	Ripple Rejection @ 1KHz	Audioprocessor (all filters flat)	50	60		dB
		Stereodecoder + Audioprocessor	45	55		dB

ESD

All pins are protected against ESD according to the MIL883 standard.

PIN CONNECTION



THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\text{-}j\,pins}$	Thermal Resistance Junction-pins Max	85	°C/W

PIN DESCRIPTION

N.	Name	Function	Type
1	CDR	CD Right Channel Input	I
2	CDROUT	CD Output Right Channel	O
3	CDGND	CD Input Common Ground	I
4	CDLOUT	CD Output Left Channel	O
5	CDL	CD Input Left Channel	I
6	nc		-
7	PH -	Differential Phone Input -	I
8	PH +	Differential Phone Input +	I
9	nc		-
10	AM	AM Input	I
11	nc		-
12	MPX	FM Stereodecoder Input	I
13	nc		-
14	LEVEL	Level Input Stereodecoder	I
15	MPIN	Multipath Input	I
16	MPOUT	Multipath Output	O
17	nc		-
18	MUXL	Multiplexer Output Left Channel	O
19	MUXR	Multiplexer Output Right Channel	O
20	nc		-
21	QUAL	Stereodecoder Quality Output	O
22	SMUTE	Soft Mute Drive	I
23	SCL	I^2C Clock Line	I
24	SDA	I^2C Data Line	I/O
25	nc		-
26	GND	Supply Ground	S
27	VS	Supply Voltage	S
28	nc		-
29	OUTRR	Right Rear Speaker Output	O
30	OUTLR	Left Rear Speaker Output	O
31	OUTRF	Right Front Spaeaker Output	O
32	OUTLF	Left Front Speaker Output	O
33	nc		-
34	ACOUTR	Pre-speaker AC Output Right Channel	O
35	ACOUTL	Pre-speaker AC Output Left Channel	O
36	nc		-
37	ACINLR	Pre-speaker Input Left Rear Channel	I
38	ACINRR	Pre-speaker Input Right Rear Channel	I
39	ACINRF	Pre-speaker Input Right Front Channel	I
40	ACINLF	Pre-speaker Input Left Front Channel	I
41	VREF	Reference Voltage Output	O
42	CREF	Reference Capacitor Pin	S
43	TAPEL	Tape Input Left	I
44	TAPER	Tape Input Right	I

Pin type legenda: I = Input O = Output I/O = Input/Output S = Supply nc = not connected

AUDIO PROCESSOR PART

Input Multiplexer
- Quasi-differential CD and cassette stereo input
- AM mono input
- Phone differential input
- Multiplexer signal after In-Gain available at separate pins

Volume control
- 1dB attenuator
- Max. gain 15dB
- Max. attenuation 79dB

Bass Control
- 2nd order frequency response
- Center frequency programmable in 4(5) steps
- DC gain programmable
- ±15 x 1dB steps

Treble Control
- 2nd order frequency response
- Center frequency programmable in 4 steps
- ±15 x 1dB steps

Speaker Control
- 4 independent speaker controls in 1dB steps
- max gain 15dB
- max. attenuation 79dB

Mute Functions
- Direct mute

Digitally controlled softmute with 4 programmable mute time

ELECTRICAL CHARACTERISTICS (V_S = 9V; T_{amb} = 25°C; R_L = 10KΩ; all gains = 0dB; f = 1KHz; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
INPUT SELECTOR						
R_{in}	Input Resistance	all inputs except Phone	70	100	130	KΩ
V_{CL}	Clipping Level		2.2	2.6		V_{RMS}
S_{IN}	Input Separation		80	100		dB
$G_{IN\ MIN}$	Min. Input Gain		-1	0	1	dB
$G_{IN\ MAX}$	Max. Input Gain		13	15	17	dB
G_{STEP}	Step Resolution		0.5	1	1.5	dB
V_{DC}	DC Steps	Adjacent Gain Step	-5	0.5	5	mV
		G_{MIN} to G_{MAX}	-10	5	10	mV
DIFFERENTIAL CD STEREO INPUT						
R_{in}	Input Resistance	Differential	70	100	130	KΩ
		Common Mode	70	100	130	KΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 1_{VRMS} @ 1KHz	45	70		dB
		V_{CM} = 1_{VRMS} @ 10KHz	45	60		dB
e_N	Output Noise @ Speaker Outputs	20Hz to 20KHz flat; all stages 0dB		6	15	µV
DIFFERENTIAL PHONE INPUT						
R_{in}	Input Resistance	Differential	40	56		KΩ
CMRR	Common Mode Rejection Ratio	V_{CM} = 1_{VRMS} @ 1KHz	40	70		dB
		V_{CM} = 1_{VRMS} @ 10KHz	40	60		dB

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
VOLUME CONTROL						
G_{MAX}	Max Gain		13	15	17	dB
A_{MAX}	Max Attenuation		70	79		dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
E_A	Attenuation Set Error	G = -20 to 20dB	-1.25	0	1.25	dB
		G = -60 to 20dB	-4	0	3	dB
E_T	Tracking Error				2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0.1	3	mV
		From 0dB to G_{MIN}		0.5	5	mV
SOFT MUTE						
A_{MUTE}	Mute Attenuation		80	100		dB
T_D	Delay Time	T1		0.48	1	ms
		T2		0.96	2	ms
		T3	20	40.4	60	ms
		T4	200	324	600	ms
V_{THlow}	Low Threshold for SM Pin[1]				1	V
V_{THhigh}	High Threshold for SM Pin		2.5			V
R_{PD}	Internal Pull-up Resistor		70	100	130	KΩ
BASS CONTROL						
C_{RANGE}	Control Range		±13	±15	±17	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
f_C	Center Frequency	f_{C1}	54	60	66	Hz
		f_{C2}	63	70	77	Hz
		f_{C3}	72	80	88	Hz
		f_{C4}	90	100 (150)[2]	110	Hz
Q_{BASS}	Quality Factor	Q_1	0.9	1	1.1	
		Q_2	1.1	1.25	1.4	
		Q_3	1.3	1.5	1.7	
		Q_4	1.8	2	2.2	
DC_{GAIN}	Bass-Dc-Gain	DC = off	-1	0	1	dB
		DC = on	3.5	4.4	5.5	dB
TREBLE CONTROL						
C_{RANGE}	Control Range		±13	±15	±17	dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
f_C	Center Frequency	f_{C1}	8	10	12	KHz
		f_{C2}	10	12.5	15	KHz
		f_{C3}	12	15	18	KHz
		f_{C4}	14	17.5	21	KHz

1) The SM pin is active low (Mute = 0)
2) See note in Programming Part

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
SPEAKER ATTENUATORS						
R_{IN}	Input Impedance		35	50	65	KΩ
G_{MAX}	Max Gain		13	15	17	dB
A_{MAX}	Max Attenuation		-70	-79		dB
A_{STEP}	Step Resolution		0.5	1	1.5	dB
A_{MUTE}	Output Mute Attenuation		80	90		dB
E_E	Attenuation Set Error				±2	dB
V_{DC}	DC Steps	Adjacent Attenuation Steps		0.1	5	mV
AUDIO OUTPUTS						
V_{CLIP}	Clipping Level	d = 0.3%	2.2	2.6		V_{RMS}
R_L	Output Load Resistance		2			KΩ
C_L	Output Load Capacitance				10	nF
R_{OUT}	Output Impedance			30	120	Ω
V_{DC}	DC Voltage Level		4.3	4.5	4.7	V
GENERAL						
e_{NO}	Output Noise	BW = 20 Hz to 20 KHz output muted		3	15	μV
		BW = 20 Hz to 20 KHz all gain = 0dB		6.5	15	μV
S/N	Signal to Noise Ratio	all gain = 0dB flat; V_O = 2V_{RMS}	102	110		dB
		bass treble at 12dB; a-weighted; V_O = 2.6V_{RMS}	96	100		dB
d	Distortion	V_{IN} = 1V_{RMS}; all stages 0dB		0.002	0.1	%
		V_{IN} = 1V_{RMS}; Bass & Treble = 12dB		0.05	0.1	%
S_C	Channel separation Left/Right		80	100		dB
E_T	Total Tracking Error	A_V = 0 to -20dB	-1	0	1	dB
		A_V = -20 to -60dB	-2	0	2	dB
BUS INPUTS						
V_{IL}	Input Low Voltage	d = 0.3%			0.8	V
V_{IH}	Input High Voltage		2.5			V
I_{IN}	Input Current	V_{IN} = 0.4V	-5		5	μA
V_O	Output Voltage SDA Acknowledge	I_O = 1.6mA			0.4	V

Stereodecoder Part

ELECTRICAL CHARACTERISTICS (V_S = 9V; deemphasis time constant = 50µs, V_{MPX} = 500mV(75KHz deviation), fm= 1KHz, Gv = 6dB, T_{amb} = 27°C; unless otherwise specified).

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{in}	MPX Input Level	Gv = 3.5dB		0.5	1.25	V_{RMS}
R_{in}	Input Resistance		70	100	130	KΩ
G_{MIN}	Min. Input Gain		1.5	3.5	4.5	dB
G_{MAX}	Max. Input Gain		8.5	11	12.5	dB
G_{STEP}	Step Resolution		1.75	2.5	3.25	dB
SVRR	Supply Voltage Ripple Rejection	V_{ripple} = 100mV; f = 1KHz	35	60		dB
α	Max. channel Separation		30	50		dB
THD	Total Harmonic Distortion			0.02	0.3	%
$\frac{S+N}{N}$	Signal plus Noise to Noise Ratio	A-weighted, S = $2V_{rms}$	80	91		dB
MONO/STEREO-SWITCH						
V_{PTHST1}	Pilot Threshold Voltage	for Stereo, PTH = 1	10	15	25	mV
V_{PTHST0}	Pilot Threshold Voltage	for Stereo, PTH = 0	15	25	35	mV
V_{PTHMO1}	Pilot Threshold Voltage	for Mono, PTH = 1	7	12	17	mV
V_{PTHMO0}	Pilot Threshold Voltage	for Mono, PTH = 1	10	19	25	mV
PLL						
$\Delta f/f$	Capture Range		0.5			%
DEEMPHASIS and HIGHCUT						
τ_{HC50}	Deemphasis Time Constant	Bit 7, Subadr, 10 = 0, V_{LEVEL} >> V_{HCH}	25	50	75	µs
τ_{HC75}	Deemphasis Time Constant	Bit 7, Subadr, 10 = 1, V_{LEVEL} >> V_{HCH}	50	75	100	µs
τ_{HC50}	Highcut Time Constant	Bit 7, Subadr, 10 = 0, V_{LEVEL} >> V_{HCL}	100	150	200	µs
τ_{HC75}	Highcut Time Constant	Bit 7, Subadr, 10 = 1, V_{LEVEL} >> V_{HCL}	150	225	300	µs
STEREOBLEND-and HIGHCUT-CONTROL						
REF5V	Internal Reference Voltage		4.7	5	5.3	V
TC_{REF5V}	Temperature Coefficient			3300		ppm
L_{Gmin}	Min. LEVEL Gain		-1	0	1	dB
L_{Gmax}	Max. LEVEL Gain		8	10	12	dB
L_{Gstep}	LEVEL Gain Step Resolution		0.3	0.67	1	dB
$VSBL_{min}$	Min. Voltage for Mono		25	29	33	%REF5V
$VSBL_{max}$	Min. Voltage for Mono		54	58	62	%REF5V
$VSBL_{step}$	Step Resolution		2.2	4.2	6.2	%REF5V
$VHCH_{min}$	Min. Voltage for NO Highcut		38	42	46	%REF5V
$VHCH_{max}$	Min. Voltage for NO Highcut		62	66	70	%REF5V
$VHCH_{step}$	Step Resolution		5	8.4	12	%REF5V
$VHCL_{min}$	Min. Voltage for FULL Highcut		12	17	22	%VHCH
$VHCL_{max}$	Max. Voltage for FULL Highcut		28	33	38	%VHCH
$VHCL_{step}$	Step Resolution		2.2	4.2	6.2	%VHCH

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
Carrier and harmonic suppression at the output						
$\alpha 19$	Pilot Signal f = 19KHz		40	50		dB
$\alpha 38$	Subcarrier f = 38KHz				75	dB
$\alpha 57$	Subcarrier f = 57KHz				62	dB
$\alpha 76$	Subcarrier f = 76KHz				90	dB
Intermodulation (Note 1)						
$\alpha 2$	f_{mod} = 10KHz, f_{spur} = 1KHz				65	dB
$\alpha 3$	f_{mod} = 13KHz, f_{spur} = 1KHz				75	dB
Traffic Ratio (Note 2)						
$\alpha 57$	Signal f = 57KHz				70	dB
SCA - Subsidiary Communications Authoorization (Note 3)						
$\alpha 67$	Signal f = 67KHz				75	dB
ACI - Adjacent Channel Interference (Note 4)						
$\alpha 114$	Signal f = 114KHz				95	dB
$\alpha 190$	Signal f = 190KHz				84	dB

Notes to the characteristics:

1. Intermodulation Suppression:

$$\alpha 2 = \frac{V_{O(signal)(at1KHz)}}{V_{O(spurious)(at1KHz)}};\ f_s = (2 \times 10KHz) - 19KHz$$

$$\alpha 3 = \frac{V_{O(signal)(at1KHz)}}{V_{O(spurious)(at1KHz)}};\ f_s = (3 \times 13KHz) - 38KHz$$

measured with: 91% pilot signal; fm = 10kHz or 13kHz.

2. Traffic Radio (V.F.) Suppression: measured with: 91% stereo signal; 9% pilot signal; fm=1kHz; 5% subcarrier (f = 57kHz, fm = 23Hz AM, m = 60%)

$$\alpha 57\ (V.W>F.) = \frac{V_{O(signal)(at1KHz)}}{V_{O(spurious)(at1KHz \pm 23KHz)}}$$

3. SCA (Subsidiary Communications Authorization) measured with: 81% mono signal; 9% pilot signal; fm = 1kHz; 10%SCA - subcarrier (fs = 67kHz, unmodulated).

$$\alpha 67 = \frac{V_{O(signal)(at1KHz)}}{V_{O(spurious)(at9KHz)}};\ F_S = (2 \times 38KHz) - 67KHz$$

4. ACI (Adjacent Channel Interference):

$$\alpha 114 = \frac{V_{O(signal)(at1KHz)}}{V_{O(spurious)(at4KHz)}};\ F_S = 110KHz - (3 \times 38KHz)$$

$$\alpha 190 = \frac{V_{O(signal)(at1KHz)}}{V_{O(spurious)(at4KHz)}};\ F_S = 186KHz - (5 \times 38KHz)$$

measured with: 90% mono signal; 9% pilot signal; fm =1kHz; 1% spurious signal (fs = 110kHz or 186kHz, unmodulated).

NOISE BLANKER PART

- internal 2nd order 140kHz high pass filter
- programmable trigger threshold
- trigger threshold dependent on high frequency noise with programmable gain
- additional circuits for deviation and field-strength dependent trigger adjustment
- very low offset current during hold time due to opamps wMOS inputs
- four selectable pulse suppression times
- programmable noise rectifier charge/discharge current

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{TR}	Trigger Threshold [0) 1)]	meas. with V_{PEAK} = 0.9V	NBT = 111	(c)	30	(c)	mV_{OP}
			NBT = 110	(c)	35	(c)	mV_{OP}
			NBT = 101	(c)	40	(c)	mV_{OP}
			NBT = 100	(c)	45	(c)	mV_{OP}
			NBT = 011	(c)	50	(c)	mV_{OP}
			NBT = 010	(c)	55	(c)	mV_{OP}
			NBT = 001	(c)	60	(c)	mV_{OP}
			NBT = 000	(c)	65	(c)	mV_{OP}
$V_{TRNOISE}$	Noise Controlled Trigger Threshold [2)]	meas. with V_{PEAK} = 1.5V	NCT = 00	(c)	260	(c)	mV_{OP}
			NCT = 01	(c)	220	(c)	mV_{OP}
			NCT = 10	(c)	180	(c)	mV_{OP}
			NCT = 11	(c)	140	(c)	mV_{OP}
V_{RECT}	Rectifier Voltage	V_{MPX} = 0mV	NRD [6)] = 00	0.5	0.9	1.3	V
		V_{MPX} = 50mV; f = 150KHz		1.5	1.7	2.1	V
		V_{MPX} = 200mV; f = 150KHz		2.2	2.5	2.9	V
$V_{RECT\ DEV}$	deviation dependent rectifier Voltage [3)]	means. with V_{MPX} = 800mV (75KHz dev.)	OVD = 11	0.5	0.9(off)	1.3	V_{OP}
			OVD = 10	0.9	1.2	1.5	V_{OP}
			OVD = 01	1.7	2.0	2.3	V_{OP}
			OVD = 00	2.5	2.8	3.1	V_{OP}
$V_{RECT\ FS}$	Fieldstrength Controlled Rectifier Voltage [4)]	means. with V_{MPX} = 0mV $V_{LEVEL} << V_{SBL}$ (fully mono)	FSC = 11	0.5	0.9(off)	1.3	V
			FSC = 10	0.9	1.4	1.5	V
			FSC = 01	1.7	1.9	2.3	V
			FSC = 00	2.1	2.4	3.1	V
T_S	Suppression Pulse Duration [5)]	Signal HOLDN in Testmode	BLT = 00	TBD	38	TBD	µs
			BLT = 10	TBD	32	TBD	µs
			BLT = 01	TBD	25.5	TBD	µs
			BLT = 00	TBD	22	TBD	µs
$V_{RECTADJ}$	Noise Rectifier discharge adjustment [6)]	Signal PEAK in Testmode	NRD = 00 [6)]	(c)	0.3	(c)	V/ms
			NRD = 01 [6)]	(c)	0.8	(c)	V/ms
			NRD = 10 [6)]	(c)	1.3	(c)	V/ms
			NRD = 11 [6)]	(c)	2.0	(c)	V/ms
SR_{PEAK}	Noise Rectifier Charge	Signal PEAK in Testmode	PCH = 0 [7)]	(c)	10	(c)	mV/µs
			PCH = 1 [7)]	(c)	20	(c)	mV/µs

(c) = by design/characterization functionally guaranteed through dedicated test mode structure

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
V_{ADJMP}	Noise Rectifier adjustment through Multipath 8)	Signal PEAK in Testmode	MPNB = 00 8)	(c)	0.3	(c)	V/ms
			MPNB = 01 8)	(c)	0.5	(c)	V/ms
			MPNB = 10 8)	(c)	0.7	(c)	V/ms
			MPNB = 11 8)	(c)	0.9	(c)	V/ms

0) All Thresholds are measured using a pulse with T_R =2µs, T_{HIGH} = 2µs and T_F = 10µs. The repetition rate must not increase the PEAK voltage.

1) NBT represents the Noiseblanker Byte bits D_2, D_0 for the noise blanker trigger threshold

2) NAT represents the Noiseblanker Byte bit pair D_4, D_3 for the noise controlled triggeradjustment

3) OVD represents the Noiseblanker Byte bit pair D_7, D_6 for the over deviation detector

4) FSC represents the Fieldstrength Byte bit pair D_1, D_0 for the fieldstrength control

5) BLT represents the Speaker RR Byte bit pair D_7, D_6 for the blanktime adjustment

6) NRD represents the Configuration-Byte bit pair D_1, D_0 for the noise rectifier discharge-adjustment

7) PCH represents the Stereodecoder-Byte bit D_5 for the noise rectifier charge-current adjustment

8) MPNB represents the HighCut-Byte bit D_7 and the Fieldstrength-Byte D_7 for the noise rectifier multipath adjustment

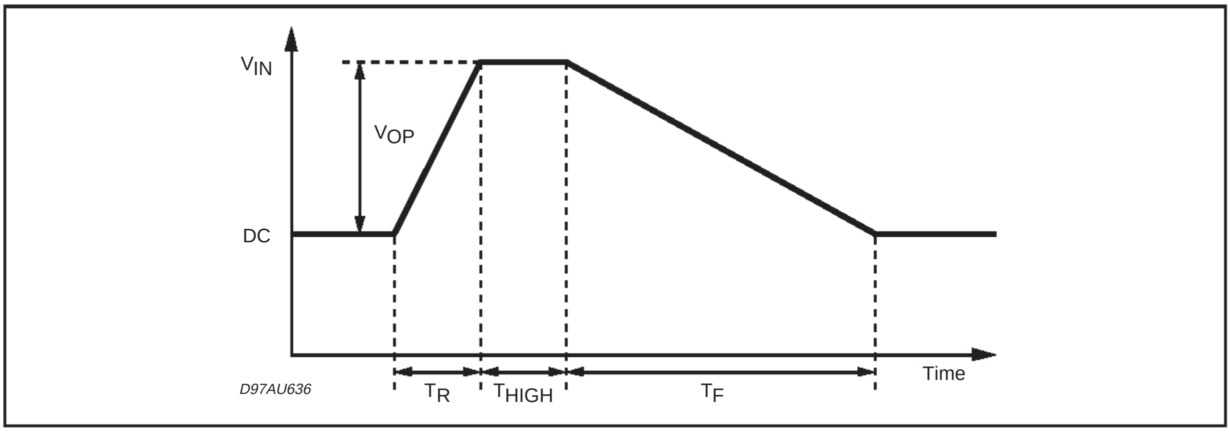


Figure 1. Trigger Threshold vs.VPEAK

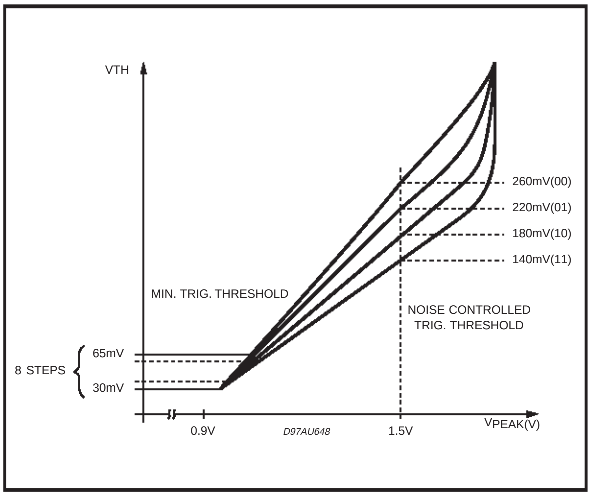


Figure 2. Deviation Controlled Trigger Adjustment

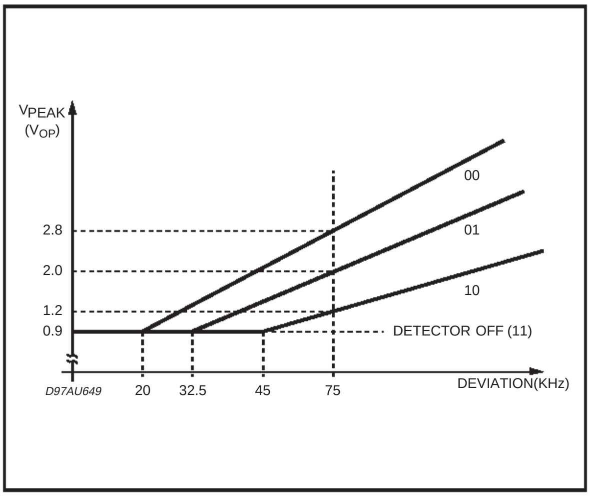
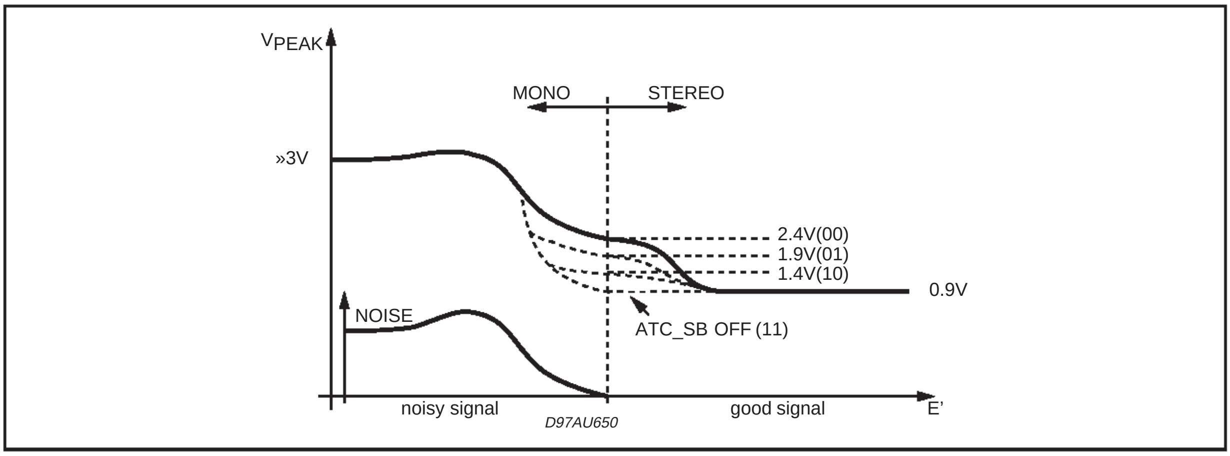


Figure 3. Fieldstrength Controlled Trigger Adjustment



Multipath Detector

- Internal 19kHz band pass filter
- Programmable band pass and rectifier gain
- two pin solution fully independent usable for external programming
- selectable internal influence on Stereoblend

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
f_{CMP}	Center Frequency of Multipath-Bandpass	stereodecoder locked on Pilottono		19		KHz
G_{BPMP}	Bandpass Gain	bits D_2, D_1 configuration byte = 00		6		dB
		bits D_2, D_1 configuration byte = 10		12		dB
		bits D_2, D_1 configuration byte = 01		16		dB
		bits D_2, D_1 configuration byte = 11		18		dB
G_{RECTMP}	Rectifier Gain	bits D_7, D_6 configuration byte = 00		7.6		dB
		bits D_7, D_6 configuration byte = 01		4.6		dB
		bits D_7, D_6 configuration byte = 10		0		dB
		bits D_7, D_6 configuration byte = 11		off		dB
I_{CHMP}	Rectifier Charge Current	bit D_5 configuration byte = 0		0.5		µA
		bit D_5 configuration byte = 1		1.0		µA
I_{DISMP}	Rectifier Discharge Current		0.5	1	1.5	mA

Quality Detector

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
A	Multipath Influence Factor	bit D_7 High-Cut byte + bit D_7 Fieldstrength byte +	00 01 10 11		0.7 0.85 1.00 1.15		

DESCRIPTION OF THE AUDIOPROCESSOR PART

Input Multiplexer

- CD quasi differential
- Cassette stereo
- Phone differential
- AM mono
- Stereodecoder input.

Input stages

Most of the input stages have remained the same as in preceeding ST audioprocessors with exception of the CD inputs (see figure 4).
In the meantime there are some CD players in the market having a significant high source impedance which affects strongly the common-mode rejection of the normal differential input stage. The additional buffer of the CD input avoids this drawback and offers the full common-mode rejection even with those CD players.

The output of the Cd stage is permanently available of the Cd out-pins

AutoZero

In order to reduce the number of pins there is no AC coupling between the In-Gain and the following stage, so that any offset generated by or before the In-Gain stage would be transferred or even amplified to the output.

To avoid that effect a special offset cancellation stage called AutoZero is implemented.

This stage is located before the volume-block to eliminate all offsets generated by the Stereodecoder, the Input Stage and the In-Gain (Please notice that externally generated offsets, e.g. generated through the leakage current of the coupling capacitors, are not cancelled).

The auto-zeroing is started every time the DATABYTE 0 is selected and takes a time of max. 0.3ms. To avoid audible clicks the audioprocessor is muted before the volume stage during this time.

AutoZero Remain

In some cases, for example if the µP is executing a refresh cycle of the I^2C bus programming, it is not useful to start a new AutoZero action because no new source is selected and an undesired mute would appear at the outputs. For such applications the TDA7400 could be switched in the "Auto Zero Remain mode" (Bit 6 of the subaddress byte). If this bit is set to high, the DATABYTE 0 could be loaded without invoking the AutoZero and the old adjustment value remains.

Multiplexer Output

The output signal of the Input Multiplexer is available at separate pins (please see the Blockdiagram). This signal represents the input signal amplifier by the In Gain stage and is also going into the Mixer stage.

Softmute

The digitally controlled softmute stage allows muting/demuting the signal with a I^2C bus programmable slope. The mute process can either be activated by the softmute pin or by the I^2C bus. The slope is realized in a special S shaped curve to mute slow in the critical regions (see figure 5).

Figure 4. Input stages

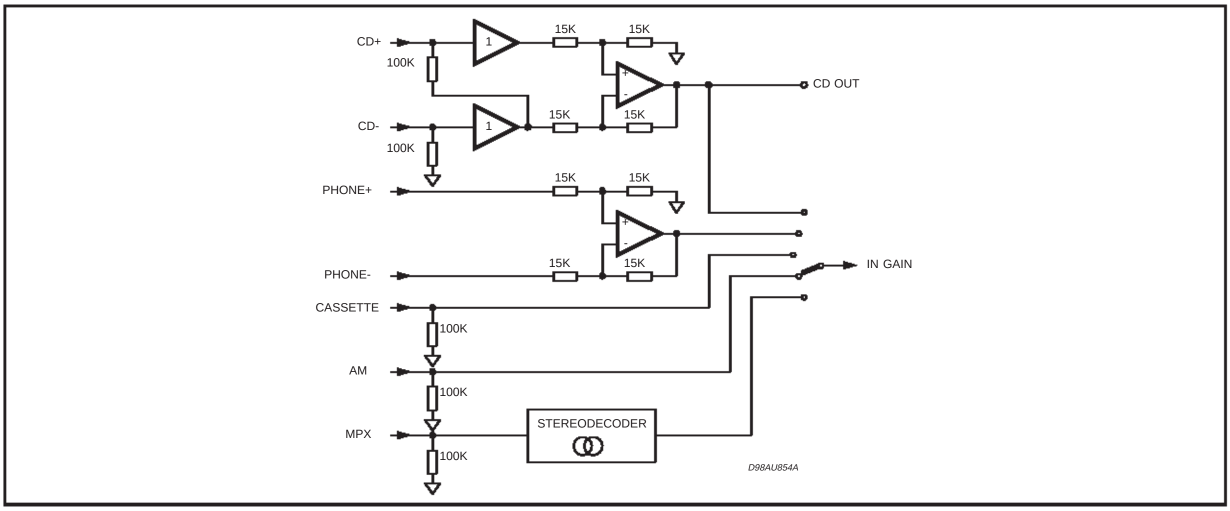
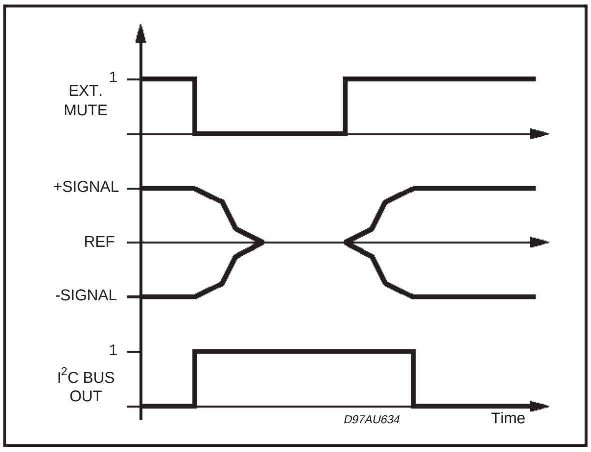


Figure 5. Softmute Timing



Note: Please notice that a started Mute action is always terminated and could not be interrupted by a change of the mute signal.

For timing purposes the Bit 3 of the I^2C bus output register is set to 1 from the start of muting until the end of demuting.

Bass

There are four parameters programmable in the bass stage: (see figs 6, 7, 8, 9):

Attenuation

Figure 6 shows the attenuation as a function of frequency at a center frequency at a center frequency of 80Hz.

Central Frequency

Figure 7 shows the four possible center frequencies 60,70,80 and 100Hz.

Quality Factors

Figure 8 shows the four possible quality factors 1, 1.25, 1.5 and 2.

DC Mode

In this mode the DC gain is increased by 5.1dB. In addition the programmed center frequency and quality factor is decreased by 25% which can be used to reach alternative center frequencies or quality factors.

TREBLE

There are two parameters programmable in the treble stage (see figs 10, 11):

Attenuation

Figure 10 shows the attenuation as a function of frequency at a center frequency of 17.5KHz.

Center Frequency

Figure 11 shows the four possible Center Frequency (10, 12.5, 15 and 17.5kHz).

AC Coupling

In some applications additional signal manipulations are desired, for example surround-sound or more-band-equalizing.

For this purpose a AC-Coupling is placed before the Speaker-attenuators, which can be activated or internally shorted by Bit7 in the Bass/Treble-Configuration byte. In short condition the input-signal of the speaker-attenuator is available at AC Outputs and the AC Input could be used as

Figure 6. Bass Control @ fc = 80Hz, Q = 1

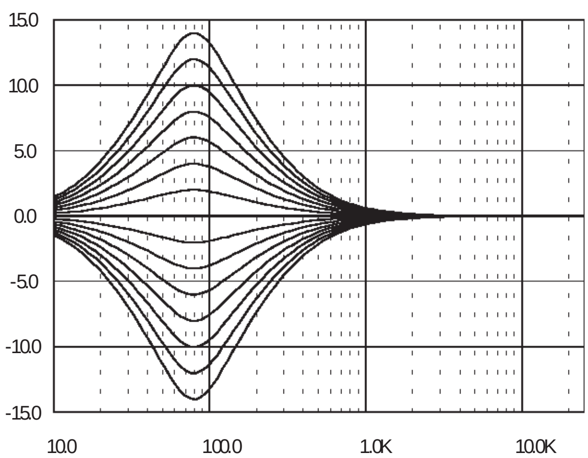


Figure 7. Bass Center @ Gain = 14dB, Q = 1

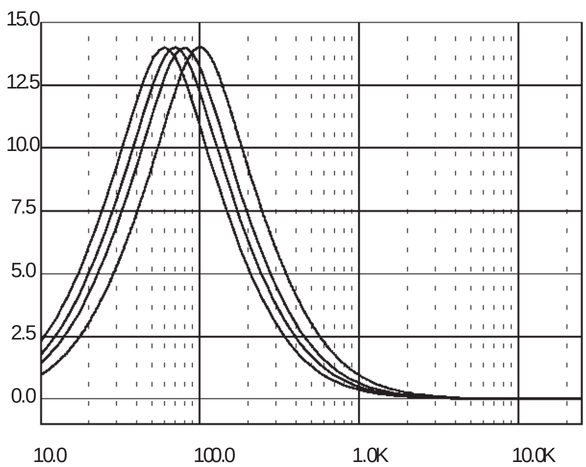


Figure 8. Bass Quality factors @ Gain = 14dB, fc = 80Hz

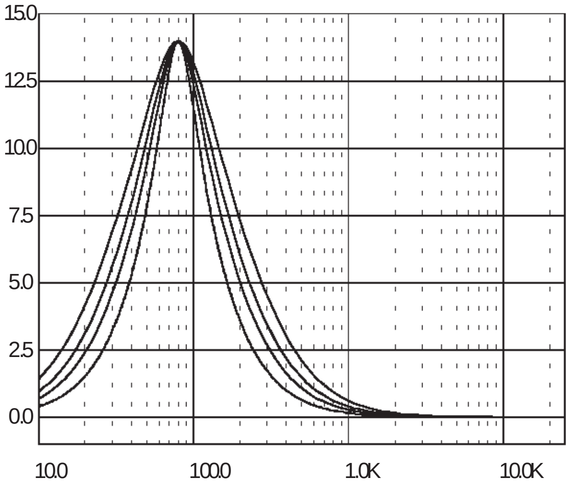
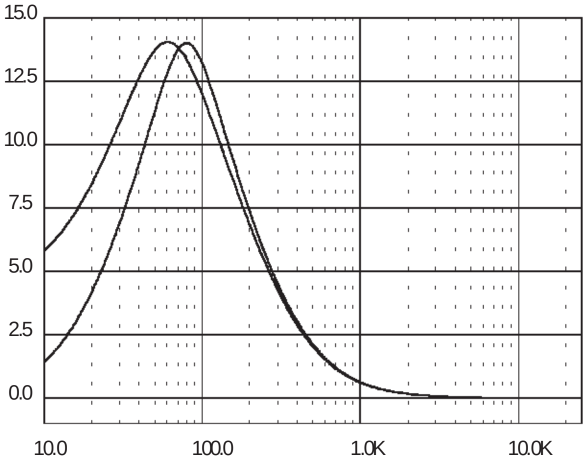


Figure 9. Bass normal and DC Mode @ Gain = 14dB, fc = 80Hz



Note: In general the center frequency, Q and DC-mode can be set independently. The exception from this rule is the mode (5/xx1111xx) where the center frequency is set to 150Hz instead of 100Hz.

Figure 10. Treble Control @ fc = 17.5KHz

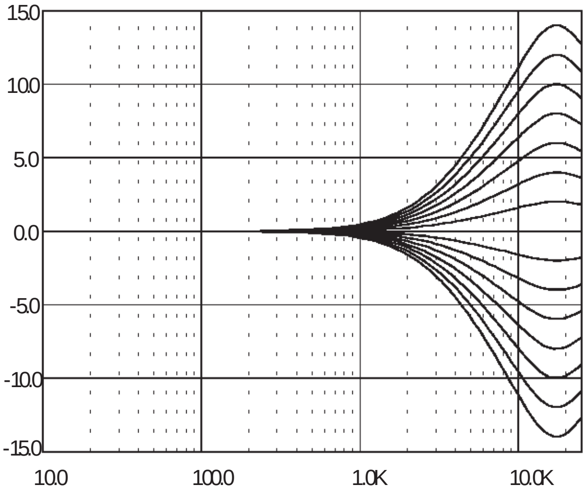
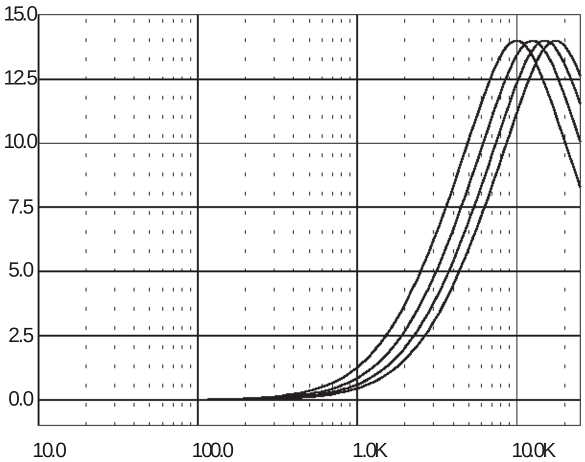


Figure 11. Treble Center Frequencies @ Gain = 14dB



additional stereo inputs. The input impedance of the AC Inputs is always 50KΩ.

Speaker Attenuator

The speaker attenuators have exactely the same structure and range like the Volume stage

FUNCTIONAL DESCRIPTION OF STEREODECODER

The stereodecoder part of the TDA7400 (see Fig. 12) contains all functions necessary to demodulate the MPX signal like pilot tone dependent MONO/STEREO switching as well as "stereoblend" and "highcut" functions.

Stereodecoder Mute

The TDA7400 has a fast and easy to control RDS mute function which is a combination of the audioprocessor's softmute and the high-ohmic mute of the stereodecoder. If the stereodecoder is selected and a softmute command is sent (or activated through the SM pin) the stereodecoder will be set automatically to the high-ohmic mute condition after the audio signal has been softmuted.

Hence a checking of alternate frequencies could be performed. To release the system from the mute condition simply the unmute command must be sent: the stereodecoder is unmuted immediately and the audioprocessor is softly unmuted. Fig. 13 shows the output signal V_O as well as the internal stereodecoder mute signal. This influence of Softmute on the stereodecoder mute can be switched off by setting bit 3 of the Softmute byte to "0". A stereodecoder mute command (bit 0, stereodecoder byte set to "1") will set the stereodecoder in any case independently to the high-ohmic mute state.

If any other source than the stereodecoder is selected the decoder remains muted and the MPX pin is connected to Vref to avoid any discharge of the coupling capacitor through leakage currents.

Ingain + Infilter

The Ingain stage allows to adjust the MPX signal to a magnitude of about 1Vrms internally which is the recommended value. The 4th order input filter has a corner frequency of 80KHz and is used to attenuate spikes and nose and acts as an anti aliasing filter for the following switch capacitor filters.

Demodulator

In the demodulator block the left and the right channel are separated from the MPX signal. In this stage also the 19 kHz pilot tone is cancelled. For reaching a high channel separation the TDA7400 offers an I2C bus programmable roll-off

Figure 12. Block Diagram of the Stereodecoder

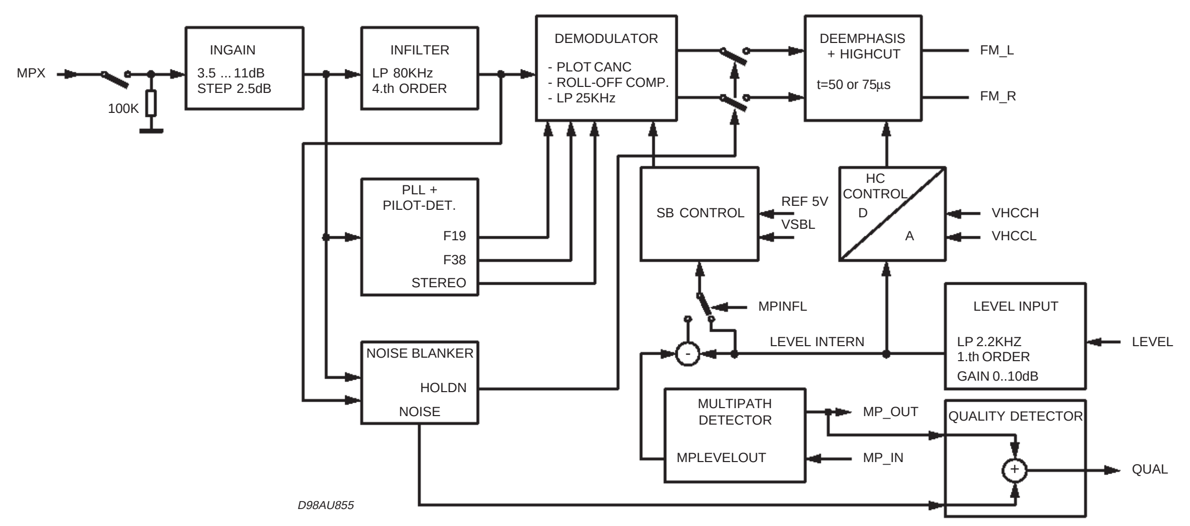


Figure 13. Signals During Stereodecoder's Softmute

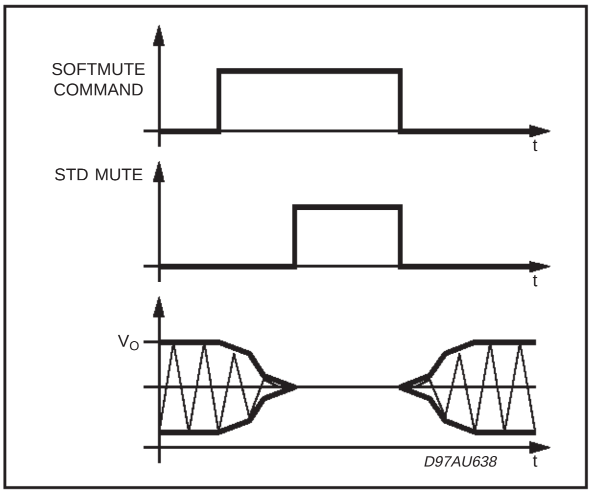
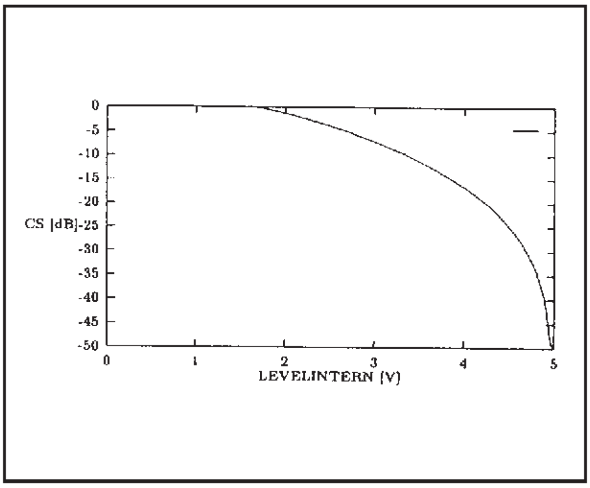


Figure 14. Internal Stereoblend Characteristics



adjustment which is able to compensate the lowpass behaviour of the tuner section. If the tuner attenuation at 38kHz is in a range from 13.8% to 24.6% the TDA7400 needs no external network in front of the MPX pin. Within this range an adjustment to obtain at least 40dB channel separation is possible.

The bits for this adjustment are located together with the fieldstrength adjustment in one byte. This gives the possibility to perform an optimization step during the production of the carradio where the channel separation and the fieldstrength control are trimmed.
The setup of the Stereoblend characteristics which is programmable in a wide range is described in 2.8.

Deemphasis and Highcut.

The lowpass filter for the deemphasis allows to choose between a time constant of 50µs and 75µs (bit D_7, Stereodecoder byte).

The highcut control range will be in both cases $\tau_{HC} = 2 \cdot \tau_{Deemp}$. Inside the highcut control range (between VHCH and VHCL) the LEVEL signal is converted into a 5 bit word which controls the lowpass time constant between $\tau_{Deemp}...3 \cdot \tau_{Deemp}$. There by the resolution will remain always 5 bits independently of the absolute voltage range between the VHCH and VHCL values.

The highcut function can be switched off by I^2C bus (bit D_7, Fieldstrength byte set to "0").

The setup of the highcut characteristics is described in 2.9.

PLL and Pilot Tone Detector

The PLL has the task to lock on the 19kHz pilotone during a stereo transmission to allow a correct demodulation. The included detector enables the demodulation if the pilot tone reaches the selected pilot tone threshold V_{PTHST}. Two different thresholds are available. The detector output (signal STEREO, see block diagram) can be checked by reading the status byte of the TDA7400 via I^2C bus.

Fieldstrength Control

The fieldstrength input is used to control the high cut and the stereoblend function. In addition the signal can be also used to control the noiseblanker thresholds and as input for the multipath detector. These additional functions are described in sections 3.3 and 4.

LEVEL Input and Gain

To suppress undesired high frequency modulation on the highcut and stereoblend function the LEVEL signal is lowpass filtered firstly.

The filter is a combination of a 1st order RC lowpass at 53kHz (working as anti-aliasing filter) and a 1st-order switched capacitor lowpass at 2.2kHz. The second stage is a programmable gain stage to adapt the LEVEL signal internally to different IF device (see Testmode section 5 LEVELINTERN).

The gain is widely programmable in 16 steps from 0dB to 10dB (step = 0.67dB). These 4 bits are located together with the Roll-Off bits in the "Stereodecoder Adjustment" byte to simplify a possible adaptation during the production of the carradio.

Stereoblend Control

The stereoblend control block converts the inter-

Figure 15. Relation Between Internal and External LEVEL Voltage and Setup of Stereoblend

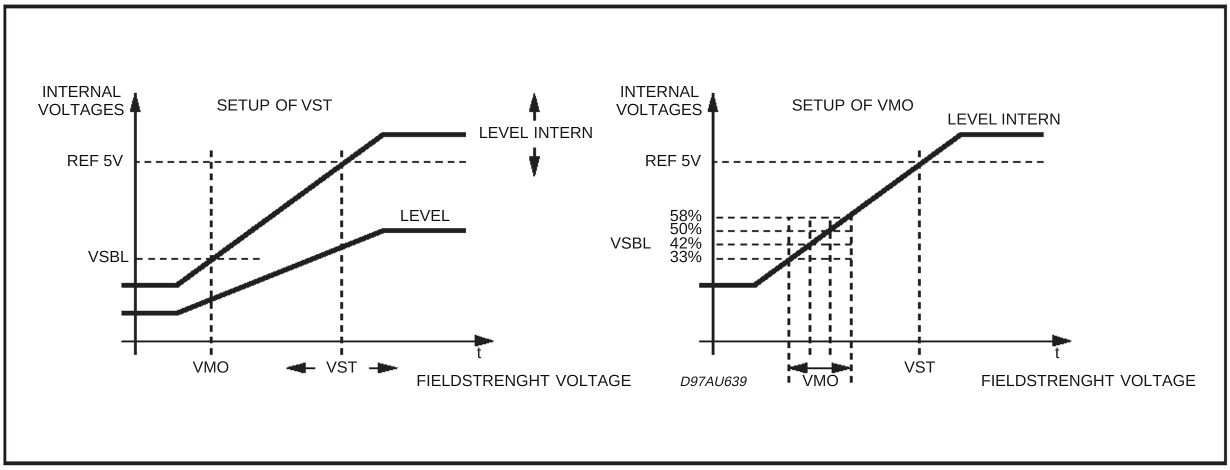
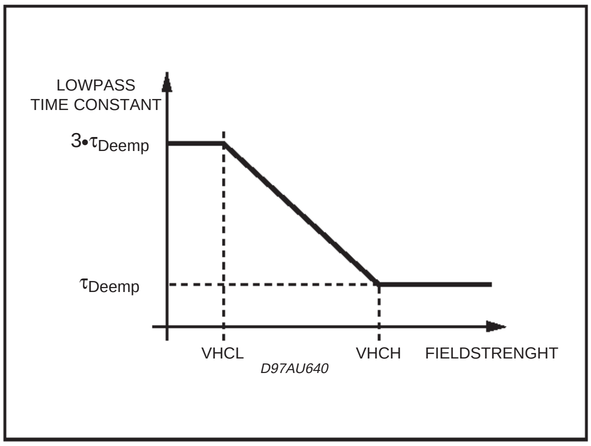


Figure 16. Highcut Characteristics



nal LEVEL voltage (LEVEL INTERN) into an demodulator compatible analog signal which is used to control the channel separation between 0dB and the maximum separation. Internally this control range has a fixed upper limit which is the internal reference voltage REF5V. The lower limit can be programmed between 29.2% and 58%, of REF5V in 4.167% steps (see figs. 11, 12).

To adjust the external LEVEL voltage to the internal range two values must be defined: the LEVEL gain L_G and VSBL (see fig. 12). To adjust the voltage where the full channel separation is reached (VST) the LEVEL gain L_G has to be defined. The following equation can be used to estimate the gain:

$$L_G = \frac{\text{REF5V}}{\text{Fieldstrengthvoltage[STEREO]}}$$

The gain can be programmed through 4 bits in the "Stereodecoder-Adjustment"byte.

The MONO voltage VMO (0dB channel separation) can be choosen selecting VSBL
All necessary internal reference voltages like REF5V are derived from a bandgap circuit. Therefore they have a temperature coefficient near zero. This is useful if the fieldstrength signal is also temperature compensated.

But most IF devices apply a LEVEL voltage with a TC of 3300ppm. The TDA7400 offers this TC for the reference voltages, too. The TC is selectable with bit D_7 of the "stereodecoder adjustment" byte.

Highcut Control

The highcut control setup is similar to the stereoblend control setup : the starting point VHCH can be set with 2 bits to be 42, 50, 58 or 66% of REF5V whereas the range can be set to be 17, 22, 28 or 33% of VHCH (see fig. 21).

FUNCTIONAL DESCRIPTION OF THE NOISE-BLANKER

In the automotive environment the MPX signal is disturbed by spikes produced by the ignition and for example the wiper motor. The aim of the noiseblanker part is to cancel the audible influence of the spikes.

Therefore the output of the stereodecoder is held at the actual voltage for a time between 22 and 38μs (programmable).

The block diagram of the noiseblanker is given in fig.17.

In a first stage the spikes must be detected but to avoid a wrong triggering on high frequency (white) noise a complex trigger control is implemented. Behind the triggerstage a pulse former generates the "blanking" pulse. To avoid any crosstalk to the signalpath the noiseblanker is supplied by his own biasing circuit.

Trigger Path

The incoming MPX signal is highpass filtered, amplified and rectified. This second order high-pass-filter has a corner frequency of 140kHz.

The rectified signal, RECT, is lowpass filtered to generate a signal called PEAK. Also noise with a frequency 140kHz increases the PEAK voltage. The resulting voltage can be adjusted by use of the noise rectifier discharge current.

The PEAK voltage is fed to a threshold generator, which adds to the PEAK voltage a DC dependent threshold VTH. Both signals, RECT and PEAK+VTH are fed to a comparator which triggers a re-triggerable monoflop. The monoflop's output activates the sample-and-hold circuits in the signalpath for selected duration.

Automatic Noise Controlled Threshold Adjustment (ATC)

There are mainly two independent possibilities for programming the trigger threshold:

a the low threshold in 8 steps (bits D_0 to D_2 of the noiseblanker byte)

b the noise adjusted threshold in 4 steps (bits D_3 and D_4 of the noiseblanker byte, see fig. 14).

The low threshold is active in combination with a good MPX signal without any noise; the PEAK voltage is less than 1V. The sensitivity in this operation is high.

If the MPX signal is noisy the PEAK voltage increases due to the higher noise, which is also rectified. With increasing of the PEAK voltage the trigger threshold increases, too. This particular gain is programmable in 4 steps (see fig. ...).

AUTOMATIC THRESHOLD CONTROL MECHANISM

Automatic Threshold Control by the Stereoblend Voltage

Besides the noise controlled threshold adjustment there is an additional possibility for influencing the trigger threshold. It is depending on the stereoblend control.

The point where the MPX signal starts to become noisy is fixed by the RF part. Therefore also the starting point of the normal noise-controlled trigger adjustment is fixed (fig. 11). In some cases the behaviour of the noiseblanker can be improved by increasing the threshold even in a region of higher fieldstrength. Sometimes a wrong triggering occures for the MPX signal often shows distortion in this range which can be avoided even if using a low threshold.
Because of the overlap of this range and the range of the stereo/mono transition it can be controlled by stereoblend. This threshold increase is programmable in 3 steps or switched off with bits D_0 and D_1 of the fieldstrength control byte.

Over Deviation Detector

If the system is tuned to stations with a high deviation the noiseblanker can trigger on the higher frequencies of the modulation. To avoid this wrong behaviour, which causes noise in the output signal, the noiseblanker offers a deviation dependent threshold adjustment.

Figure 17. Block Diagram of the Noiseblanker

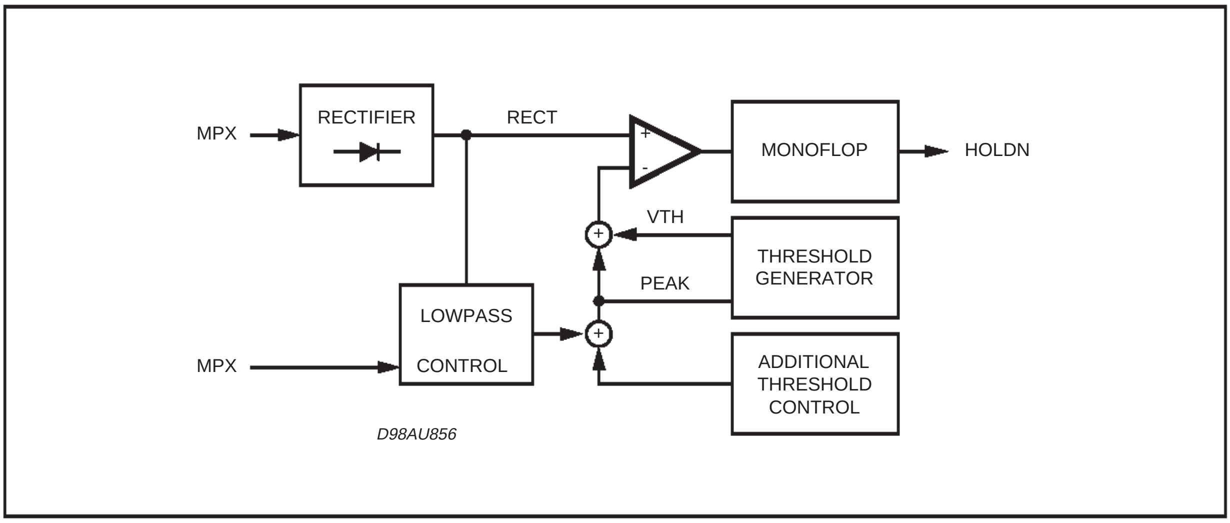
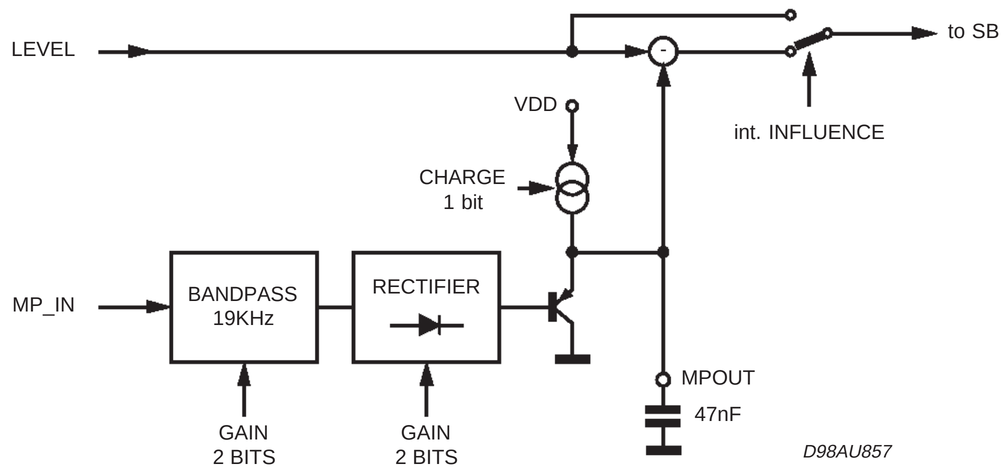


Figure 18. Block Diagram of the Multipath Detector



By rectifying the MPX signal a further signal representing the actual deviation is obtained. It is used to increase the PEAK voltage. Offset and gain of this circuit are programmable in 3 steps with the bits D_6 and D_7 of the stereodecoder byte (the first step turns off the detector, see fig. 15).

FUNCTIONAL DESCRIPTION OF THE MULTIPATH DETECTOR

Using the internal multipath detector the audible effects of a multipath condition can be minimized. A multipath condition is detected by rectifying the 19kHz spectrum in the fieldstrength signal.
An external capacitor is used to define the attack and decay times (see block diagram fig. 23). the MPOUT pin is used as detector output connected to a capacitor of about 47nF and additionally the MPIN pin is selected to be the fieldstrength input. Using the configuration an external adaptation to the user's requiremet is given in fig.25.

Selecting the "internal influence" in the configuration byte, the channel separation is automatically reduced during a multipath condition according to the voltage appearing at the MP_OUT pin. A possible application is shown in fig. 26.

Programming

To obtain a good multipath performance an adaptation is necessary. Therefore tha gain of the 19kHz bandpass is programmable in four steps as well as the rectifier gain. The attack and decay times can be set by the external capacitor value.

QUALITY DETECTOR

The TDA7400 offers a quality detector output which gives a voltage representing the FM reception conditions. To calculate this voltage the MPX noise and the multipath detector output are summed according to the following formula:

$$\text{Quality} = 1.6\,(V_{noise} - 0.8V) + a\,(REF5V - V_{MPOUT})$$

The noise signal is the PEAK signal without additional influences. The factor "a" can be programmed from 0.7 to 1.15. the output is a low impedance output able to drive external circuitry as well as simply fed to an A/D converter for RDS applications.

TEST MODE

During the test mode which can be activated by setting bit D_0 of the testing byte and bit D_5 of the subaddress byte to "1" several internal signals are available at the CASSR pin.

During this mode the input resistor of 100kOhm is disconnected from the pin. The internal signals available are shown in the software specification.

I²C BUS INTERFACE DESCRIPTION

Interface Protocol

The interface protocol comprises:

-a start condition (S)

-a chip address byte (the LSB bit determines read / write transmission)

-a subaddress byte

-a sequence of data (N-bytes + acknowledge)

-a stop condition (P)

CHIP ADDRESS										SUBADDRESS									DATA 1 to DATA n							
	MSB							LSB		MSB							LSB		MSB						LSB	
S	1	0	0	0	1	1	0	R/W	ACK	X	AZ	T	I	A3	A2	A1	A0	ACK				DATA				ACK	P

D97AU627

S = Start

ACK = Acknowledge

AZ = AutoZero-Remain

T = Testing

I = Autoincrement

P = Stop

MAX CLOCK SPEED 500kbits/s

The transmitted data is automatically updated after each ACK. Transmission can be repeated without new chip address.

Auto increment

If bit I in the subaddress byte is set to "1", the autoincrement of the subaddress is enabled.

TRANSMITTED DATA (send mode)

MSB							LSB
X	X	X	X	ST	SM	X	X

SM = 1 Soft mute activated

ST = 1 Stereo mode

X = Not Used

SUBADDRESS (receive mode)

MSB							LSB	FUNCTION
I3	I2	I1	I0	A3	A2	A1	A0	
								AntiRadiation Filter
0								off
1								on
								AutoZero Remain
	0							off
	1							on
								Testmode
		0						off
		1						on
								Auto Increment Mode
			0					off
			1					on
								Databyte Addressing
				0	0	0	0	Input Selector
				0	0	0	1	Volume
				0	0	1	0	Treble
				0	0	1	1	Bass
				0	1	0	0	Speaker attenuator LF
				0	1	0	1	Speaker attenuator RF
				0	1	1	0	Speaker attenuator LR
				0	1	1	1	Speaker attenuator RR
				1	0	0	0	SoftMute / Bass Prog.
				1	0	0	1	Stereodecoder
				1	0	1	0	Noiseblanker
				1	0	1	1	High Cut Control
				1	1	0	0	Fieldstrength & Quality
				1	1	0	1	Configuration
				1	1	1	0	Stereodecoder Adjustment
				1	1	1	1	Testing

DATA BYTE SPECIFICATION

Input Selector (subaddress 0H)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Source Selector
					0	0	0	CD
					0	0	1	Cassette
					0	1	0	Phone
					0	1	1	AM
					1	0	0	Stereo Decoder
					1	0	1	AC Inputs Front
					1	1	0	Mute
					1	1	1	AC inputs Rear
								In-Gain
	0	0	0	0				15dB
	0	0	0	1				14dB
	:	:	:	:				:
	1	1	1	0				1 dB
	1	1	1	1				0 dB
								Coupl. Front Speaker
0								external
1								internal

Volume and Speaker Attenuation (subaddress 1H, 4H, 5H, 6H, 7H)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
1	0	0	1	1	1	1	1	not used configurations
:	:	:	:	:	:	:	:	
1	0	0	1	0	0	0	1	
1	0	0	1	0	0	0	0	
1	0	0	0	1	1	1	1	+15dB
:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	1	+1dB
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	0	0dB
0	0	0	0	0	0	0	1	-1dB
:	:	:	:	:	:	:	:	:
0	0	0	0	1	1	1	1	-15dB
0	0	0	1	0	0	0	0	-16dB
:	:	:	:	:	:	:	:	:
0	1	0	0	1	1	1	0	-78dB
0	1	0	0	1	1	1	1	-79dB
X	1	1	X	X	X	X	X	Mute

Treble Filter (subaddress 2H)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Treble Steps
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								Treble Center Frequency
	0	0						10.0KHz
	0	1						12.5KHz
	1	0						15.0KHz
	1	1						17.5KHz
								Coupl. Rear Speaker
0								external (AC)
1								internal

Bass Filter (subaddress 3H)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Bass Steps
			0	0	0	0	0	-15dB
			0	0	0	0	1	-14dB
			:	:	:	:	:	:
			0	1	1	1	0	-1dB
			0	1	1	1	1	0dB
			1	1	1	1	1	0dB
			1	1	1	1	0	+1dB
			:	:	:	:	:	:
			1	0	0	0	1	+14dB
			1	0	0	0	0	+15dB
								Bass Q-Factor
	0	0						1.0
	0	1						1.25
	1	0						1.50
	1	1						2.0
								Bass DC Mode
0								off
1								on

Soft Mute and Bass Programming (subaddress 8H)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	FUNCTION
								Mute
							0	Enable Soft Mute
							1	Disable Soft Mute
					0	0		Mutetime = 0.48ms
					0	1		Mutetime = 0.96ms
					1	0		Mutetime = 40.4ms
					1	1		Mutetime = 324ms
				0				Stereodecoder Soft Mute Influence = on
				1				Stereodecoder Soft Mute Influence = off
								Bass Center Frequency
		0	0					Center Frequency = 60 Hz
		0	1					Center Frequency = 70 Hz
		1	0					Center Frequency = 80 Hz
		1	1					Center Frequency = 100Hz
		1	1					Center Frequency = 150Hz
								Noise Blanker Time
0	0							38µs
0	1							25.5µs
1	0							32µs
1	1							22µs

1 Only for Bass Q-Factor = 2.0

Stereodecoder (subaddress 9H)

MSB D7	D6	D5	D4	D3	D2	D1	LSB D0	FUNCTION
							0	STD Unmuted
							1	STD Muted
					0	0		In Gain 11dB
					0	1		In Gain 8.5dB
					1	0		In Gain 6dB
					1	1		In Gain 3.5dB
				1				must be ”1”
			0					Forced Mono
			1					Mono/Stereo switch automatically
		0						Noiseblanker PEAK charge current low
		1						Noiseblanker PEAK charge current high
	0							Pilot Threshold HIGH
	1							Pilot Threshold LOW
0								Deemphasis 50µs
1								Deemphasis 75µs

Noiseblanker (subaddress AH)

MSB							**LSB**	**FUNCTION**
D7	D6	D5	D4	D3	D2	D1	D0	
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	Low Threshold 65mV Low Threshold 60mV Low Threshold 55mV Low Threshold 50mV Low Threshold 45mV Low Threshold 40mV Low Threshold 35mV Low Threshold 30mV
			0 0 1 1	0 1 0 1				Noise Controlled Threshold 320mV Noise Controlled Threshold 260mV Noise Controlled Threshold 200mV Noise Controlled Threshold 140mV
		0 1						Noise blanker OFF Noise blanker ON
0 0 1 1	0 1 0 1							Over deviation Adjust 2.8V Over deviation Adjust 2.0V Over deviation Adjust 1.2V Over deviation Detector OFF

High Cut (subaddress BH)

MSB							**LSB**	**FUNCTION**
D7	D6	D5	D4	D3	D2	D1	D0	
							0 1	High Cut OFF High Cut ON
					0 0 1 1	0 1 0 1		Max. High Cut 2dB Max. High Cut 5dB Max. High Cut 7dB Max. High Cut 10dB
			0 0 1 1	0 1 0 1				VHCH at 42% REF 5V VHCH at 50% REF 5V VHCH at 58% REF 5V VHCH at 66% REF 5V
	0 0 1 1	0 1 0 1						VHCL at 16.7% VHCH VHCL at 22.2% VHCH VHCL at 27.8% VHCH VHCL at 33.3% VHCH
 0 1								**Strong Multipath influence on PEAK 18K** OFF ON (18K Discharge if V_{MPOUT} <2.5V)

Fieldstrength Control (subaddress CH)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
					0 0 0 0 1 1 1 1	0 0 1 1 0 0 1 1	0 1 0 1 0 1 0 1	VSBL at 29% REF 5V VSBL at 33% REF 5V VSBL at 38% REF 5V VSBL at 42% REF 5V VSBL at 46% REF 5V VSBL at 50% REF 5V VSBL at 54% REF 5V VSBL at 58% REF 5V
			0 0 1 1	0 1 0 1				Noiseblanker Field strength Adj 2.3V Noiseblanker Field strength Adj 1.8V Noiseblanker Field strength Adj 1.3V Noiseblanker Field strength Adj OFF
	0 0 1 1	0 1 0 1						Quality Detector Coefficient a = 0.7 Quality Detector Coefficient a = 0.85 Quality Detector Coefficient a = 1.0 Quality Detector Coefficient a = 1.15
0 1								Multipath off influence on PEAK discharge -1V/ms (at MPout = 2.5V

Configuration (subaddress DH)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
						 0 0 1 1	 0 1 0 1	**Noise Rectifier Discharge Resistor** R = infinite R = 56kΩ R = 33kΩ R =18kΩ
				 0 1 0 1	 0 0 1 1			**Multipath Detector Bandpass Gain** 6dB 12dB 16dB 18dB
			 0 1					**Multipath Detector internal influence** ON OFF
		0 1						Multipath Detector Charge Current 0.5µA Multipath Detector Charge Current 1µA
 0 0 1 1	 0 1 0 1							**Multipath Detector Reflection Gain** Gain = 7.6dB Gain = 4.6dB Gain = 0dB disabled

Stereodecoder Adjustment (subaddress EH)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Roll Off Compensation
					0	0	0	not allowed
					0	0	1	19.6%
					0	1	0	21.5%
					:	:	:	:
					1	0	0	25.3%
					:	:	:	:
					1	1	1	31.0%
								Level Gain
	0	0	0	0				0dB
	0	0	0	1				0.66dB
	0	0	1	0				1.33dB
	:	:	:	:				:
	1	1	1	1				10dB
1								must be ”1”

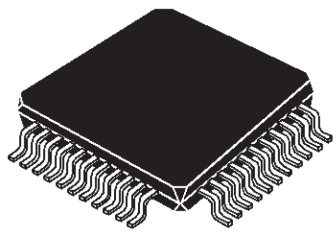
Testing (subaddress FH)

MSB							LSB	FUNCTION
D7	D6	D5	D4	D3	D2	D1	D0	
								Stereodecoder test signals
							0	OFF
							1	Test signals enabled if bit D5 of the subaddress (test mode bit) is set to ”1”, too
						0		External Clock
						1		Internal Clock
								Testsignals at CASS_R
		0	0	0	0			VHCCH
		0	0	0	1			Level intern
		0	0	1	0			Pilot magnitude
		0	0	1	1			VCOCON; VCO Control Voltage
		0	1	0	0			Pilot threshold
		0	1	0	1			HOLDN
		0	1	1	0			NB threshold
		0	1	1	1			F228
		1	0	0	0			VHCCL
		1	0	0	1			VSBL
		1	0	1	0			not used
		1	0	1	1			not used
		1	1	0	0			PEAK
		1	1	0	1			not used
		1	1	1	0			REF5V
		1	1	1	1			not used
								VCO
	0							OFF
	1							ON
								Audioprocessor test mode
0								enabled if bit D5 of the subaddress (test mode bit) is set to ”1”
1								OFF

Note : This byte is used for testing or evaluation purposes only and must not be set to other values than the default ”11111110” in the application!

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10)