AN1088
APPLICATION NOTE

L6234 THREE PHASE MOTOR DRIVER

by Domenico Arrigo

INTRODUCTION

The L6234 is a DMOSs triple half-bridge driver with input supply voltage up 52V and output current of 5A. It can be used in a very wide range of applications.

It has been realized in Multipower BCD60II technology which allows the combination of isolated DMOS transistors with CMOS and Bipolar circuits on the same chip. It is available in Power DIP 20 (16+2+2) and in Power SO 20 packages.

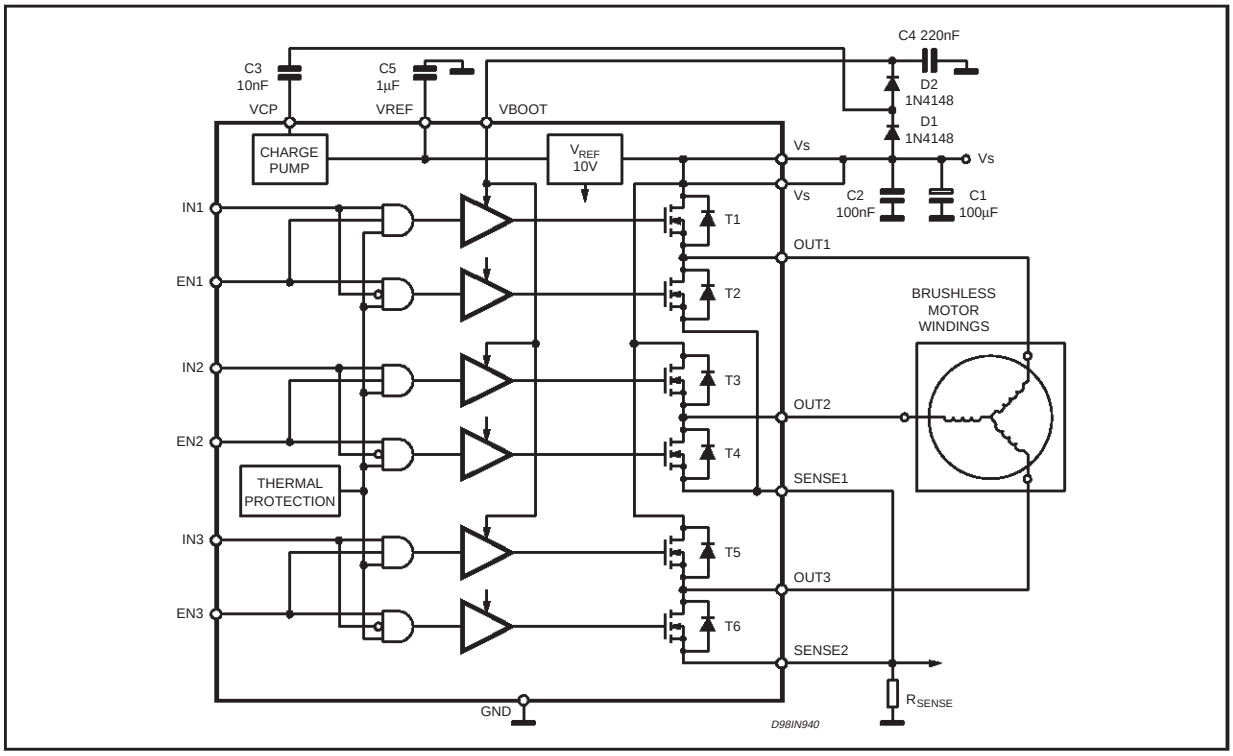
All the inputs are TTL/CMOS compatible and each half bridge can be driven by its own dedicated input and enable.

The DMOS structure has an intrinsic free wheeling body diode so the use of external diodes, which are necessary in the bipolar configuration, can be avoided. The DMOS structure allows a very low quiescent current of 6.5 mA typ. at Vs=42V , irrespective of the load.

DEVICE DESCRIPTION

The device is composed of three channels. Each channel is composed of a half bridge with two power DMOS switches (typ. Rdson of 300mW @ 25°C) and intrinsic free wheeling diodes. Each channel includes two TTL/CMOS and uP compatible comparators, and a logic block to interface the inputs with the drivers. The device includes an internal bandgap reference of 1.22V, a 10V voltage reference to supply the internal circuitry of the device, a central charge pump to drive the upper DMOS switch, thermal shutdown protection and an internal hysteretic function which turns off the device when the junction temperature exceeds approximately 160 °C. Hysteresys is about 20 °C.

Figure 1. L6234 Block Diagram



PIN DESCRIPTION.

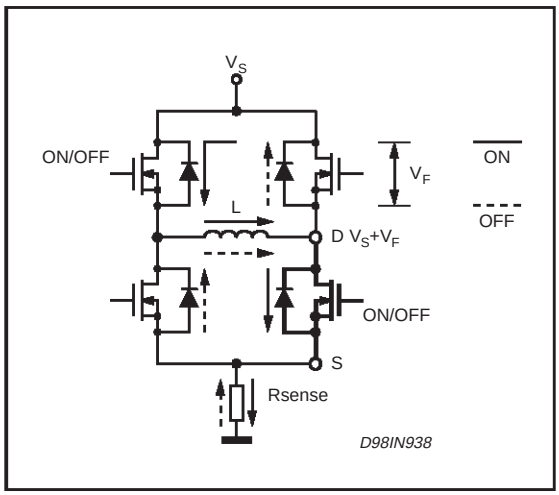
Vs (INPUT SUPPLY VOLTAGE PINS).

These are the two input supply voltage pins. The unregulated input DC voltage can range from 7V to 52V.

With inductive loads the recommended operating maximum supply voltage is 42V to prevent overvoltage applied to the low side Mos. In fact considering a full bridge configuration (see fig. 2), when the bridge is switched off (ENABLE CHOPPING) the current recirculation produces a negative voltage to the source of the lower DMOS switches. In this condition the drain voltage (point D in fig. 2) is V_S + V_F, so the drain-source voltage of this DMOS switch can be some Volts higher than the V_S voltage. The input capacitors C1 and C2 are chosen in order to reduce overvoltage.

The device can sustain a 4A DC input current for each of the two Vs pins, in accordance with the power dissipation.

Figure 2.



OUT1, OUT2, OUT3 (OUTPUTS). These are the output pins that correspond to the mid point of each half bridge. They are designed to sustain a DC current of 4A.

SENSE1, SENSE2.

SENSE1 is the common source of the lower DMOS of the half bridge 1 and 2.

SENSE2 is the source of the lower DMOS of the half bridge 3.

Each of these pins can handle a current of 5A.

A resistance, Rsense, connected to these pins provides feedback for motor current control.

Care must be taken with the negative voltage applied to these pins : negative DC voltage lower than -1V could damage the device. For duration lower than 300ns the device can sustain pulsed negative voltage up to -4V.

For example, if enable chopping current control method is used, negative voltage pulses appear to these pins, due to the current recirculation through the sensing resistor.

Vref (Voltage Reference).

This is the internal 10V voltage reference pin to bias the logic and the low voltage circuitry of the device. A 1µF electrolytic capacitor connected from this pin to GND ensures the stability of the DMOS drive circuit. This pin can be externally loaded up to 5mA . Figure 3 and 4 show the typical behavior of the Vref pin.

Vcp (CHARGE PUMP).

This is the internal oscillator output pin for the charge pump. The oscillator supplied by the 10V Voltage Reference switches from GND to 10V with a typical frequency of

Figure 3. Reference Voltage vs. Junction Temperature.

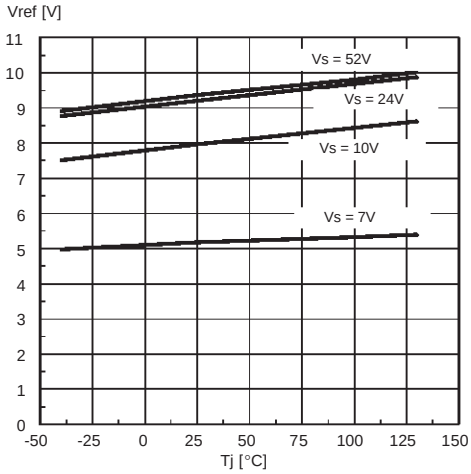
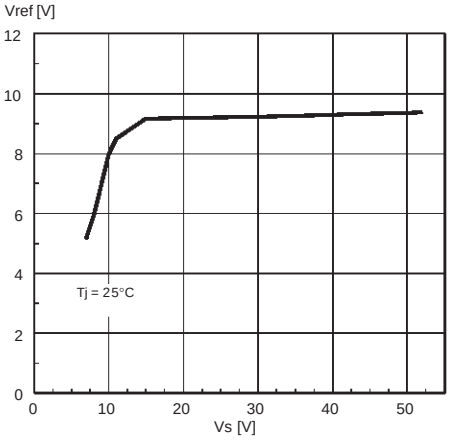


Figure 4. Reference Voltage vs. Supply Voltage.

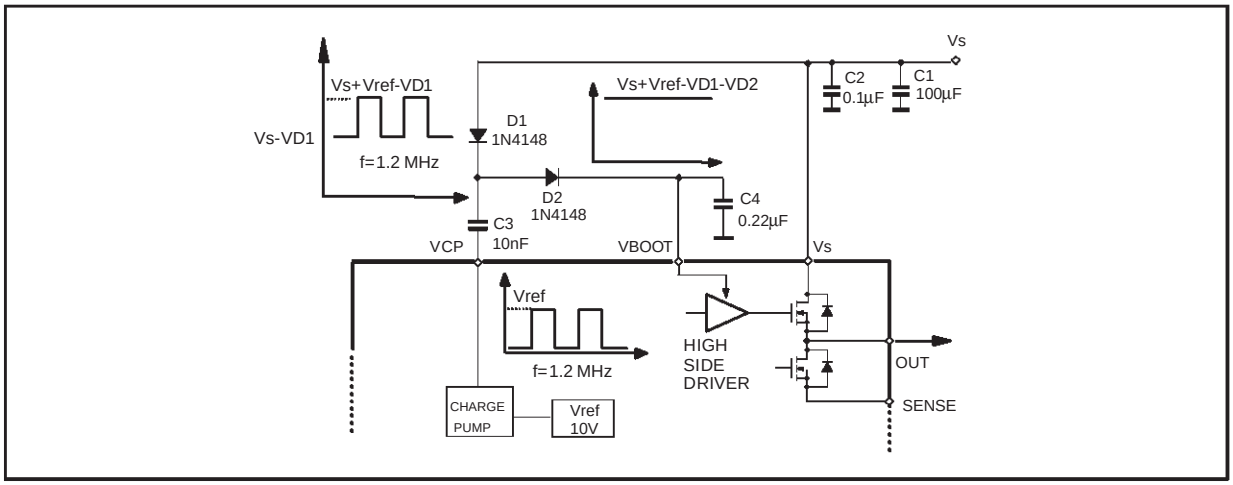


1.2MHz (see fig 4). When the oscillator output is at ground , C3 is charged by Vs through D1. When it rises to 10V, D1 is reverse biased and the charge flows from C3 to C4 through D2, so the Vboot pin after a few cycles reaches the maximum voltage of Vs + 10V - VD1- VD2.

Vboot (BOOTSTRAP).

This is the input bootstrap pin which gives the overvoltage necessary to drive all the upper DMOS of the three half bridges (see fig 5).

Figure 5. Charge Pump Circuit.



LOGIC INPUTS PINS.

EN1, EN2, EN3 (ENABLES).

These pins are TTL/CMOS and µP compatible. Each half bridge can be enabled by its own dedicated pin with a logic HIGH. The logic LOW on these pins switches off the related half bridge (see Fig. 6). The maximum switching frequency is 50kHz.

Figure 6. Control logic for each half bridge.

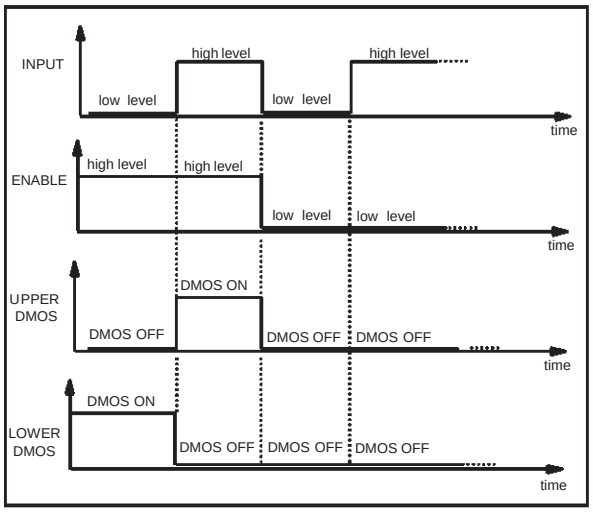
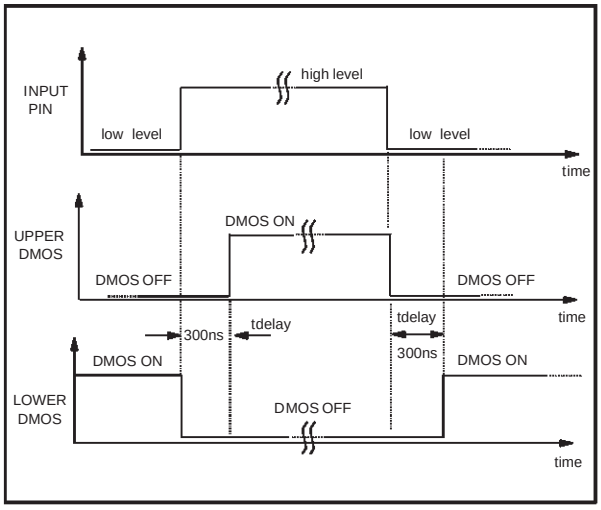


Figure 7. Cross Conduction Protection.



IN1, IN2, IN3 (INPUTS).

These pins are TTL/CMOS and µP compatible. They allow switching on the upper DMOS (INPUT at high logic level) or the lower Dmos (INPUT at low logic level) in each half bridge (see Fig. 6).

Cross conduction protection (see Fig. 7) avoids simultaneously turning on both the upper and lower DMOS of each half bridge. There is a fixed delay time of 300ns between the turn on and the turn off of the two DMOS switches in each half bridge. The switching operating frequency is up 50kHz. High commutation frequency permits the reduction of ripple of the output current but increases the device's power dissipation, however low commutation frequency causes high ripple of the output current. The switching frequency should be higher than 16kHz to avoid acoustic noises.

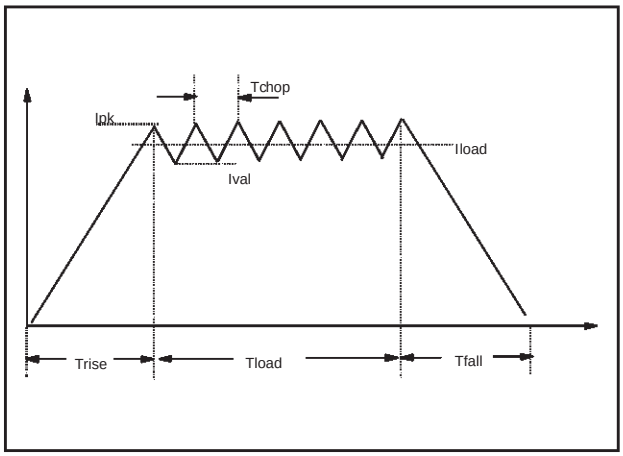
The sink current at the INPUTS and ENABLES pins is approximately 30µA if the voltage to these pins is at least 1V less than the Vref voltage (see Fig. 3 and Fig. 4). To avoid overload of the logic INPUTS and ENABLES , voltage should be applied to Vs prior to the logic signal inputs.

POWER DISSIPATION

An evaluation of the power dissipation of the IC driving a three phase motor in a chopping current control application follows.

With a simplified approach it can be distinguished three periods (see Fig. 8) :

Figure 8.



Rise Time, Tr, period.

This is the rise time period, Tr, in which the current switches from one winding to another. In this time a DMOS is switched on and the current increases up to the peak value Ipk with the law i(t) = (Ipk/Tr) t. The energy lost for the rise time in the period T is :

$$Erise = \int_0^{Tr} Rdson \cdot i^2(t)dt = Rdson \cdot I^2pk \cdot \frac{Tr}{3}$$

Fall Time,Tf, period.

When the current switches from one winding to another, there is a fall time in which the current that flows in the intrisic diode of the DMOS decreases from Ipk to zero. If VD is the voltage fall of the diode, the energy lost is :

$$Efall = \int_0^{tf} VD(t) \cdot i(t)dt$$

Tload

During this time the current that flows in the winding is limited by the chopping current control. The energy dissipated due to the ON resistance of the DMOS is :

$$Eload = Rdson \cdot (I_{rms})^2 \cdot Tload$$

In the formula, Irms is the RMS load current, given by :

$$Irms = Iload + \frac{I_{pk} - Ival}{\sqrt{3}}$$

and Iload is the average load current.

When the switch is ON, the energy dissipated due to the commutation of the chopping current control in the DMOS can be assumed to be:

$$Eon = Vs \cdot Ival \cdot \frac{tcom}{2}$$

where tcom is the commutation time of the DMOS switch.

When the switch is OFF :

$$Eoff = Vs \cdot Ipk \cdot \frac{tcom}{2}$$

The energy lost by commutation in a chopping period, given by Eon + Eoff, is :

$$Ecom = Vs \cdot Iload \cdot tcom$$

The energy lost by commutation during the Tload time is given by :

$$Ecom = Vs \cdot Iload \cdot tcom \cdot Tload \cdot fchop$$

Quiescent Power Dissipation, Pq.

The power dissipation due to the quiescent current is $Pq = Vs \cdot Iq$, in which Iq is the quiescent current at the chopping frequency, fchop = 1/Tchop.

Total Power Dissipation.

Let's evaluate the power dissipation of the device driving a three phase brushless motor in chopping current control. In the driving sequence only one upper DMOS and a lower one are on at the same time (see fig. 9 and 10). The total power dissipation is given by :

$$Ptot = \frac{2 \cdot (Erise + Efall + Eload + Ecom)}{T} + Pq$$

Figure 11 shows the total power dissipation, Pd, of the L6234 driving a three phase brushless motor in input chopping current control at different chopping frequency.

EVALUATION BOARD.

The L6234 Power SO20 board has been realized to evaluate the device driving, in closed loop control, a three phase brushless motor with open collector Hall effect sensors.

Figure 9. Input chopping current circulation.

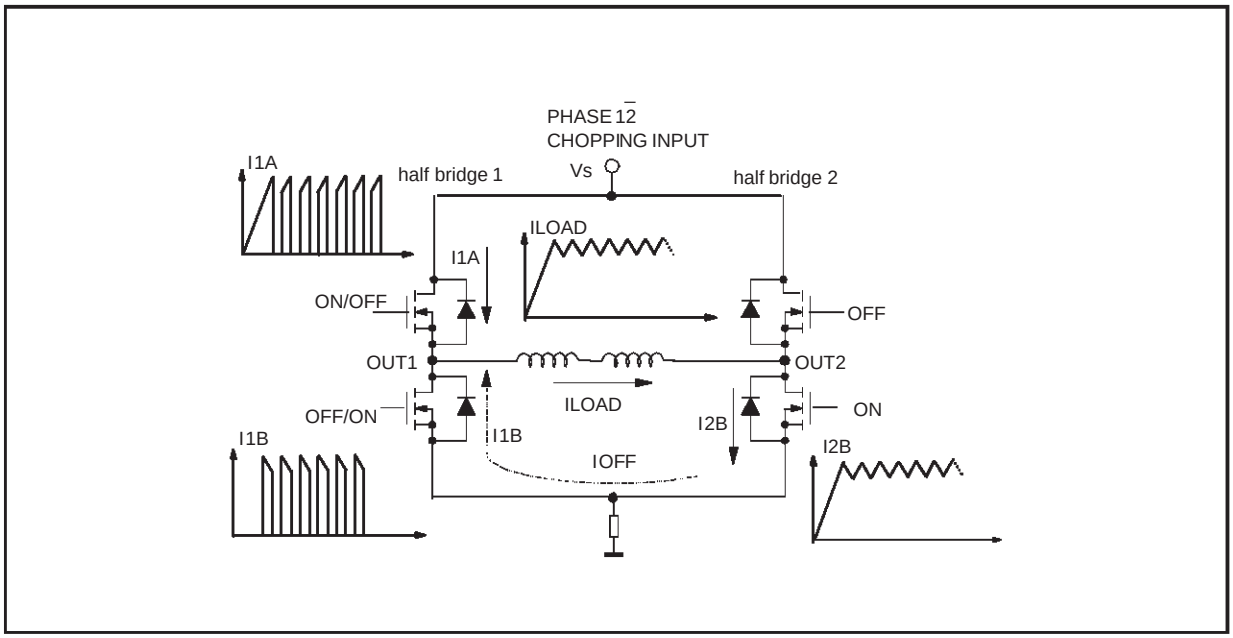
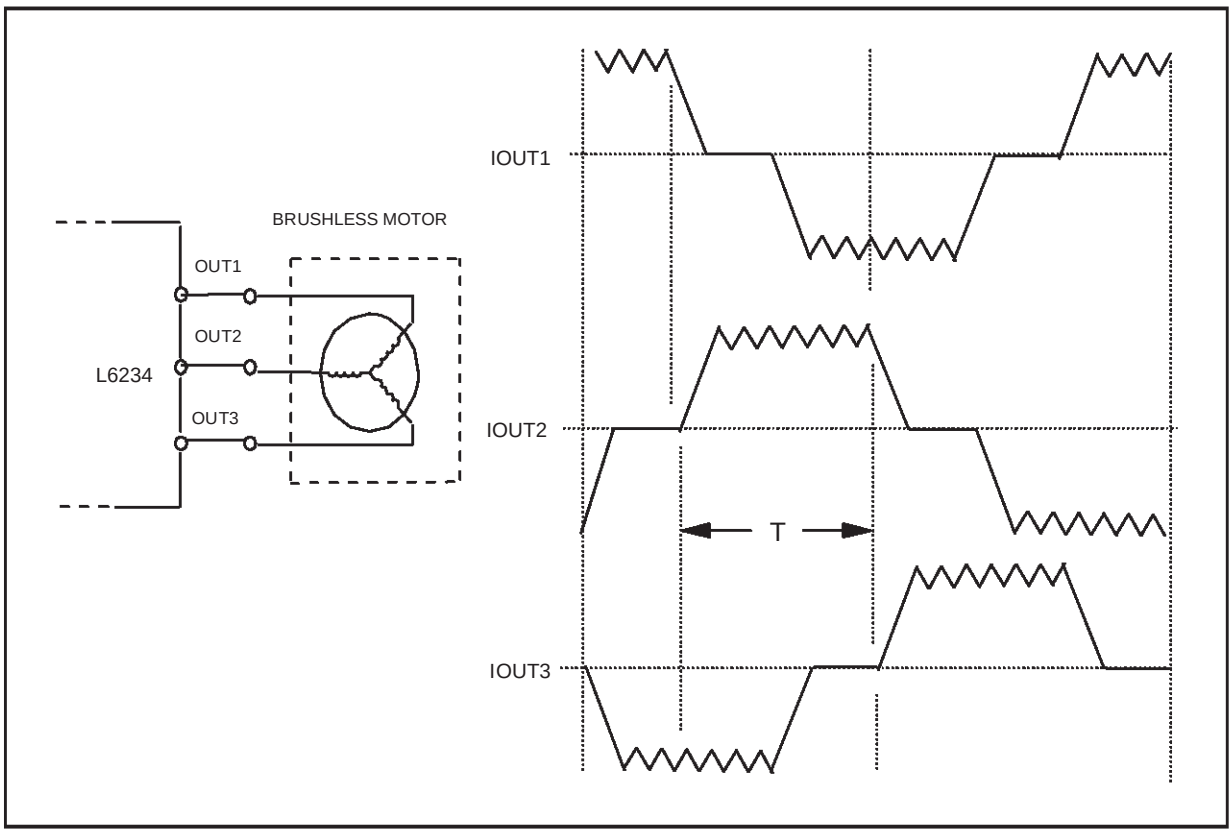


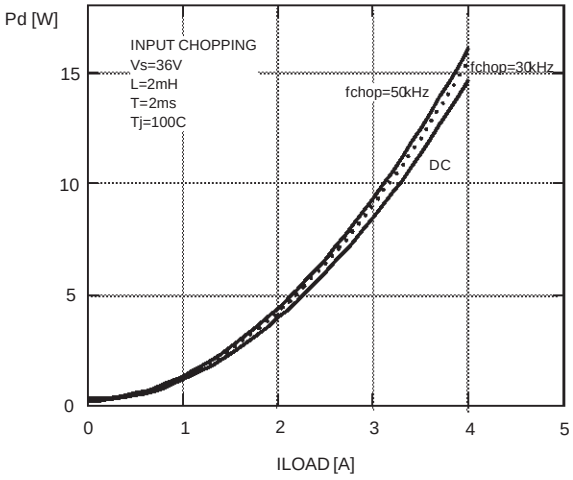
Figure 10. Three Phase Brushless motor control sequence.



The device soldered on the copper heat dissipating area on the board ,without any additional heat sink, can sustain a DC load current of 2.3 A at T_{amb} of approximately 40 °C.

The board provides a closed loop speed and torque control, with a constant TOFF chopping current control method. It allows the user to change the direction and brake the motor.

Figure 11. L6234 Power Dissipation in Three Phase Brushless Motor Control.



Constant t_{OFF} Chopping Current Control.

When the current through the motor exceeds the threshold, fixed by the ratio between the control voltage Vcontrol and the sensing resistor, Rsense, an error signal is generated, the output of the LM393 comparator switches to ground. This state is maintained by the monostable (M74HC123) for a constant delay time (t_{OFF}) generating a PWM signal that achieves the chopping current control. The PWM signal is used for chopping the INPUT pattern. During the toff in chopping current control, the current flows in the low side loop (see fig. 9) and does not flow through the sensing resistor.

The t_{OFF} value can be set by the R9 and C11 to values shown in the table 1.

A suitable value of toff for the majority of applications is 30µs. The larger the t_{OFF}, the higher is the current ripple. If the t_{OFF} is too large the ripple current becomes excessive . On the other hand if the t_{OFF} is too small the winding current cannot decrease under the threshold and current regulation is not guaranteed.

Figure 12. Application board Schematic Circuit.

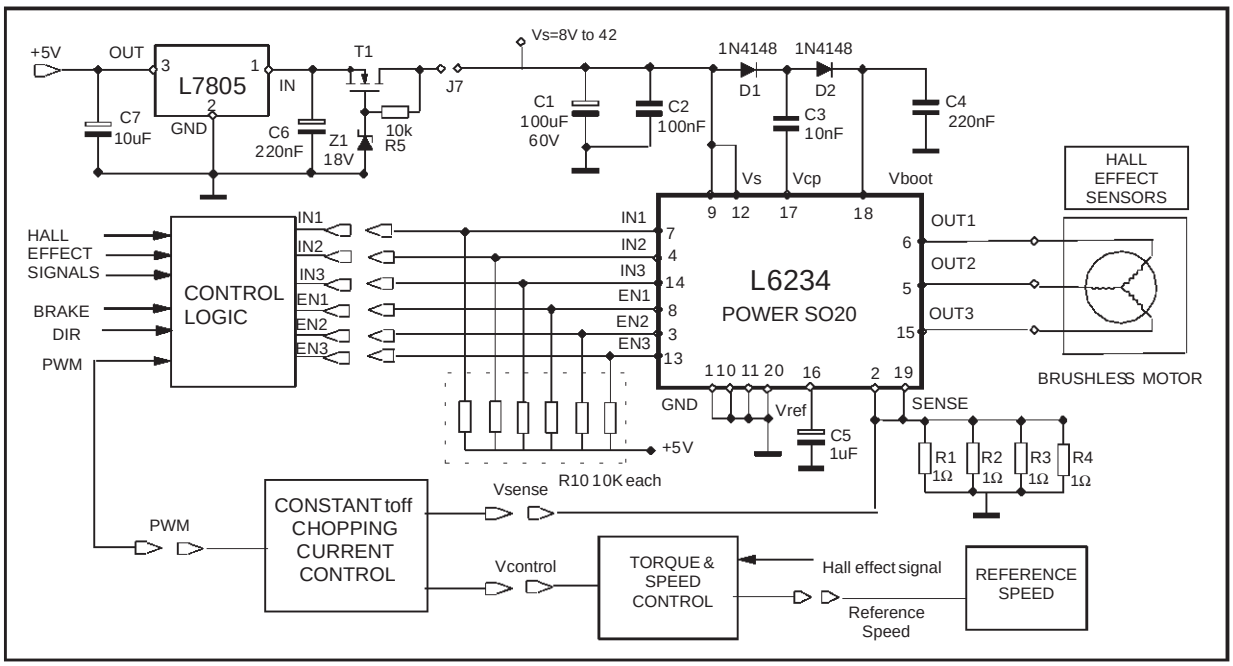


Figure 13. Costant toff current control.

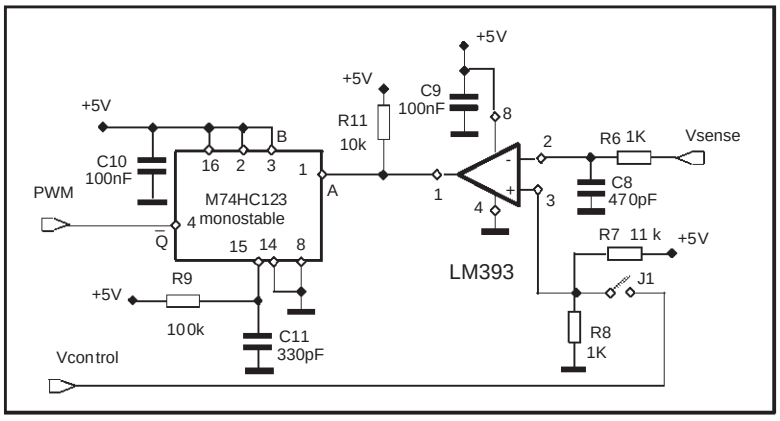


Table 1. toff selection

toff	R9	C11
20µs	100k	270pF
30µs	100k	330pF
45µs	100k	560pF
70µs	100k	1nF

Torque & Speed Closed Loop Control.

The motor's rotational speed is determined by the frequency of the Hall effect signals. The speed control loop has been achieved by comparing this frequency with a frequency of a reference oscillator (see fig. 14) that corresponds to a desired speed limit.

Figure 14. PLL Motor Control.

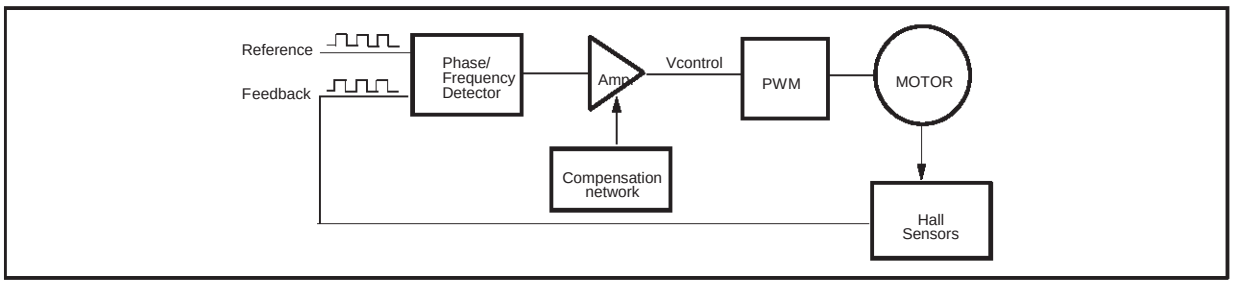
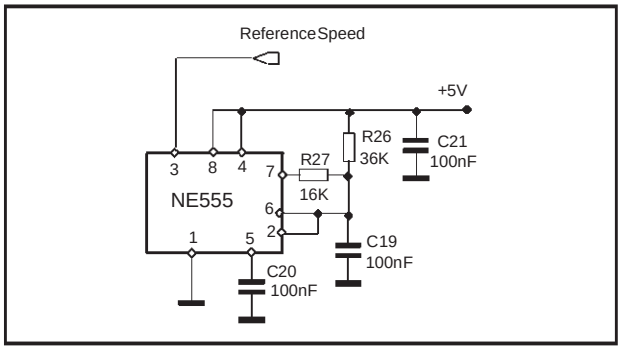


Figure 15. Oscillator for Reference Speed.



When the hall effect signal frequency is lower than the reference frequency, the control voltage is maintained to a value that sets the motor current limit and therefore the torque control limit. The peak current limit is given by Ipeak = Vcontrol/Rsense.

When the frequency from the Hall Effect sensors exceeds the reference frequency and an error signal is generated by the PLL (see Fig. 14). An LM358 comparator, a loop amplifier and an auxiliary OP-AMP ensure the right gain and filtering to guarantee the stability (see fig.16). The error signal causes Vcontrol decrease to a value that sets the PWM chopping current control in order to reduce the torque and set the desired speed. The motor speed is regulated to within ± 0.02 % of the desired speed.

Figure 16. Phase Locked Loop and filtering.

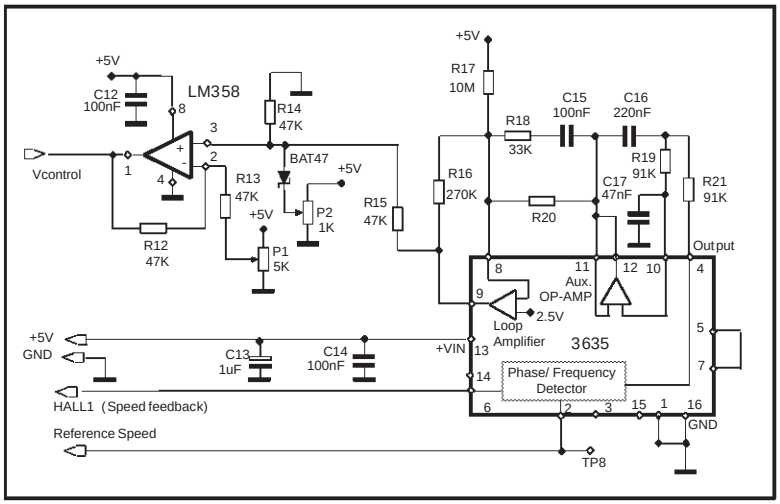
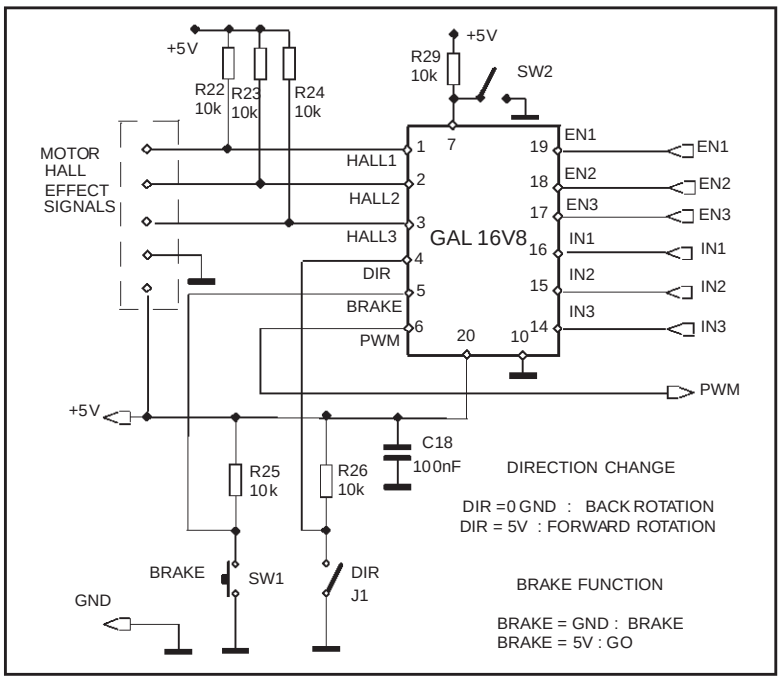


Figure 17. Control Logic Circuit.



Control Logic Circuit.

The logic sequence to the motor is generated by a GAL16V8, which decodes the Hall Effect signals and generates the INPUT and ENABLE pattern shown in Fig. 18.

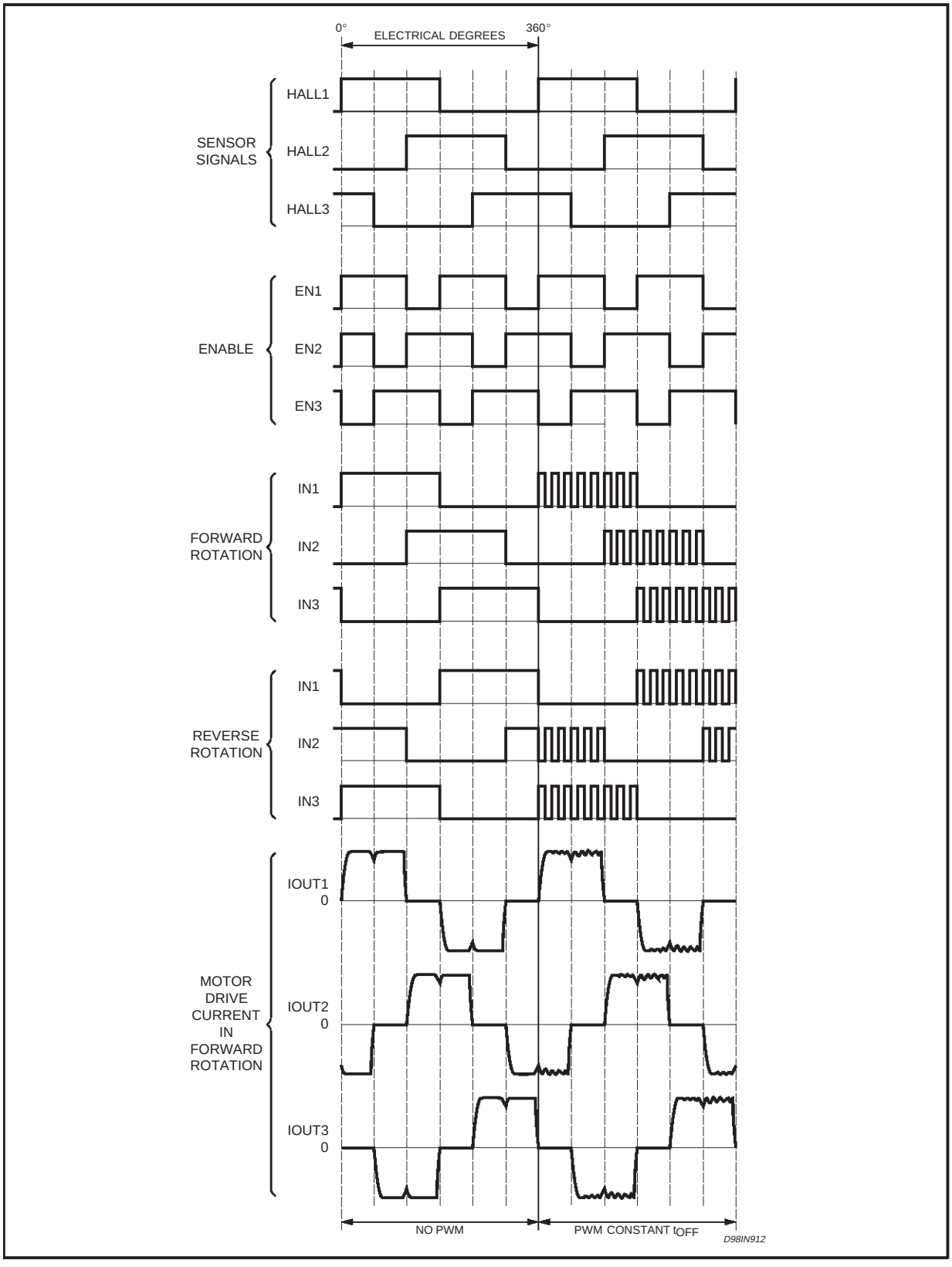
The brake function is obtained by setting the input pattern to logic low and thus turning on the lower DMOS switches of the enabled half-bridges.

The PWM signal is used for chopping the INPUT pattern.

The control logic circuit decodes Hall effect sensors having different phasing.

With the DIR jumper opened the application achieves forward rotation for motors having 60° and 120° Hall Effect sensor electrical phasing and the reverse rotation for motors having 300° and 240° Hall Effect sensor phasing.

Figure 17.


0°
ELECTRICAL DEGREES
360°
SENSOR SIGNALS
HALL1
HALL2
HALL3
ENABLE
EN1
EN2
EN3
FORWARD ROTATION
IN1
IN2
IN3
REVERSE ROTATION
IN1
IN2
IN3
MOTOR DRIVE CURRENT IN FORWARD ROTATION
IOUT1
0
IOUT2
0
IOUT3
0
NO PWM
PWM CONSTANT tOFF
D98IN912

Connecting the DIR jumper to ground sets the reverse rotation for motors having 60° and 120° Hall sensors phasing and the forward rotation for motors having 300° and 240° Hall sensor phasing.
The SW2 switch performs the start-stop function.

Layout Considerations.

Special attention must be taken to avoid overvoltages at Vs and additonal negative voltages to the SENSE pins and noise due to distributed inductance. Thus the input capacitor must be connected close to the Vs pins with symmetrical paths. The paths between the SENSE pins and the input capacitor ground have to be minimized and symmetrical . The sensing resistors must be non-inductive. The device GND has to be connected with a separate path to the input capacitor ground.

Figure 19. Application Board Layout.

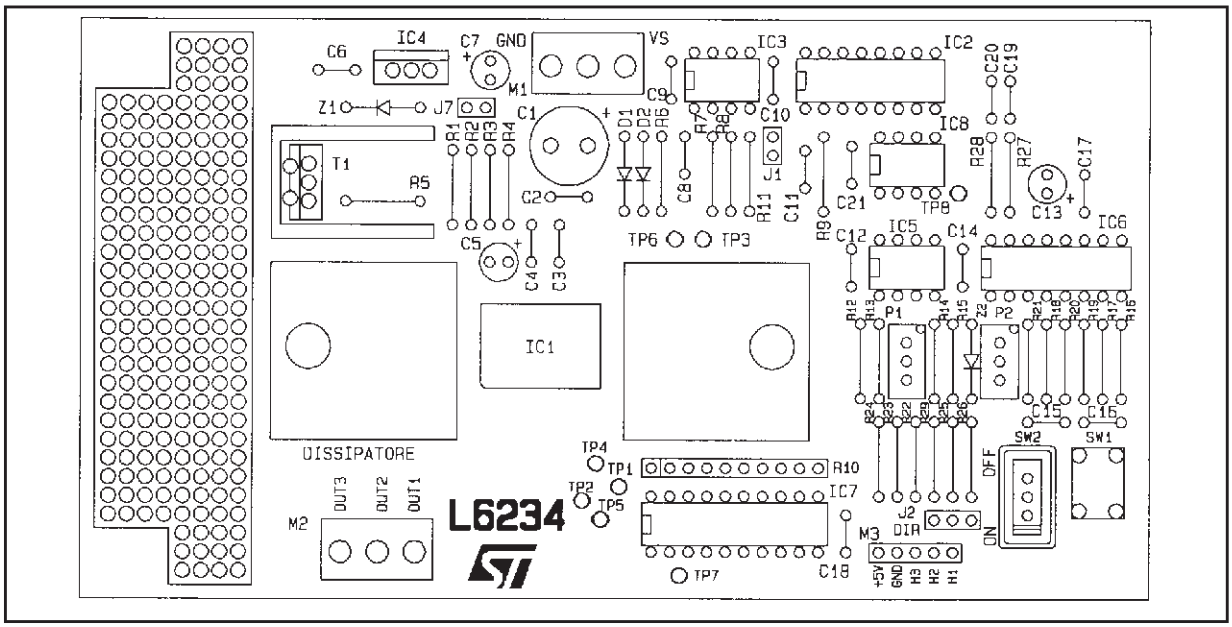


Figure 20. Component side.

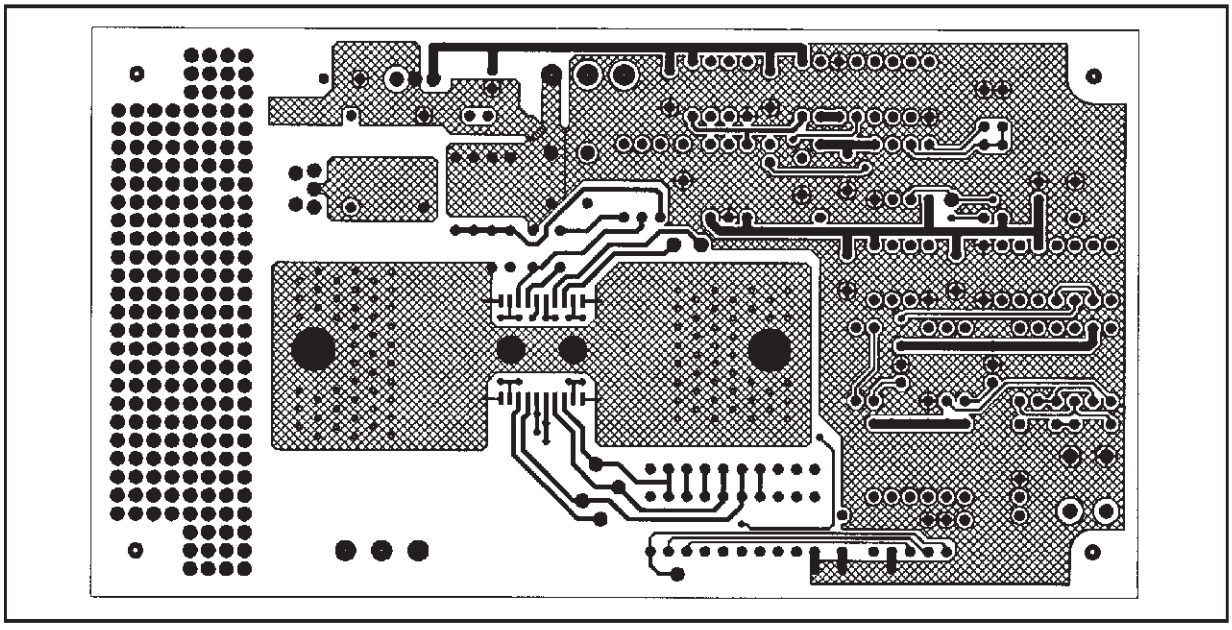
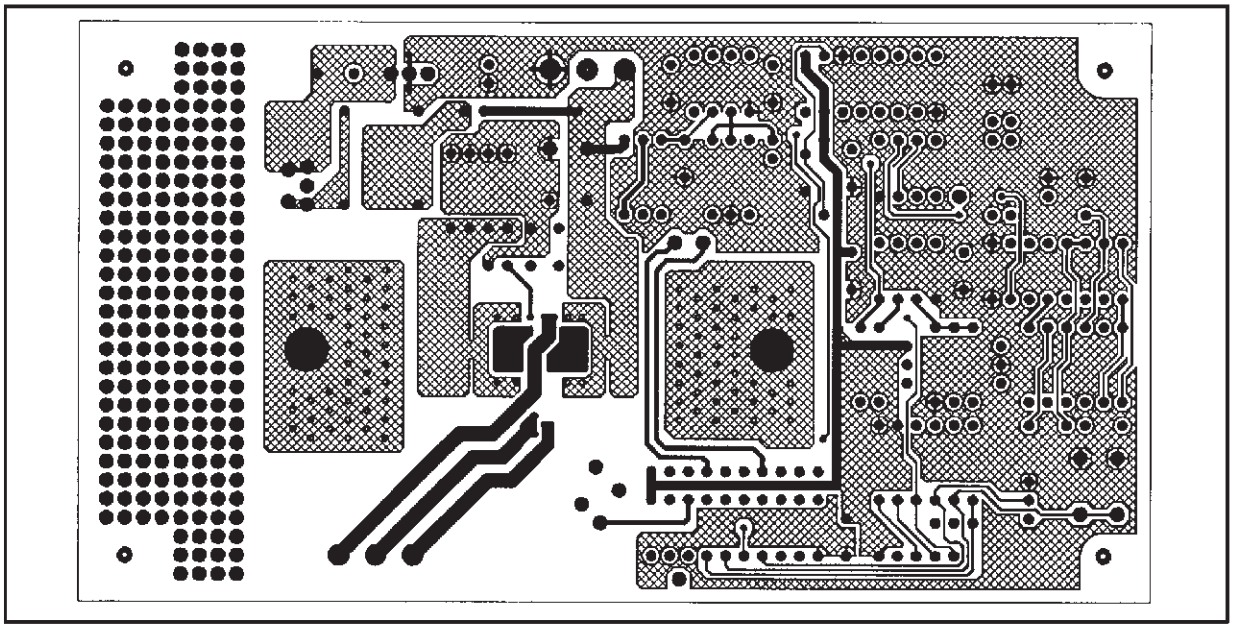


Figure 21. Copper side.



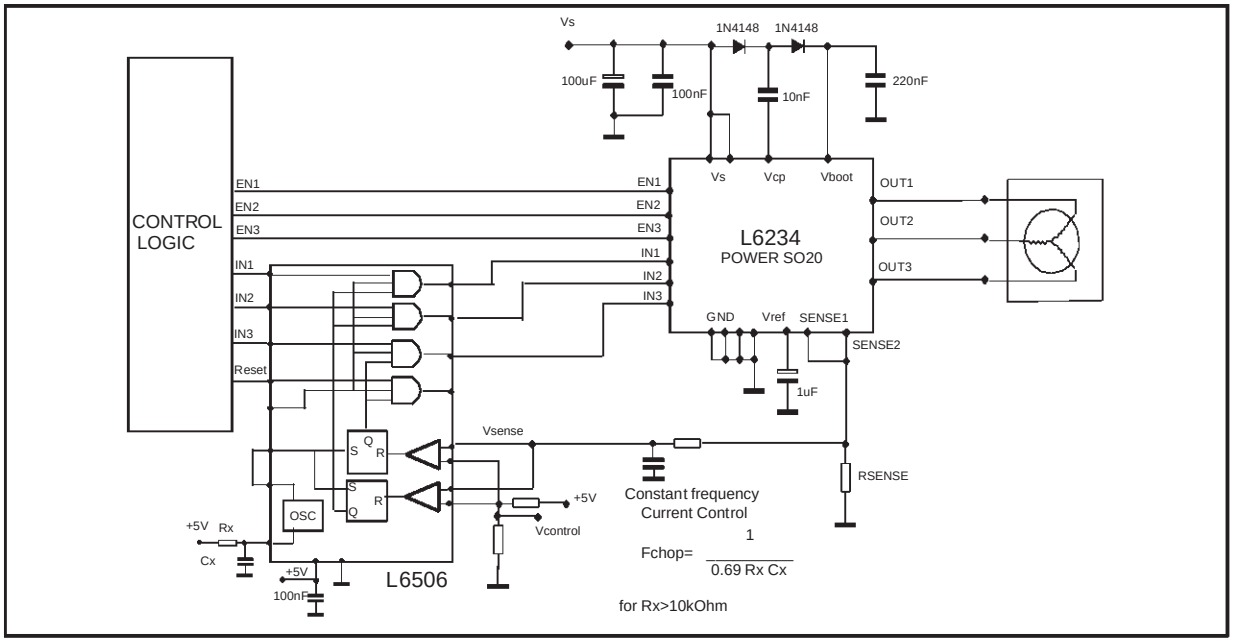
APPLICATION IDEAS.

The L6234 can be used in many different applications. Typical examples are a half bridge driver using one channel and a full bridge driver using two channels. In addition, the bridges can be paralleled to reduce the RDSon and the device dissipation.

The paralleled configuration can also be used to increase output current capability. Channel 1 can be paralleled with Channel 3 or Channel 2 can be paralleled with Channel 3. Channel 1 should not be paralleled with Channel 2 because the sources of their low side DMOSs are connected to the same SENSE1 pin .

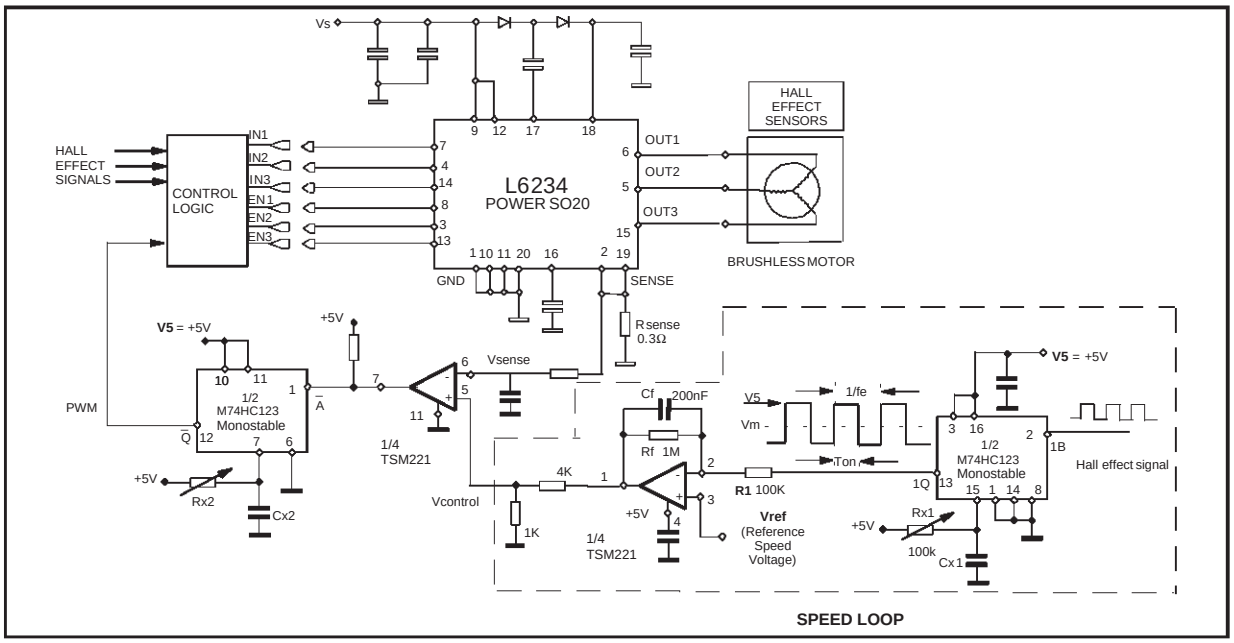
Application ideas for the L6234 follow .

Figure 22. Constant frequency current control



Low Cost Application with Speed and Torque Control Loops.

Figure 23. Complete three phase brushless motor application with speed and torque control.



A low cost solution to obtain a complete three phase brushless motor control application with speed and torque closed control loop is shown in Fig. 23. This simple low cost solution is useful when high dynamic performances and accuracy of the speed loop are not required.

The current regulation limit, which determines the torque , is given by Vcontrol/Rsense. The constant toff of the PWM is fixed by Rx2 and Cx2.

The speed loop is realised using a Hall effect signal, whose frequency is proportional to the motor speed. At each positive transition of the Hall effect sensors the monostable maintains the pulse for a constant time , Ton, with a fixed amplitude, V5. The average value of this signal is proportional to the frequency of the Hall effect signal and the motor speed . An OP-AMP configured as an integrator , filters this signal and compares it with a reference voltage, Vref, which sets the speed . The generated error signal is the control voltage, Vcontrol, of the currrent loop. Therefore the current loop modifies the produced torque in order to regulate the speed at the desired value.

The values of Cf and R2 should be chosen to obtain a nearly ripple free op-amp output, even at low motor speed. This constrain limits the system bandwidth and so limits the response time of the loop.

The regulated speed, for a rotor with n pairs of permanent magnetic poles , is given by :

$$\omega m = \frac{\left(1 + \frac{R1}{R2}\right)}{V5 \cdot Ton \cdot n + \frac{1}{KG}} \cdot Vref \cdot 60 \qquad [RPM]$$

$$\text{with} \qquad KG = \frac{1}{5} \cdot Kt \cdot \frac{1}{Rsense} \cdot \frac{1}{B}$$

in which Kt, expressed in [Nm/A] , is the Motor Torque constant and B, expressed in [Nms], is the Total Viscous Friction.

In most cases KG can be neglected.

The Ton values, given by KCx1Rx1, must be less than the period of the Hall effect electrical signal at the desired motor speed , so Ton must meet the requirement of 1.1 :

$$(1.1)\quad Ton < \frac{60}{n \cdot \omega m}$$

For the motor and the load used in this application, which have the following parameters :

$Jt = 10^{-4}$ [Kg · m^2] (Motor plus Load Inertia Moment); $Kt = 10^{-2}$ [Nm/A] ; $B = 10^{-5}$ [Nms]
n=4 ; R1=100k +/- 10% [kΩ] ; R2=1M ±1[kW] ; Cf=220n [F]

A regulated speed of 6000RPM can be obtained with an accuracy of around +/-3%, considering Ton accuracy of +/-1% , the V5 and Vref mismatch of +/-1% .

If the speed is 6000RPM, there are 100 rotor revolution for second, with n=4, the Hall effect frequency is 400Hz. Therefore Ton has to be lower than 2.5ms (according to equation 1.1).

The phase margin is about 45° and the response time of the speed loop for a speed step variation is around 200ms .

6X6 BRUSHLESS APPLICATION

Figure 24. 6x6 Three Phase Brushlees Application Circuit