QRR9802
QUALITY & RELIABILITY REPORT

July 1997 to June 1998 - EPROM, Flash Memory, EEPROM and NVRAM Products

INTRODUCTION

STMicroelectronics manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; Flash memories in 1.2 to 0.6µ CMOS technology; OTP EPROMs in 0.8 to 0.6µ and EEPROMs in 1.2 to 0.6µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAM: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.7µ HCMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from July 1997 to June 1998. Regular reports are issued each quarter with the last years cumulative results.

Director of
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Quality Control & Reliability

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CONTENT

Table 1. Final Average Outgoing Quality (AOQ)
July 1997 to June 1998

Process	Electrical ppm				Visual ppm			
	3Q97	4Q97	1Q98	2Q98	3Q97	4Q97	1Q98	2Q98
UV EPROM								
CMOS	17	19	20	18	15	11	13	19
NMOS	0	0	0	20	20	0	20	20
OTP EPROM								
CMOS	18	18	20	20	14	11	10	8
FLASH								
CMOS	0	0	2	3	5	10	6	6
NVRAM								
CMOS	0	0	0	0	4	5	3	3
EEPROM								
CMOS	1	2	2	4	4	6	8	8

Table 2. Failure Rate Predictions (Fit)
July 1997 to June 1998

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C ($\times 10^6$)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs ($\times 10^6$)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -35%	4.203	140	0.6	4.0	1,153	0	0.8	1.9
CMOS E6 - DM	3.152	140	0.6	4.0	865	0	1.1	2.7
CMOS E6 -10%	1.844	140	0.6	4.0	506	0	1.8	4.5
OTP EPROM								
CMOS E5 -35%	2.67	140	0.6	4.0	689	0	1.3	3.3
FLASH								
CMOS T5 -20%	5.623	140	0.6	4.0	1,458	0	0.6	1.6
CMOS T6	13.246	140	0.6	4.6	3,948	0	0.2	0.6
EEPROM								
CMOS F4S	3.780	140	0.6	3.0	890	0	1	2.6
CMOS F6SP	1.014	140	0.6	4.6	366	0	2.5	6.3
NVRAM								
CMOS Spectrum	1.744	100	0.7	64	2,232	1	0.9	1.7
HCMOS S3	1.593	100	0.7	64	2,039	1	1	1.9
HCMOS 4DZ	3.225	125	0.7	6.0	1,489	0	0.6	1.5

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	-	-	-	-	685	0	80	0	-	-	-	-
		– 168 hrs	-	-	-	-	560	0	80	0	-	-	-	-
		– 500 hrs	-	-	-	-	560	0	80	0	-	-	-	-
		– 1000 hrs	-	-	-	-	480	0	80	0	-	-	-	-
Retention Bake	1008	250°C,												
		– 48 hrs	-	-	-	-	560	0	80	0	-	-	-	-
		– 168 hrs	-	-	-	-	560	0	80	0	-	-	-	-
		– 500 hrs	-	-	-	-	560	0	80	0	-	-	-	-

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	927	0
		– 168 hrs	80	0
		– 500 hrs	80	0
		– 1000 hrs	80	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	80	0
		– 168 hrs	80	0
		– 500 hrs	80	0

Table 5A. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C1001 (D)		M27C1024 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	4,413	0	3,492	0	539	0	80	0
		– 168 hrs	640	0	720	0	-	-	80	0
		– 500 hrs	640	0	640	0	-	-	80	0
		– 1000 hrs	560	0	560	0	-	-	80	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	640	0	720	0	-	-	80	0
		– 168 hrs	640	0	720	0	-	-	80	0
		– 500 hrs	640	0	640	0	-	-	80	0
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 5B. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (D)		M27C4002 (D)		M27C801 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	1,552	0	397	0	27,963	0
		– 168 hrs	320	0	320	0	320	0
		– 500 hrs	320	0	320	0	320	0
		– 1000 hrs	320	0	320	0	320	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	250°C,						
		– 48 hrs	320	0	320	0	320	0
		– 168 hrs	320	0	320	0	320	0
		– 500 hrs	320	0	320	0	320	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 6. CMOS E6/0.6µm Process (-10% upgrade) UV EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024 (F)		M27C2001 (F)		M27C4002 (F)		M27C801 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	1,660	0	317	0	1,399	0	240	0	6,012	0
		– 168 hrs	960	0	240	0	160	0	240	0	160	0
		– 500 hrs	880	0	240	0	160	0	240	0	80	0
		– 1000 hrs	880	0	160	0	80	0	160	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,										
		– 48 hrs	960	0	240	0	160	0	240	0	160	0
		– 168 hrs	960	0	240	0	160	0	240	0	160	0
		– 500 hrs	880	0	160	0	160	0	240	0	80	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 7. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	2,559	0	23,181	0	16,137	0
		– 168 hrs	480	0	400	0	320	0
		– 500 hrs	480	0	400	0	320	0
		– 1000 hrs	480	0	400	0	320	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	250°C,						
		– 48 hrs	480	0	400	0	320	0
		– 168 hrs	480	0	400	0	320	0
		– 500 hrs	480	0	400	0	320	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal)
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,431 3,381 3,231	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,080	0
Resistance to Solvents	2015	4 Solvent Solutions	240	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	175	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)		M27C1001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 168 hrs	300	0	900	0	360	0	540	0
		– 500 hrs	300	0	840	0	360	0	540	0
		– 1000 hrs	240	0	780	0	300	0	480	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	290	0	780	0	360	0	420	0
		– 500 hrs	290	0	720	0	360	0	360	0
		– 1000 hrs	180	0	660	0	300	0	300	0
		– 2000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 9B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 168 hrs	360	0	420	0
		– 500 hrs	300	0	420	0
		– 1000 hrs	300	0	420	0
		– 2000 hrs	-	-	-	-
Retention Bake	1008	150°C,				
		– 168 hrs	360	0	300	0
		– 500 hrs	300	0	300	0
		– 1000 hrs	240	0	300	0
		– 2000 hrs	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 (D) M87C257 (D)		M27C512 (D)		M27C516 (D)		M27C1001 (D)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	300	0	900	0	360	0	540	0
		– 500 hrs	300	0	780	0	360	0	540	0
		– 1000 hrs	240	0	780	0	300	0	480	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	130	0	355	0	150	0	205	0
		– 96 hrs	130	0	355	0	150	0	205	0
		– 168 hrs	25	0	75	0	100	0	50	0
		– 240 hrs	25	0	-	-	25	0	25	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	300	0	780	0	360	0	540	0
		– 96 hrs	300	0	780	0	360	0	540	0
		– 168 hrs	300	0	780	0	300	0	540	0
		– 240 hrs	300	0	780	0	300	0	480	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	297	0	708	0	300	0	480	0
		– 500 cycles	297	0	708	0	300	0	480	0
		– 1000 cycles	297	0	708	0	300	0	420	0
Solderability										
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 10B)							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 10B)							
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 10B)							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1024 (D)		M27C2001 (D)	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	360	0	360	0
		– 500 hrs	300	0	360	0
		– 1000 hrs	240	0	360	0
		– 2000 hrs	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	125	0	160	0
		– 96 hrs	125	0	160	0
		– 168 hrs	50	0	-	-
		– 240 hrs	25	0	-	-
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	300	0	360	0
		– 96 hrs	300	0	360	0
		– 168 hrs	240	0	360	0
		– 240 hrs	240	0	360	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	240	0	360	0
		– 500 cycles	240	0	360	0
		– 1000 cycles	240	0	360	0
Solderability						
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 805/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 125/0			
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 312/0			

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 11. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 960 900 840 -	 0 0 0 -
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 960 900 840 -	 0 0 0 -

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Package Related Tests July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 960 900 840 -	 0 0 0 -
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 330 330 25 -	 0 0 0 -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 960 960 900 830	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 776 776 720	 0 0 0
Solderability				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	175	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	-	-
Resistance to solvents	2015	4 Solvent Solutions	56	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 13. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	360	0	120	0	120	0
		– 500 hrs	300	0	120	0	120	0
		– 1000 hrs	300	0	120	0	120	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	300	0	120	0	120	0
		– 500 hrs	240	0	120	0	120	0
		– 1000 hrs	240	0	120	0	120	0
		– 2000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800 (F)		M27C160 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	360	0	120	0	120	0
		– 500 hrs	300	0	120	0	120	0
		– 1000 hrs	300	0	120	0	120	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	155	0	50	0	55	0
		– 96 hrs	155	0	50	0	55	0
		– 168 hrs	50	0	25	0	-	-
		– 240 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	360	0	120	0	120	0
		– 96 hrs	360	0	120	0	120	0
		– 168 hrs	300	0	120	0	120	0
		– 240 hrs	300	0	120	0	120	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	300	0	120	0	60	0
		– 500 cycles	300	0	120	0	60	0
		– 1000 cycles	300	0	120	0	60	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 124/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 52/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 60/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	703	0	485	0	101,955	0	41,859	0
		– 168 hrs	540	0	360	0	720	0	720	0
		– 500 hrs	540	0	300	0	720	0	720	0
		– 1000 hrs	540	0	240	0	660	0	660	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	540	0	360	0	480	0	720	0
		– 500 hrs	540	0	300	0	450	0	720	0
		– 1000 hrs	420	0	240	0	450	0	600	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	376	0	60	0
		– 500 hrs	-	-	-	-	376	0	60	0
		– 1000 hrs	-	-	-	-	376	0	-	-
Write/Erase Cycling		1,000 cycles	3,744	0	3,547	0	14,614	0	20,544	0
		10,000 cycles	-	-	-	-	914	0	-	-
Retention Bake	1008	150°C, 36 hrs	3,744	0	3,547	0	14,704	0	20,544	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 16. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	540	0	360	0	780	0	720	0
		– 500 hrs	540	0	300	0	720	0	660	0
		– 1000 hrs	540	0	240	0	720	0	660	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	270	0	140	0	380	0	350	0
		– 96 hrs	270	0	140	0	380	0	350	0
		– 168 hrs	270	0	140	0	380	0	350	0
		– 240 hrs	60	0	25	0	85	0	85	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	540	0	300	0	720	0	720	0
		– 96 hrs	540	0	300	0	720	0	720	0
		– 168 hrs	540	0	240	0	720	0	660	0
		– 240 hrs	540	0	240	0	720	0	600	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	418	0	240	0	684	0	720	0
		– 500 cycles	418	0	180	0	624	0	660	0
		– 1000 cycles	418	0	180	0	564	0	660	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 430/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 105/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 188/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17A. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F210 (C) M28F211 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	33,530	0	117,240	0	18,855	0
		– 168 hrs	540	0	600	0	180	0
		– 500 hrs	540	0	540	0	180	0
		– 1000 hrs	540	0	540	0	120	0
Retention Bake (1)	1008	150°C,						
		– 168 hrs	510	0	600	0	180	0
		– 500 hrs	510	0	600	0	120	0
		– 1000 hrs	480	0	540	0	120	0
Retention Bake	1008	250°C,						
		– 168 hrs	361	0	-	-	180	0
		– 500 hrs	361	0	-	-	180	0
		– 1000 hrs	361	0	-	-	180	0
Write/Erase Cycling		1,000 cycles	5,149	0	11,968	0	2,432	0
		10,000 cycles	319	0	-	-	386	0
		100,000 cycles	-	-	-	-	188	0
		200,000 cycles	-	-	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	5,179	0	11,968	0	2,492	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 17B. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	27,963	0	169,180	0	58,125	0
		– 168 hrs	180	0	1,410	0	480	0
		– 500 hrs	180	0	1,350	0	360	0
		– 1000 hrs	180	0	1,290	0	360	0
Retention Bake (1)	1008	150°C,						
		– 168 hrs	180	0	810	0	360	0
		– 500 hrs	180	0	780	0	300	0
		– 1000 hrs	180	0	780	0	300	0
Retention Bake	1008	250°C,						
		– 168 hrs	51	0	797	0	222	0
		– 500 hrs	51	0	797	0	222	0
		– 1000 hrs	51	0	797	0	222	0
Write/Erase Cycling		1,000 cycles	2,912	0	26,311	0	6,235	0
		10,000 cycles	101	0	1,164	0	735	0
		100,000 cycles	-	-	813	0	432	0
		200,000 cycles	-	-	63	0	-	0
Retention Bake	1008	150°C, 36 hrs	2,912	0	26,491	0	6,235	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 18A. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F201 (B)		M28F211 (C) M28F210 (C) M28F220 (C)		M28F411 (C) M28F410 (C) M28F420 (C)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	540	0	660	0	180	0
		– 500 hrs	540	0	540	0	120	0
		– 1000 hrs	540	0	540	0	120	0
		– 2000 hrs	-	-	-	-	60	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	270	0	315	0	90	0
		– 96 hrs	270	0	315	0	90	0
		– 168 hrs	270	0	315	0	90	0
		– 240 hrs	90	0	30	0	60	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	510	0	660	0	120	0
		– 96 hrs	510	0	660	0	120	0
		– 168 hrs	510	0	540	0	120	0
		– 240 hrs	510	0	540	0	60	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	477	0	645	0	180	0
		– 500 cycles	477	0	525	0	180	0
		– 1000 cycles	477	0	525	0	180	0
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-
Solderability								
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 18B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 18B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 18B. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F200 M29F100		M29F040 (C) M29W040		M29F400 M29W400	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	180	0	1,260	0	480	0
		– 500 hrs	180	0	1,260	0	360	0
		– 1000 hrs	180	0	1,260	0	360	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	90	0	670	0	200	0
		– 96 hrs	90	0	670	0	200	0
		– 168 hrs	90	0	670	0	200	0
		– 240 hrs	-	-	140	0	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	180	0	1,320	0	360	0
		– 96 hrs	180	0	1,320	0	360	0
		– 168 hrs	180	0	1,320	0	360	0
		– 240 hrs	180	0	1,320	0	300	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	120	0	1,306	0	475	0
		– 500 cycles	120	0	1,246	0	352	0
		– 1000 cycles	120	0	1,186	0	352	0
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-
Solderability								
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 540/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 248/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93C06C ST93C46C		ST95010		ST95020	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,						
		– 24 hrs	10,370	0	-	-	-	-
		– 168 hrs	1,370	0	-	-	-	-
		– 500 hrs	1,370	0	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	850	0	-	-	-	-
		– 500 hrs	850	0	-	-	-	-
		– 1000 hrs	850	0	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	200	0	-	-	-	-
		1,000,000 cycles	200	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	200	0	-	-	-	-

Table 20. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93C06C ST93C46C	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	740	0
		– 500 hrs	740	0
		– 1000 hrs	740	0
		– 2000 hrs	-	-
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	500	0
		– 96 hrs	500	0
		– 168 hrs	500	0
		– 240 hrs	500	0
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	550	0
		– 200 cycles	100	0
		–40 to 150°C,		
		– 500 cycles	-	-
		– 1000 cycles	-	-
Soderability				
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)	
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)	
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)	
Resistance to Surface Mount:				
– SO Package			(See cumulative data on Table 24B)	

Table 21A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24C16 ST25C16		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	11,090	0	6,340	0	7,920	0	5,330	0	1,920	0	-	-
		– 168 hrs	1,890	0	1,740	0	920	0	530	0	320	0	-	-
		– 500 hrs	1,890	0	1,740	0	920	0	530	0	320	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	850	0	700	0	500	0	250	0	510	0	-	-
		– 500 hrs	850	0	700	0	500	0	250	0	510	0	-	-
		– 1000 hrs	850	0	700	0	500	0	250	0	510	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	300	0	200	0	100	0	100	0	-	-	-	-
		1,000,000 cycles	300	0	200	0	100	0	100	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	300	0	200	0	100	0	100	0	-	-	-	-

Table 21B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M93C06		M93C46		M93C56		M93C66		M28C64D M28C64	
			Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	-	-	480	0	1,920	0	480	0	480	0	160	0
		– 168 hrs	-	-	80	0	320	0	80	0	80	0	160	0
		– 500 hrs	-	-	80	0	320	0	80	0	80	0	160	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	-	-	50	0	150	0	50	0	-	-	3,733 (1)	0
		– 500 hrs	-	-	50	0	150	0	50	0	-	-	3,733 (1)	0
		– 1000 hrs	-	-	50	0	150	0	50	0	-	-	3,733 (1)	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		1,000,000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Note: 1. 3,483 samples have performed the same test at 250°C.

Table 22A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	900	0	1,900	0	280	0	380	0
		– 500 hrs	900	0	1,900	0	280	0	380	0
		– 1000 hrs	900	0	1,900	0	280	0	380	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	900	0	1,300	0	450	0	500	0
		– 96 hrs	900	0	1,300	0	450	0	500	0
		– 168 hrs	900	0	1,300	0	450	0	500	0
		– 240 hrs	850	0	1,300	0	250	0	500	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	1,200	0	1,600	0	500	0	800	0
		– 200 cycles	350	0	400	0	100	0	350	0
		– 1000 cycles	-	-	-	-	-	-	-	-
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)							
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 24B)							

Table 22B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C16 ST25C16		M24C16		M93C46	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	900	0	-	-	120	0
		– 500 hrs	900	0	-	-	120	0
		– 1000 hrs	900	0	-	-	120	0
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	1,370	0	-	-	250	0
		– 96 hrs	1,370	0	-	-	250	0
		– 168 hrs	1,370	0	-	-	250	0
		– 240 hrs	960	0	-	-	250	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	1,010	0	-	-	400	0
		– 200 cycles	360	0	-	-	200	0
		– 1000 cycles	360	0	-	-	-	-
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)					
Resistance to Surface Mount:								
– SO Package			(See cumulative data on Table 24B)					

Table 22C. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M93C56		M93C66		M28C64 M28C64D	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	40	0	-	-	120	0
		– 500 hrs	40	0	-	-	80	0
		– 1000 hrs	40	0	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	50	0	50	0	2,590	0
		– 96 hrs	50	0	50	0	2,590	0
		– 168 hrs	50	0	50	0	2,590	0
		– 240 hrs	50	0	50	0	2,590	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	100	0	250	0	2,000	0
		– 200 cycles	50	0	50	0	150	0
		– 1000 cycles	-	-	-	-	-	-
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)					
– PLCC Package			(See cumulative data on Table 24B)					
– TSOP Package			(See cumulative data on Table 24B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)					
Resistance to Surface Mount:								
– SO Package			(See cumulative data on Table 24B)					
– TSOP Package			(See cumulative data on Table 24B)					
– PLCC Package			(See cumulative data on Table 24B)					

Table 23. CMOS F6 0,6µm Process EEPROM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C02		M24C04		M24C08		M24C16		M24C32		M24C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	2,480	0	480	0	480	0	3,840	0	1,360	0	960	0
		– 168 hrs	2,480	0	480	0	80	0	240	0	160	0	160	0
		– 500 hrs	80	0	80	0	80	0	240	0	160	0	160	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	-	-	50	0	50	0	100	0	50	0	50	0
		– 500 hrs	-	-	50	0	50	0	100	0	50	0	50	0
		– 1000 hrs	-	-	50	0	50	0	100	0	50	0	50	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		1,000,000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Table 24A. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C02		M24C04		M24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	-	-	120	0	120	0
		– 500 hrs	-	-	120	0	120	0
		– 1000 hrs	-	-	120	0	120	0
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	50	0	200	0	200	0
		– 96 hrs	50	0	200	0	200	0
		– 168 hrs	50	0	200	0	200	0
		– 240 hrs	50	0	200	0	150	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	100	0	400	0	300	0
		– 200 cycles	50	0	200	0	150	0
			-	-	-	-	-	-
		–40 to 150°C,						
		– 500 cycles						
		– 1000 cycles	-	-	-	-	-	-
			-	-	-	-	-	-
Soderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 24B)					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 24B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 24B)					
Resistance to Surface Mount:								
– SO Package			(See cumulative data on Table 24B)					

Table 24B. CMOS F6 0,6µm Process EEPROM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M24C16		M24C32		M24C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	40	0	-	-	-	-
		– 500 hrs	40	0	-	-	-	-
		– 1000 hrs	40	0	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	100	0	-	-	100	0
		– 96 hrs	100	0	-	-	100	0
		– 168 hrs	100	0	-	-	100	0
		– 240 hrs	100	0	-	-	100	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	100	0	-	-	200	0
		– 200 cycles	50	0	-	-	100	0
		– 1000 cycles			-	-		
		–40 to 150°C,	-	-			-	-
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles			-	-		
Solderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 50/0					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 150/0					
– PLCC Package			Cumulative Sample/Fail = 175/0					
– TSOP Package			Cumulative Sample/Fail = 845/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 192/0					
Resistance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 10,320/0					
– TSOP Package			Cumulative Sample/Fail = 2,400/0					
– PLCC Package			Cumulative Sample/Fail = 880/0					

Table 25. CMOS SPECTRUM/2.0µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,951 1,926 1,554	 0 1(1) 0

Note: 1. Failure: particle induced gate oxide break down in p-channel of memory cell.

Table 26. CMOS SPECTRUM/2.0µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 768 762 596	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 240 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	72	0

Table 27. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,967 1,732 1,376	 1(1) 0 0

Note: 1. Failure: mechanical domage on metal 2 write signal.

Table 28. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 921 844 843	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 560 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	76	0

Table 29. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	152	0	2,686	0
		– 500 hrs	152	0	2,498	0
		– 1000 hrs	-	-	2,163	0
		– 2000 hrs	-	-	-	-

Table 30. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	-	-	539	0
		– 500 hrs	-	-	456	0
		– 1000 hrs	-	-	453	0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 96 hrs	-	-	-	-
		– 168 hrs	-	-	-	-
		– 240 hrs	-	-	-	-
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	80	0	951	0
		– 500 cycles	80	0	871	0
		– 1000 cycles	80	0	789	0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 68/0			

Table 31. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 787 787 787 -	 0 0 0 -

Table 32. HCMOS 4DZ/0.7µm Process ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T37Y (5V)	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 66 66 -	 0 0 -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 179 179 179	 0 0 0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 64/0	

Table 33. ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	45	0	85	0
		– 500 hrs	45	0	85	0
		– 1000 hrs	45	0	84	0
		– 2000 hrs	-	-	-	-

Table 34. ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests
July 1997 to June 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	21	-	41	0
		– 500 hrs	21	-	41	0
		– 1000 hrs	-	-	41	0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 96 hrs	21	0	-	-
		– 168 hrs	21	0	-	-
		– 240 hrs	-	-	-	-
Temperature Cycling	1010	–40 to 100°C,				
		– 100 cycles	47	0	-	-
		– 500 cycles	47	0	-	-
		– 1000 cycles	47	0	-	-
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-			

Table 35. Statistical Process Control: CMOS E5/0.6µm Process (–35% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.85	1.98	2.2	2.66
Silicon Nitride Thickness	1.59	1.51	1.7	1.85
Field Oxide Thickness	2.24	2.37	2.61	3.47
Gate Oxide Thickness	1.34	1.74	2.06	2.20
Interpoly Oxide Thickness	1.77	2.28	2.4	2.58
Intermediate Dielectric Thickness	1.75	1.97	1.71	1.7
Polysilicon 1 Thickness	1.55	1.63	1.91	2.72
Active Area Critical Dimensions	2.17	1.43	2.51	1.75
Policide Critical Dimensions	1.79	1.59	1.6	2.00

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	1.38	1.44	1.74	3.94
VT P-Channel Square Tr.	1.72	1.84	2.56	2.17
VT Natural Square Tr.	3.12	2.75	4.74	3.92
VT Memory Cell	1.41	1.52	2.22	1.9
I_{DON} N-Channel	2.61	2.48	3.1	3.48
N+ Active Area Contact Chain	6.60	7.37	9.67	5.85
AL-W Silicide Contact Chain Resistance	2.98	3.38	5.99	1.92

Table 36. Statistical Process Control: CMOS E6DM/0.6µm Process UV EPROM and OTP EPROM, Phoenix - USA PF1 Diffusion Line

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	1.71	1.97	2.02
Silicon Nitride Thickness	-	1.46	1.63	1.78
Field Oxide Thickness	-	2.49	2.86	5.20
Gate Oxide Thickness	-	2.69	2.18	2.76
Interpoly Oxide Thickness	-	1.44	1.35	1.34
Intermediate Dielectric Thickness	-	1.35	1.34	1.34
Polysilicon 1 Thickness	-	6.21	4.56	2.90
Active Area Critical Dimensions		2.24	2.34	2.06
Policide Critical Dimensions	-	2.35	2.64	1.37

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	-	3.26	3.09	3.08
VT P-Channel Square Tr.	-	1.64	1.67	1.60
VT Natural Square Tr.	-	3.99	3.92	4.55
VT Memory Cell	-	1.36	1.61	1.15 (1)
I_{DON} N-Channel	-	1.44	1.73	1.14 (1)
N+ Active Area Contact Chain	-	5.02	4.61	4.77
AL-W Silicide Contact Chain Resistance	-	1.33	1.59	1.35

Note: 1. Photo spec. retargeted at poly gate.

Table 37. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	-	-	2.27
Silicon Nitride Thickness	-	-	-	1.33
Field Oxide Thickness	-	-	-	2.03
Gate Oxide Thickness	-	-	-	2.20
Interpoly Oxide Thickness	-	-	-	2.58
Intermediate Dielectric Thickness	-	-	-	1.72
Polysilicon 1 Thickness	-	-	-	2.72
Active Area Critical Dimensions	-	-	-	2.43
Policide Critical Dimensions	-	-	-	2.07

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	-	-	-	2.33
VT P-Channel 10 x 10µm	-	-	-	2.53
VT Natural 10 x 10µm	-	-	-	1.35
VT Memory Cell 0.65 x 0.65µm	-	-	-	1.33
I_{DON} N-Channel 10 x 10µm	-	-	-	2.01
N+ Active Area Contact Chain	-	-	-	5.6
AL-W Silicide Contact Chain Resistance	-	-	-	2.22

Table 38. Statistical Process Control: CMOS E6/0.6µm Process (–10% upgrade) UV EPROM and OTP EPROM, Catania - Italy M5 Diffusion Line

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	-	-	1.38
Silicon Nitride Thickness	-	-	-	1.33
Field Oxide Thickness	-	-	-	2.59
Gate Oxide Thickness	-	-	-	1.81
Interpoly Oxide Thickness	-	-	-	1.57
N-Well Oxidation	-	-	-	3.74
Polysilicon 1 Thickness	-	-	-	1.51
Active Area Critical Dimensions	-	-	-	2.4
Policide Critical Dimensions	-	-	-	1.44

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	-	-	-	4.12
VT P-Channel Square Tr.	-	-	-	2.76
VT Natural Square Tr.	-	-	-	4.34
VT Memory Cell	-	-	-	1.33
I_{DON} N-Channel	-	-	-	2.72
N+ Active Area Contact Chain	-	-	-	5.51
AL-W Silicide Contact Chain Resistance	-	-	-	2.22

Table 39. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.33	2.25	2.15	2.44
Polysilicon 1 Thickness	2.89	2.65	2.96	3.64
Gate Oxide Thickness	1.28 (1)	1.87	1.82	2.61
Tunnel Oxide Thickness	2.23	2.35	2.23	2.79
ONO Bottom Oxide Thickness	1.50	1.44	2.22	2.06
ONO Nitride Thickness	1.66	1.66	1.92	1.34
ONO Top Oxide Thickness	3.22	2.41	2.67	2.00
Active Area Critical Dimensions	1.50	1.54	2.96	1.73
Polysilicon 2 Critical Dimensions	1.92	1.63	1.69	2.39

Note: 1. Exhaust problems (progressive obstruction) solved in week 45 by rebuilding part of the exaust, to avoid this problems detectors have been installed.

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
VT N-Channel 25 x 25 µm	2.06	2.42	2.77	2.71
VT P-Channel 25 x 25 µm	1.75	1.54	1.69	2.17
BV N-Channel 25 x 0.8 µm	4.75	3.23	1.63	3.36
BV P-Channel 25 x 0.9 µm	3.00	3.87	3.68	4.11
VT Memory Cell 0.8 x 0.8 µm	1.78	1.87	1.36	3.08
I_{DON} N-Channel 25 x 0.8 µm	2.23	2.00	2.02	1.76
Al+N+ Contact Chain	3.93	3.86	4.58	5.16
AL-W Silicide Contact Chain Resistance	4.01	4.07	1.81	5.76

Table 40. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	2Q97	3Q97	4Q97/1Q98 (2)	2Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.67	1.60	-	1.92
Polysilicon 1 Thickness (1)	1.25	1.14	-	1.33
Gate Oxide Thickness	1.78	1.55	-	2.77
Tunnel Oxide Thickness	1.65	1.86	-	1.76
ONO Bottom Oxide hickness	1.39	1.44	-	1.37
ONO Nitride Thickness	1.60	1.52	-	1.84
ONO Top Oxide Thickness	1.57	2.02	-	1.49
Active Area Critical Dimensions	1.38	1.34	-	1.03 (3)
Polysilicon 2 Critical Dimensions	1.36	1.33	-	0.95 (3)

Note: 1. The furnace temperature control system alignment is going to be implemented.
2. No production.
3. New resist under evaluation.

Key Electrical Parameters	2Q97	3Q97	4Q97/1Q98 (1)	2Q98
	CPK	CPK	CPK	CPK
VT N-Channel 25 x 25 µm	1.52	1.36	-	1.83
VT P-Channel 25 x 25 µm	1.48	1.42	-	1.57
BV N-Channel 25 x 0.8 µm	1.39	1.82	-	1.37
BV P-Channel 25 x 0.9 µm	1.84	2.48	-	3.25
VT Memory Cell 0.8 x 0.8 µm	1.73	1.66	-	2.53
I_{DON} N-Channel 25 x 0.8 µm	1.49	2.12	-	2.04
Al+N+ Contact Chain	1.48	3.12	-	2.53
Al-W Silicide Contact Chain Resistance	2.31	3.01	-	2.95

Note: 1. No production.

Table 41A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.42	1.59	1.77	1.92
First Poly Thickness	1.19 (1)	1.46	1.04 (2)	1.33
Gate Oxide HV Thickness	1.83	1.69	2.48	2.77
Tunnel Oxide Thickness	1.64	2.36	1.92	1.76
Gate Oxide LV Thickness	1.37	1.49	1.94	1.94
ONO Bottom Oxide Thickness	1.45	1.15 (3)	1.33	1.37
ONO Nitride Thickness	1.49	1.35	1.88	1.84
ONO Top Oxide Thickness	1.68	1.78	1.90	1.49
Active Area CD	1.49	1.66	2.15	0.97 (4)
Second Poly CD	1.43	1.38	1.35	0.99 (5)

Note: 1. The furnace temperature control system alignment is going to be implemented.
2. The low value of CPK is due to low run uniformity on two furnaces. A modification of hardware has been done on the furnace with good results. At the end of this month the same modification will be done also on the other furnace.
3. The recipe has been transferred from tubes with atmoscan to tubes with cantilever. We had a deterioration of thickness uniformity along the load. Tests have been completed to evaluate the possibility to transfer the recipe in a vertical tube allowing much better thickness control. This evaluation was completed and the process has been loaded on the Vtube starting from the end of January. We are confident to recover this value within the 1Q 98.
4 New resist under evaluation.
5 Low CPK value due to new target.

Table 41B. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	2.20	2.82	3.42	3.34
LV-PCh LVS (10 x 0.9) BV	2.55	2.55	3.10	2.27
LV-PCh LVS (10 x 0.9) Saturation Current	1.94	1.85	1.68	1.34
LV-PCh SQ. VTh	1.39	1.54	1.68	2.65
HV-NCh SQ. VTh	1.61	1.66	1.82	1.88
HV-NCh (10 x 1.2) LVS Saturation Current	2.45	2.26	2.38	3.34
HV-PCh (10 x 1.3) BV	2.18	3.18	2.61	2.27
HV-PCh (10 x 1.3) Saturation Current	1.90	2.51	2.02	3.29
HV-PCh SQ. VTh	1.37	1.20 (1)	1.33	1.59
UV Erased Cell VTh	1.35	1.43	1.64	1.36
N+ Contact Chain	2.00	1.84	1.67	2.54
Silicide Contact Chain	2.32	1.96	2.08	2.36
LV-NCh (10 x 0.8) BV	2.18	5.31	3.28	3.63

Note: 1. The problem is correlated with a tail of transistor dose implant that pass through the Poly 1. We have already implemented a Poly implant energy modification, but this change is not sufficient to solve the problem. A trial is going to be issued to evaluate the change of Poly 1 thickness.

Table 42A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Field Oxide Thickness	-	1.91	1.85	2.19
First Poly Thickness	-	1.51	1.49	1.78
Gate Oxide HV Thickness	-	1.21 (1)	1.34	(*)
Tunnel Oxide Thickness	-	1.80	1.84	1.95
Gate Oxide LV Thickness	-	1.36	1.33	1.39
ONO Bottom Oxide Thickness	-	1.54	1.33	1.33
ONO Nitride Thickness	-	2.09	1.78	1.63
ONO Top Oxide Thickness	-	2.05	2.3	1.89
Active Area CD	-	1.33	1.79	1.57
Second Poly CD	-	1.50	1.47	1.92

Note: 1. Process alignment is running.
(*) No production during 2Q98.

Table 42B. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	-	2.54	5.77	2.45
LV-PCh LVS (10 x 0.9) BV	-	1.35	2.61	2.3
LV-PCh LVS (10 x 0.9) Saturation Current	-	2.00	1.67	1.89
LV-PCh SQ. VTh	-	1.53	1.78	1.73
HV-NCh (10 x 1.2) LVS BV	-	1.49	1.57	(*)
HV-NCh SQ. VTh	-	1.45	0.98 (1)	(*)
HV-NCh (10 x 1.2) LVS Saturation Current	-	2.35	4.15	(*)
HV-PCh (10 x 1.3) BV	-	1.62	2.31	(*)
HV-PCh (10 x 1.3) Saturation Current	-	1.73	4.38	(*)
HV-PCh SQ. VTh	-	1.38	1.44	(*)
UV Erased Cell VTh	-	1.55	1.68	1.65
N+ Contact Chain	-	3.84	3.84	4.58
Silicide Contact Chain	-	1.36	0.92 (2)	1.38
LV-NCh (10 x 0.8) BV	-	2.32	2.27	3.05

Note: 1. Low CPK due to ox tunnel equipment, now replaced.
2 Low CPK due to one w deposition chamber equipment adjustment in progress.
(*) No production during 2Q98.

Table 43. Statistical Process Control: CMOS F6 0.6µm Process EEPROM Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	-	-	-	2.27
Silicon Nitride Thickness	-	-	-	1.37
Field Oxide Thickness	-	-	-	2.44
Gate Oxide 1 Thickness	-	-	-	2.20
Gate Oxide 2 Thickness	-	-	-	1.90
Tunnel Oxide Thickness	-	-	-	3.24
Dialectric Thickness	-	-	-	1.53
Active Area Critical Dimensions	-	-	-	1.51
Policide Critical Dimensions	-	-	-	1.77
Poly Front Deposition Thickness	-	-	-	2.08
Contacts Critical Dimension	-	-	-	1.62

Key Electrical Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
VT N-Channel 10 x 10µm	-	-	-	2.35
VT P-Channel 10 x 10µm	-	-	-	2.61
VT Natural 10 x 10µm	-	-	-	3.18
BV N-Channel 10 x 10µm	-	-	-	2.44
BV P-Channel 10 x 10µm	-	-	-	1.33
EBD-LVN	-	-	-	5.37
N+ Active Area Contact Chain	-	-	-	2.56
EBD-TUN	-	-	-	2.73

Table 44. Statistical Process Control: UV EPROM Ceramic Frit-Seal Package Assembly Line, Singapore

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	37.14	40.18	16.11	26.2
Stud Pull	1.71	1.40	1.67	1.57
Bond Strength (W.B.)	5.29	5.50	5.67	5.58
SN Thickness (Tin Plate)	1.48	1.39	1.71	1.77

Table 45. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.13	2.24	1.78	2.38
Ball Shear (W.B.)	1.89	2.07	2.00	2.65
Bond Strength (W.B.)	1.57	1.85	1.88	2.76
Coplanarity	3.55	2.53	2.83	4.47
Plating Thickness	2.00	2.17	2.24	1.60

Table 46. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	3Q97	4Q97	1Q98	2Q98
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	4.18	3.30	3.22	3.37
Ball Shear (W.B.)	2.05	2.09	2.13	2.21
Bond Strength (W.B.)	1.62	1.52	1.49	2.10
Plating Thickness	3.56	2.85	2.14	1.90

If you have any questions or suggestion concerning the matters raised in this document please send them to the following electronic mail address:

ask.memory@st.com (for general enquiries)

Please remember to include your name, company, location, telephone number and fax number