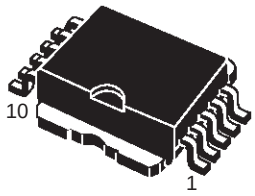
VN610SP

SINGLE CHANNEL HIGH SIDE SOLID STATE RELAY

PRELIMINARY DATA

TYPE	$R_{DS(on)}$	I_{OUT}	V_{CC}
VN610SP	10mΩ	45A	36 V

- OUTPUT CURRENT: 45 A
- CMOS COMPATIBLE INPUT
- PROPORTIONAL LOAD CURRENT SENSE
- UNDERVOLTAGE AND OVERVOLTAGE SHUT-DOWN
- OVERVOLTAGE CLAMP
- THERMAL SHUT DOWN
- CURRENT LIMITATION
- VERY LOW STAND-BY POWER DISSIPATION
- PROTECTION AGAINST:
  LOSS OF GROUND AND LOSS OF V_{CC}
- REVERSE BATTERY PROTECTION (*)

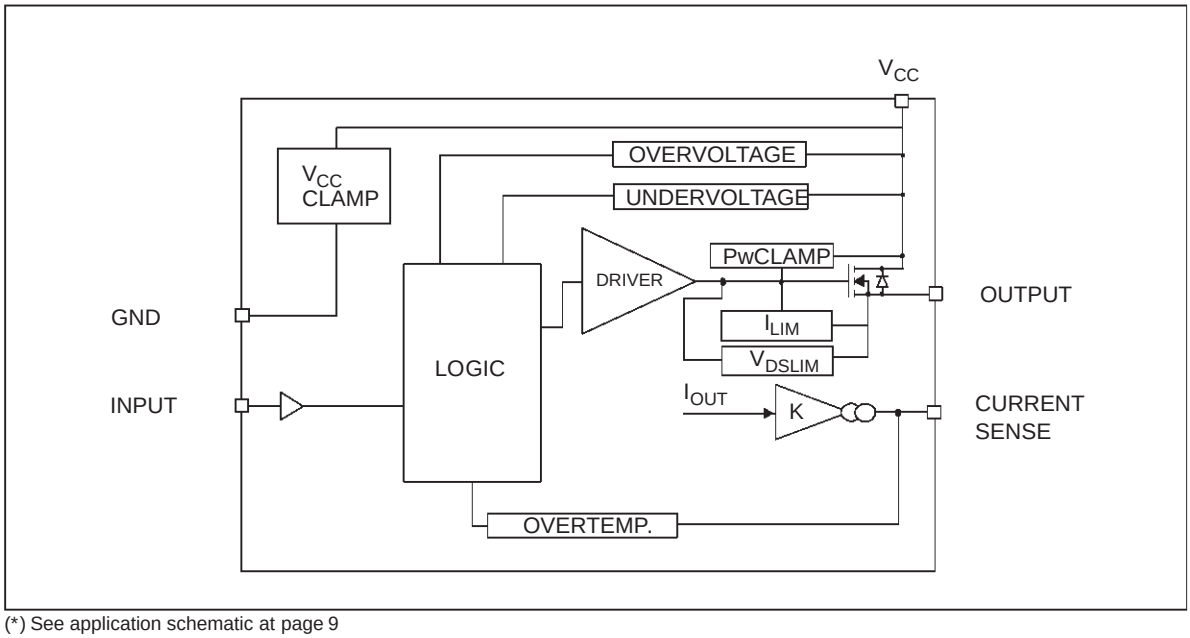


PowerSO-10™

DESCRIPTION

The VN610SP is a monolithic device made using STMicroelectronics VIPower M0-3 technology. It is intended for driving resistive or inductive loads with one side connected to ground. Active V_{CC} pin voltage clamp protects the device against low energy spikes (see ISO7637 transient compatibility table). This device integrates an analog current sense which delivers a current proportional to the load current (according to a known ratio). Active current limitation combined with thermal shut-down and automatic restart protect the device against overload. Device automatically turns off in case of ground pin disconnection.

BLOCK DIAGRAM

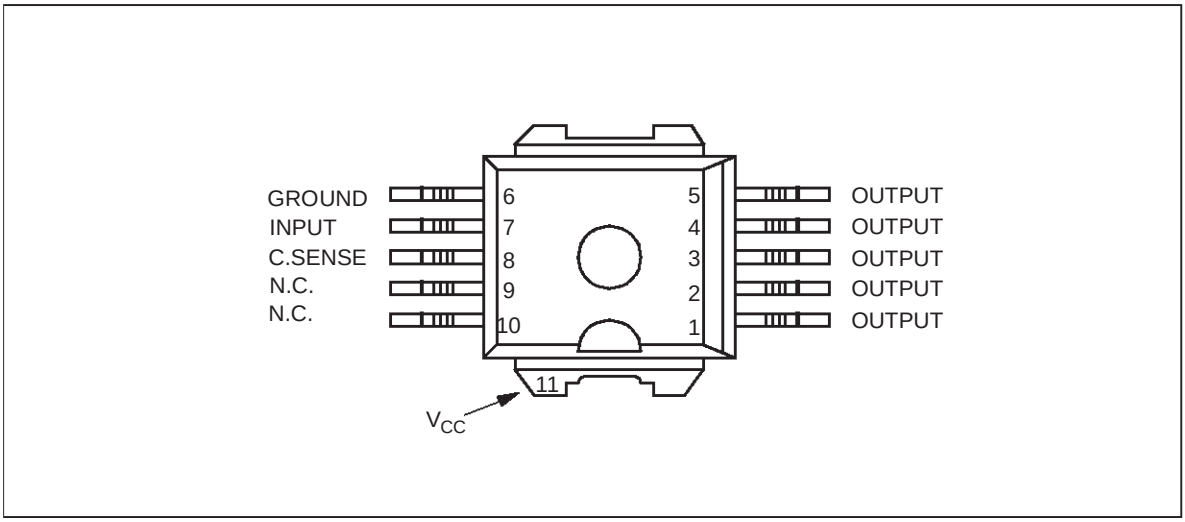


(*) See application schematic at page 9

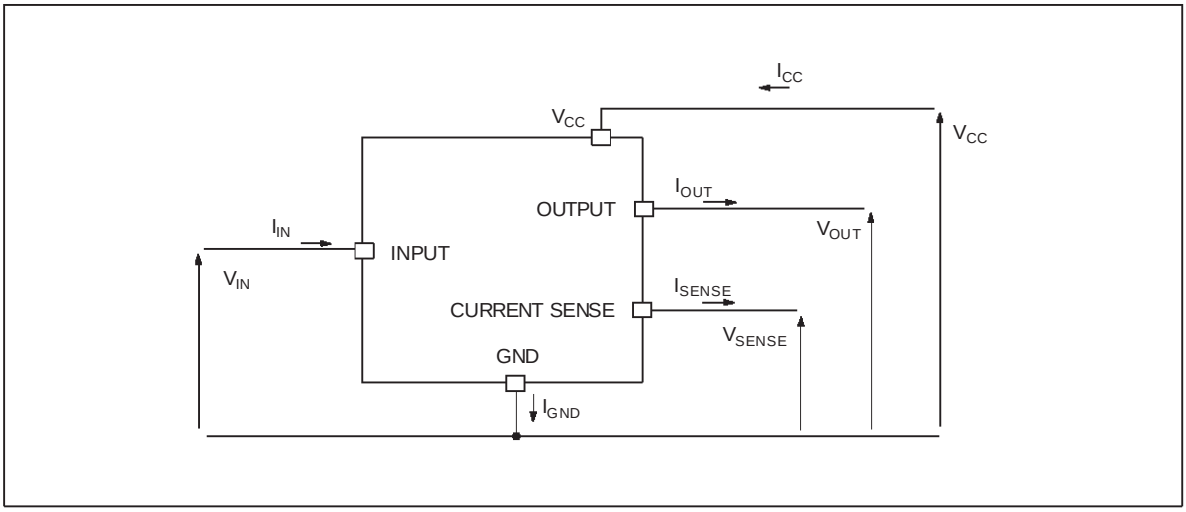
ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	-0.3	V
$-I_{GND}$	DC reverse ground pin current	-200	mA
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	-50	A
I_{IN}	DC input current	+/- 10	mA
V_{CSENSE}	Current sense maximum voltage	-3 +15	V V
V_{ESD}	Electrostatic discharge (R=1.5kΩ; C=100pF)	2000	V
P_{TOT}	Power dissipation at $T_C \leq 25°C$	125	W
T_j	Junction operating temperature	Internally limited	°C
T_c	Case operating temperature	-40 to 150	°C
T_{STG}	Storage temperature	-55 to 150	°C

CONNECTION DIAGRAM (TOP VIEW)



CURRENT AND VOLTAGE CONVENTIONS



THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case	(MAX)	1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	(MAX)	51 (*)	°C/W

(*) When mounted on a standard single-sided FR-4 board with 50mm^2 of Cu (at least 35µm thick).

ELECTRICAL CHARACTERISTICS (8V<V_{CC}<36V; -40°C<T_j<150°C; unless otherwise specified)

POWER

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Operating supply voltage		5.5	13	36	V
V_{USD}	Undervoltage shutdown		3	4	5.5	V
V_{OV}	Overvoltage shutdown	(See Note 1)	36	42	48	V
R_{ON}	On state resistance	I_{OUT}=15A; T_j=25°C			10	mΩ
		I_{OUT}=15A; T_j=150°C			20	mΩ
		I_{OUT}=9A; V_{CC}=6V			35	mΩ
V_{clamp}	Clamp Voltage	I_{CC}=20 mA (see note 1)	41	48	55	V
I_S	Supply current	Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V		10	25	µA
		Off State; V_{CC}=13V; V_{IN}=V_{OUT}=0V; T_j=25°C		10	20	µA
		On State; V_{CC}=13V; V_{IN}=5V; I_{OUT}=0A R_{SENSE}=3.9K			5	mA
$I_{L(off)}$	Off state output current	V_{IN}=V_{OUT}=0V	0		50	µA

Note 1: V_{clamp} and V_{OV} are correlated. Typical difference is 5V.

SWITCHING (V_{CC}=13V)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-on delay time	R_L=0.87Ω		50		µs
$t_{d(off)}$	Turn-on delay time	R_L=0.87Ω		50		µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L=0.87Ω		0.3		V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L=0.87Ω		0.3		V/µs
W_{ON}	Switching losses energy at turn-on	R_L=2.6Ω		1.0		mJ
W_{OFF}	Switching losses energy at turn-off	R_L=2.6Ω		0.5		mJ

PROTECTIONS

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{lim}	DC Short circuit current	V_{CC}=13V	45	75	120	A
		5.5V<V_{CC}<36V			120	A
T_{TSD}	Thermal shutdown temperature		150	175	200	°C
T_R	Thermal reset temperature		135			°C
T_{HYST}	Thermal hysteresis		7	15		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT}=2A; V_{IN}=0; L=6mH	V_{CC}-41	V_{CC}-48	V_{CC}-55	V
V_{ON}	Output voltage drop limitation	I_{OUT}=1.5A T_j= -40°C...+150°C		50		mV

ELECTRICAL CHARACTERISTICS (continued)

CURRENT SENSE ($9V \leq V_{CC} \leq 16V$) (See Fig.1)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
K_1	I_{OUT}/I_{SENSE}	I_{OUT}=1.5A; V_{SENSE}=0.5V; T_j= -40°C...150°C	3300	4400	6000	
dK_1/K_1	Current Sense Ratio Drift	I_{OUT}=1.5A; V_{SENSE}=0.5V; T_j= -40°C...150°C	-10		+10	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT}=15A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	6000 5750	
dK_2/K_2	Current Sense Ratio Drift	I_{OUT}=15A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	-6		+6	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT}=45A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	4200 4400	4900 4900	5500 5250	
dK_3/K_3	Current Sense Ratio Drift	I_{OUT}=45A; V_{SENSE}=4V; T_j=-40°C T_j=25°C...150°C	-6		+6	%
I_{SENSE0}	Analog sense current	Vcc=6...16V; I_{OUT}=0A; V_{SENSE}=0V; Tj=-40°C...150°C Off State; V_{IN}=0V On State; V_{IN}=5V	 0 0		 5 10	 µA µA
V_{SENSE}	Max analog sense output voltage	V_{CC}=5.5V; I_{OUT} =7.5A; R_{SENSE}=10KΩ V_{CC} >8V; I_{OUT}=15A; R_{SENSE}=10KΩ	3.5 5			V V
V_{SENSEH}	Analog sense output voltage in overtemperature condition	V_{CC}=13V; R_{SENSE}=3.9KΩ		5.5		V
R_{SENSEH}	Analog sense output impedance in overtemperature condition	Vcc=13V		400		Ω
t_{DSENSE}	Delay Response time	V_{SENSE}<4V, R_{SENSE}=2.7KΩ I_{SENSE}=90% of $I_{SENSE\ max}$			500	µs

LOGIC INPUT

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input low level voltage				1.25	V
I_{IL}	Low level input current	V_{IN}=1.25V	1			µA
V_{IH}	Input high level voltage		3.25			V
I_{IH}	High level input current	V_{IN}=3.25V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.5			V
V_{ICL}	Input clamp voltage	I_{IN}=1mA I_{IN}=-1mA	6	6.8 -0.7	8	V V

TRUTH TABLE

CONDITIONS	INPUT	OUTPUT	SENSE
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overvoltage	L H	L L	0 0
Short circuit to GND	L H	L L	0 0
Short circuit to V_{CC}	L H	H H	0 < Nominal
Negative output voltage clamp	L	L	0

ELECTRICAL TRANSIENT REQUIREMENTS

ISO T/R 7637/1 Test Pulse	TEST LEVELS				
	I	II	III	IV	Delays and Impedance
1	-25 V	-50 V	-75 V	-100 V	2 ms 10 Ω
2	+25 V	+50 V	+75 V	+100 V	0.2 ms 10 Ω
3a	-25 V	-50 V	-100 V	-150 V	0.1 µs 50 Ω
3b	+25 V	+50 V	+75 V	+100 V	0.1 µs 50 Ω
4	-4 V	-5 V	-6 V	-7 V	100 ms, 0.01 Ω
5	+26.5 V	+46.5 V	+66.5 V	+86.5 V	400 ms, 2 Ω

ISO T/R 7637/1 Test Pulse	TEST LEVELS RESULTS			
	I	II	III	IV
1	C	C	C	C
2	C	C	C	C
3a	C	C	C	C
3b	C	C	C	C
4	C	C	C	C
5	C	E	E	E

CLASS	CONTENTS
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device is not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

SWITCHING CHARACTERISTICS

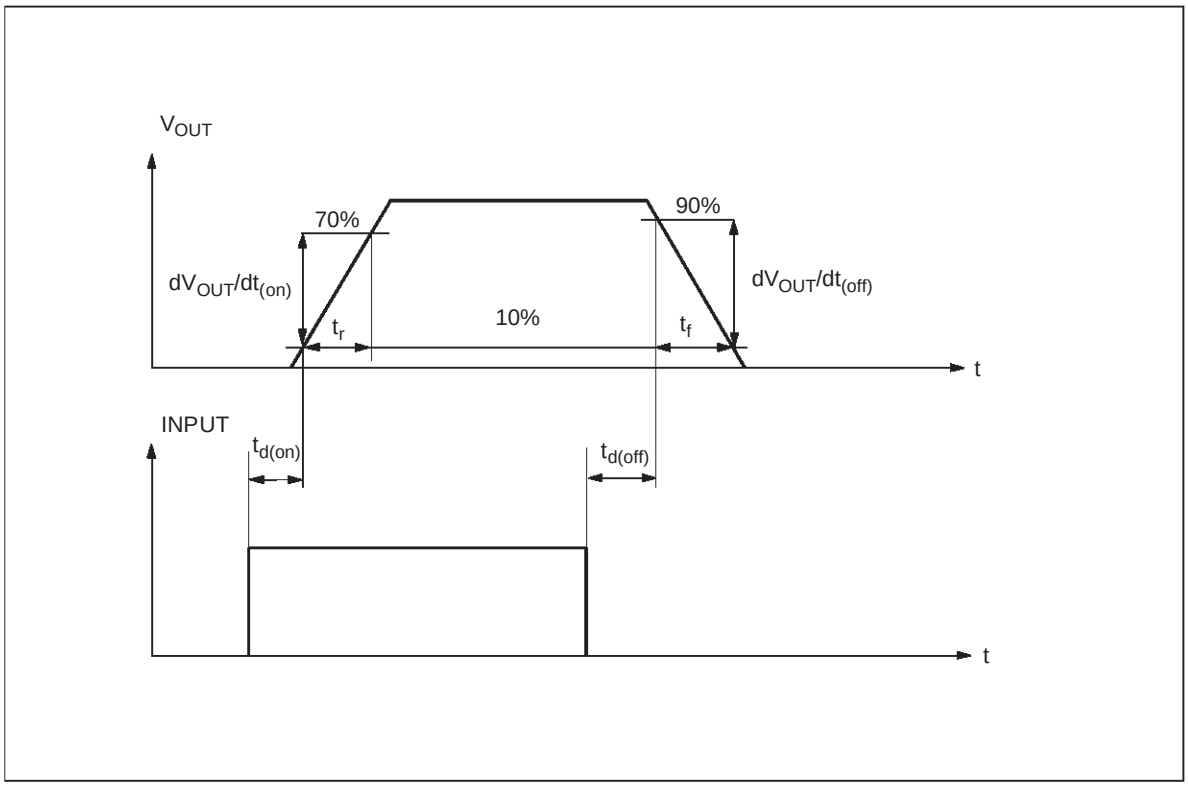


Fig 1: I_{OUT}/I_{SENSE} versus I_{OUT}

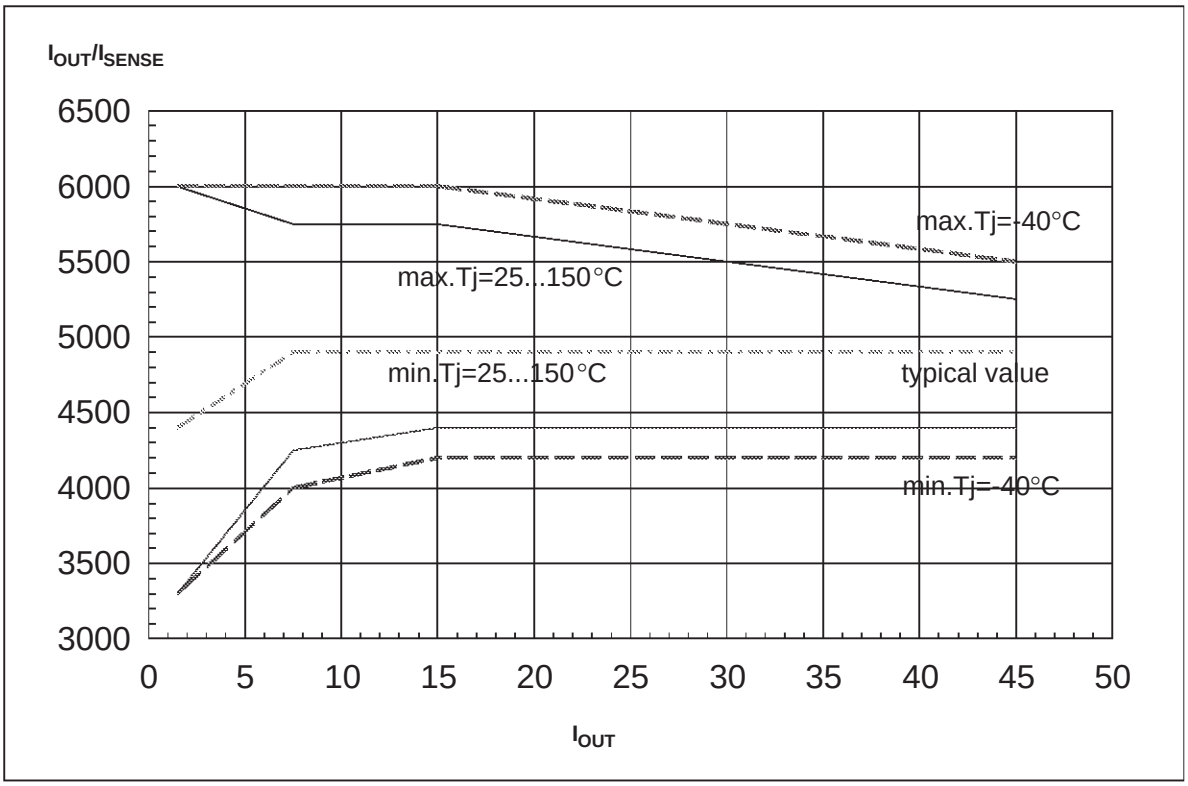
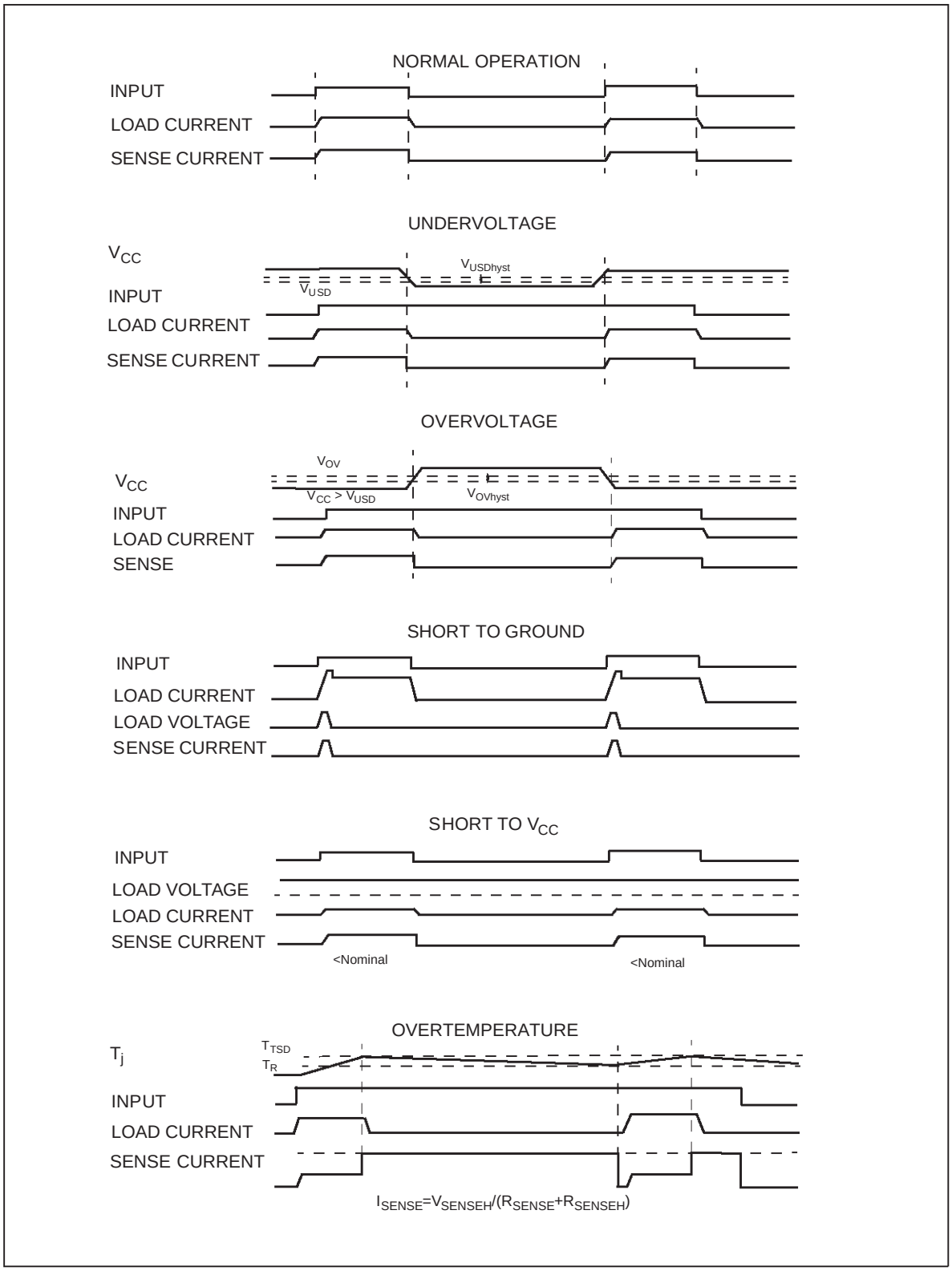
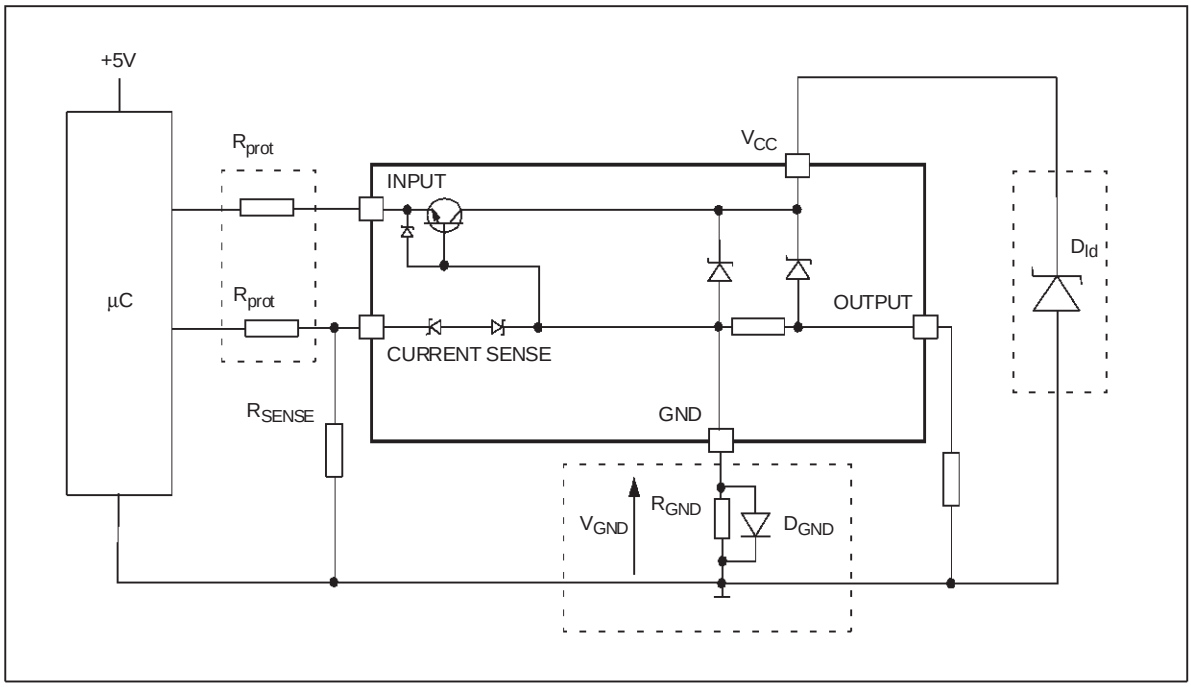


Figure1: Waveforms



APPLICATION SCHEMATIC



GND PROTECTION NETWORK AGAINST REVERSE BATTERY

Solution 1: Resistor in the ground line (R_{GND} only). This can be used with any type of load.

The following is an indication on how to dimension the R_{GND} resistor.

1) $R_{GND} \leq 600mV / (I_{S(on)max})$.

2) $R_{GND} \geq (-V_{CC}) / (-I_{GND})$

where $-I_{GND}$ is the DC reverse ground pin current and can be found in the absolute maximum rating section of the device's datasheet.

Power Dissipation in R_{GND} (when V_{CC}<0: during reverse battery situations) is:

$P_D= (-V_{CC})^2/R_{GND}$

This resistor can be shared amongst several different HSD. Please note that the value of this resistor should be calculated with formula (1) where $I_{S(on)max}$ becomes the sum of the maximum on-state currents of the different devices.

Please note that if the microprocessor ground is not common with the device ground then the R_{GND} will produce a shift ($I_{S(on)max} * R_{GND}$) in the input thresholds and the status output values. This shift will vary depending on how many devices are ON in the case of several high side drivers sharing the same R_{GND}.

If the calculated power dissipation leads to a large resistor or several devices have to share the same resistor then the ST suggests to utilize Solution 2 (see below).

Solution 2: A diode (D_{GND}) in the ground line.

A resistor (R_{GND}=1kΩ) should be inserted in parallel to D_{GND} if the device will be driving an inductive load.

This small signal diode can be safely shared amongst several different HSD. Also in this case, the presence of the ground network will produce a shift (j 600mV) in the input threshold and the status output values if the microprocessor ground is not common with the device ground. This shift will not vary if more than one HSD shares the same diode/resistor network.

LOAD DUMP PROTECTION

D_{ld} is necessary (Transil or MOV) if the load dump peak voltage exceeds V_{CC} max DC rating. The same applies if the device will be subject to transients on the V_{CC} line that are greater than the ones shown in the ISO T/R 7637/1 table.

µC I/Os PROTECTION:

If a ground protection network is used and negative transients are present on the V_{CC} line, the control pins will be pulled negative. ST suggests to insert a resistor (R_{prot}) in line to prevent the µC I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of µC and the current required by the HSD I/Os (Input levels compatibility) with the latch-up limit of µC I/Os.

$-V_{CCpeak}/I_{latchup} \leq R_{prot} \leq (V_{OH\mu C}-V_{IH}-V_{GND}) / I_{IHmax}$

Calculation example:

For V_{CCpeak}= - 100V and $I_{latchup} \geq$ 20mA; $V_{OH\mu C} \geq$ 4.5V

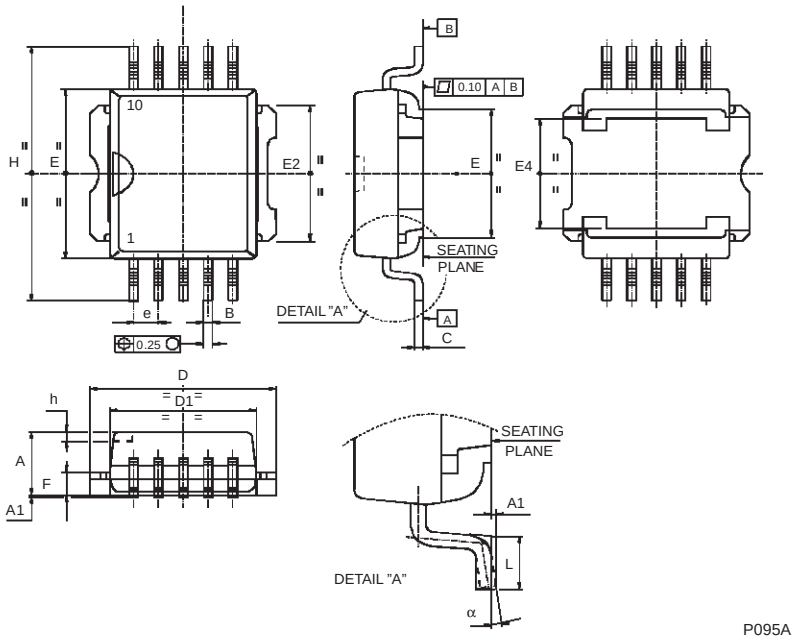
5kΩ ≤ R_{prot} ≤ 10kΩ.

Recommended R_{prot} value is 65kΩ.

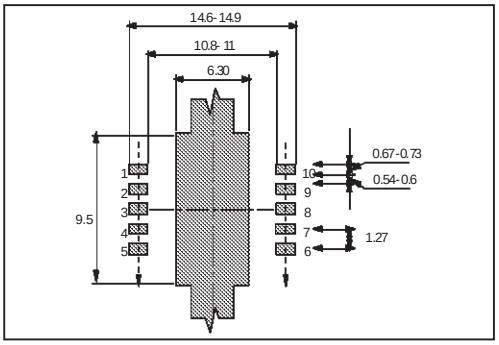
PowerSO-10™ MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	3.35		3.65	0.132		0.144
A (*)	3.4		3.6	0.134		0.142
A1	0.00		0.10	0.000		0.004
B	0.40		0.60	0.016		0.024
B (*)	0.37		0.53	0.014		0.021
C	0.35		0.55	0.013		0.022
C (*)	0.23		0.32	0.009		0.0126
D	9.40		9.60	0.370		0.378
D1	7.40		7.60	0.291		0.300
E	9.30		9.50	0.366		0.374
E2	7.20		7.60	0.283		300
E2 (*)	7.30		7.50	0.287		0.295
E4	5.90		6.10	0.232		0.240
E4 (*)	5.90		6.30	0.232		0.248
e		1.27			0.050	
F	1.25		1.35	0.049		0.053
F (*)	1.20		1.40	0.047		0.055
H	13.80		14.40	0.543		0.567
H (*)	13.85		14.35	0.545		0.565
h		0.50			0.002	
L	1.20		1.80	0.047		0.070
L (*)	0.80		1.10	0.031		0.043
α	0º		8º	0º		8º
α (*)	2º		8º	2º		8º

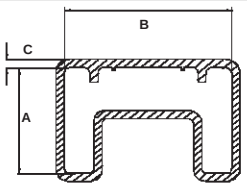
(*) Muar only POA P013P



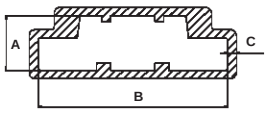
PowerSO-10™ SUGGESTED PAD LAYOUT



TUBE SHIPMENT (no suffix)



CASABLANCA

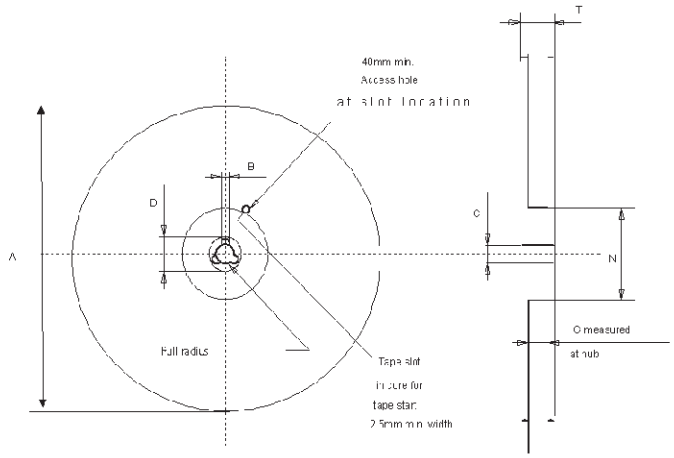


MUAR

All dimensions are in mm.

	Base Q.ty	Bulk Q.ty	Tube length (± 0.5)	A	B	C (±0.1)
Casablanca	50	1000	532	10.4	16.4	0.8
Muar	50	1000	532	4.9	17.2	0.8

TAPE AND REEL SHIPMENT (suffix "13TR")



REEL DIMENSIONS

Base Q.ty	600
Bulk Q.ty	600
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	24.4
N (min)	60
T (max)	30.4

All dimensions are in mm.

TAPE DIMENSIONS

According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	**W**	24
Tape Hole Spacing	**P0 (± 0.1)**	4
Component Spacing	**P**	24
Hole Diameter	**D (± 0.1/-0)**	1.5
Hole Diameter	**D1 (min)**	1.5
Hole Position	**F (±0.05)**	11.5
Compartment Depth	**K (max)**	6.5
Hole Spacing	**P1 (± 0.1)**	2

All dimensions are in mm.