QNEE9801
QUALITY NOTE

High Reliability Certified Flow (HRCF)

The High Reliability Certified Flow has been developed by STMicroelectronics for sensitive applications, such as security automotive and medical applications, that need a very high level of reliability (with the proviso that expressed written permission is still required from STMicroelectronics before using these devices in such applications, as indicated in disclaimer at the end of this document). This special production flow is tailored to the “3” temperature range of products (-40 °C to +125 °C).

With HRCF, ST is able to ensure the greatest stringency in controlling the product failure rate and reliability. HRCF is also a continuous quality improvement driver, with the production test data and reject failure analysis being used for fine tuning the HRCF, and manufacturing processes.

HRCF is highly efficient at detecting “out of normal distribution” lots, and gives a very high capability for screening for early failures. The central principle of the HRCF is to perform as many tests and screens as possible at wafer level (to maintain wafer to wafer traceability) and to apply all pass/fail and min/max criteria at the wafer level rather than at lot level. Using this principle, “out of normal distribution” wafers are removed, and do not pollute the defect figures for the full lot (which is measured in just a few parts per million). Consequently, only well-centered lots are used for HRCF.

The tests are grouped in seven test modules. The headings of these modules are as follows:

- Process parameter test (T84)
- Electrical wafer sort
- Wafer visual/mechanical inspection
- Final test
- Final visual/mechanical inspection
- QA cycling gate
- QA electrical gate

These tests are described in the following sections, with attention drawn to the main differences between ST’s HRCF range 3 production flow, and our Standard range 6 production flow. The operating conditions are summarized in Table 3, at the end of this document.

PROCESS PARAMETER TEST (T84)

The process parameter test, T84, is performed for HRCF in the same way as it is for the Standard flow. During this test, using our Statistical Process Control (SPC) checks are made on the process parameters that are directly linked to yield and performance, and on the parameters that are linked to product reliability.

ELECTRICAL WAFER SORT

Under HRCF, there are two steps in this stage of the testing, as opposed to one under the Standard flow.

1. **Electrical and functional test.** This test, used on Standard range 6 and HRCF range 3 products, is designed to screen 100% of the wafers against the standard defect distribution. Under the Standard flow, wafers are tested at ambient temperature, but under HRCF, the test is performed at 90 °C thereby

allowing us to exercise the wafers almost to the high end of their specified operating temperature.

During this test, all dice are subjected to a number of erase/write cycles, at V_{CC} = 6.0 V, in order to release charge that has been induced by the fabrication process, and to break any unreliable, weak parts. This corresponds to an Early Failure Screening, and is equivalent to the burn-in stage for logic products. This test stresses all high voltage circuitry-oxide (such as decoder transistors, charge pump and ramp generator capacitors) together with the tunnel window-oxide. More than 98% of dice are exercised. Under the Standard flow, 500 erase/write cycles are performed, but under HRCF each cell is erase/write cycled 3000 times. This test finishes with the programming of the entire memory, ready for the retention test.

2. **Retention test.** The aim of this test, performed on HRCF range 3 products, is to screen for parts containing leaky memory cells. The first electrical test is followed by a 24 hour bake at 250 °C. This high temperature bake, performed at the wafer level, is equivalent to a retention test of 7.4 years of the application operating at 55 °C. The retention bake is then followed by a second electrical test performed at 25 °C to verify the data retention. On Standard range 6 products, this test is only performed on the finished product, and so is limited to 150 °C, due to specification of the package.

EEPROM performance is defined by two main criteria: *endurance* and *retention*. At the wafer level, product range 3 parts that are manufactured with HRCF are tested for both criteria, thereby maintaining wafer to wafer traceability, and allowing pass/fail decision-making on the smallest homogenous population of processed material.

WAFER VISUAL MECHANICAL INSPECTION

The aim of this inspection is to check each wafer for any abnormal contamination, or mechanical damage that may affect product performance. Under the Standard flow, visual and mechanical inspection is performed on a lot sampling basis: 5 wafers per lot (25 wafers). Under HRCF, this step is performed on all the wafers of the lot.

FINAL TEST

1. **Thermal cycling (-65°C/150°C).** After assembly, each lot of range 3 products, manufactured with the HRCF, is cycled up to 20 times from -65 °C to 150 °C. Mechanical stress tests are performed to show up any package weakness that had been induced during the assembly of the product. For Standard range 6 products, this behavior is monitored during the daily production.
2. **Electrical and functional test.** This first test, for Standard range 6 and HRCF range 3 products, is designed to screen 100% of the parts for assembly rejects and high temperature functional failures. Under the Standard flow, assembled lots are tested at 90 °C, but under HRCF, the test is performed at 130°C. This test finishes with the programming of the entire memory, ready for the retention test.
3. **Retention test.** The aim of this test, for Standard range 6 and HRCF range 3 products, is to screen for assembly defects (for HRCF range 3 products) and for standard defect distribution rejects (for Standard range 6 products). 100% of the parts are submitted to a retention bake at 150 °C. The bake duration is 48 hours (for HRCF range 3 products) and 36 hours (for Standard range 6 products). This bake is equivalent to a retention test of 7.8 months of an application operating at 55 °C (for HRCF range 3 products) and of 3.8 months (for Standard range 6 products). The retention bake is then followed by a second electrical test, performed at 25 °C, to verify the retention of the data programmed during the electrical and functional test.

FINAL VISUAL MECHANICAL INSPECTION

The aim of this inspection is to control lead coplanarity and marking. The same mechanical and visual inspection is performed on both flows, except that automated lead scanning and straightening is explicitly specified for HRCF.

QA CYCLING GATE

The same two steps are performed under HRCF as under the Standard flow, but with a different sample size (as shown in Table 1).

Table 1. QA Cycling Gate

Flow	Sample	Accepted	Rejected
HRCF range 3	145 per wafer lot	0	1
STD range 6	45 per wafer lot	0	1

1. **Erase/write cycles.** The devices are subjected to 100000 erase/write cycles, at 25 °C, to verify the endurance of the wafer lot. This test finishes with the programming of the entire memory, ready for the retention test.
2. **Retention test.** The sample is submitted to a 150 °C bake for 24 hours, followed by an electrical test at 25 °C, to verify the retention of the data programmed during the erase/write cycles.

QA ELECTRICAL GATE

Again, the same two steps are performed on both production flows, but with a different sample size (as shown in Table 2).

Table 2. QA Electrical Gate

Flow	Sample	Accepted	Rejected
HRCF range 3	315 per test lot	0	1
STD range 6	200 per test lot	0	1

1. **Low temperature test.** Samples are tested on each lot at -40 °C, to verify the functionality of the lot at the cold end of its temperature range. This test finishes with the programming of the entire memory, ready for the retention test.
2. **Retention test.** The low temperature test is followed by a bake at 150 °C for 24 hours, and by an electrical test at 85 °C (for Standard range 6 products) and 125 °C (for HRCF range 3 products). This is to verify the retention of the data programmed during the low temperature test.

Table 3. Summary of Operating Conditions (subject to change without notice, as noted below)

Test Procedure	Standard Flow		High Reliability Certified Flow	
		Sample size		Sample size
Process Parameter Test	yes		yes	
Electrical Wafer Sort				
Electrical and functional test	Ambient (read retention pattern)	100%	90 °C (write retention pattern)	100%
Erase/write cycles	500 cycles	100%	3000 cycles	100%
Retention bake	200 °C for 24 hour	100%	250 °C for 24 hour	100%
Electrical test	no		Ambient (read retention pattern)	100%
Wafer Mechanical and Visual Inspection	yes	5 wafers/lot	yes	100%
Assembly	yes	100%	yes	100%
Final Test				
Temperature cycles	no (process monitor)		-65 °C to +150 °C	100 %
Electrical and functional test	90 °C (read retention pattern)	100 %	130 °C (write retention pattern)	100 %
Retention bake	no		150 °C for 48 hours	100 %
Electrical test	no		Ambient (read retention pattern)	100%
Final Mechanical and Visual Inspection	yes	100%	yes + SO lead scanning + DIL lead straightening	100 %
QA Cycling Gate	Accept 0 / Reject 1		Accept 0 / Reject 1	
Erase/write cycling	100 000 cycles	45 / wafer lot	100 000 cycles	145 / wafer lot
Retention bake	150 °C for 24 hours	45 / wafer lot	150 °C for 24 hours	145 / wafer lot
Electrical test	Ambient	45 / wafer lot	Ambient	145 / wafer lot
QA Electrical Gate	Accept 0 / Reject 1		Accept 0 / Reject 1	
Electrical and functional test	-40 °C	200 / wafer lot	-40 °C	315 / wafer lot
Retention bake	150 °C for 24 hours	200 / wafer lot	150 °C for 24 hours	315 / wafer lot
Electrical test	85 °C	200 / test lot	125 °C	315 / test lot

Because HRCF is also a continuous quality improvement tool, used to drive the quality improvement of our overall production, ST reserves the right to modify HRCF at any time, without notice.

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail addresses:

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Please remember to include your name, company, location, telephone number and fax number.

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