

## D.A.A. LINE INTERFACE

PRELIMINARY DATA

- HOOK SWITCH DRIVER
- RING INDICATOR
- LINE INTERFACE
  - DC TERMINATION (4V AT 20mA)
  - 2W/4W HYBRID CONVERTER
  - FLAT FREQUENCY RESPONSE DOWN TO 10Hz FOR 56Kps MODEM
- INTERFACE WITH CAPACITIVE ISOLATION BARRIER
- CALLER ID INTERFACE
- DIGITAL PHONE LINE OR OVER LOOP CURRENT LIMIT DETECT
- PHONE LINE IN USE CHECK

### APPLICATIONS

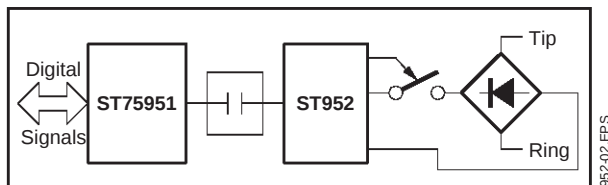
- MODEMS UP TO V.34, 33.6KBPS AND 56Kbps
- PCMCIA CARDS
- FAX MACHINES
- PERSONAL DIGITAL ASSISTANTS
- ANSWERING MACHINES
- HIGH FEATURE PHONES
- WEBPHONES AND SET TOP BOXES

### DESCRIPTION

ST952 is a line interface designed to implement Modem application up to 56Kbps and Voice applications.

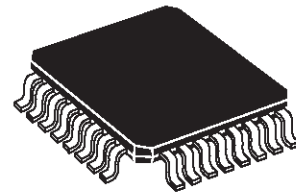
ST952 interfaces between telephone line and capacitive isolation barrier.

A complete D.A.A. is made with ST75951 which interfaces between capacitive isolation barrier and the DSP or HSP signals.



It incorporates Krypton Isolation Inc. patented silicon DAA technology.

The ring burst signal is detected by ST952 and is sent to ST75951 through the capacitive isolation barrier. Using the control signals given by ST75951, through the capacitive isolation barrier, ST952 activates the off-hook or the CLID external transistor switch.



**TQFP32** (7 x 7 x 1.4mm)  
(Thin Plastic Quad Flat Pack)  
**ORDER CODE** : ST952TQF7

If CLID external transistor switch is enabled, a limited amount of current, less than 1mA, is drawn from the line.

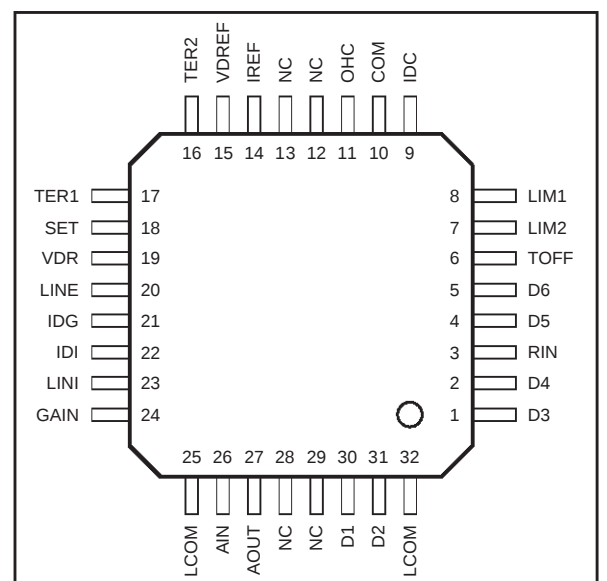
In off-hook state, ST952 DC voltage, 4V at a 20mA line current, allows to interface with most of public networks in the world.

The return loss is externally adjustable to real or complex impedance.

In case of a wrong connection in a digital phone line, ST952 detects the over current value and sends to ST75951 an alert signal through the capacitive isolation barrier.

Before starting a line connection, ST952 is able to check if the line is used by an other terminal connected on the same telephone line.

### PIN CONNECTIONS



## PIN LIST

| Pin Number | Name  | Type   | Description                           |
|------------|-------|--------|---------------------------------------|
| 1          | D3    | Output | Isolation Signal Output               |
| 2          | D4    | Output | Isolation Signal Output               |
| 3          | RIN   | Input  | Ring Signal Input                     |
| 4          | D5    | Input  | Isolation Control Signal Input        |
| 5          | D6    | Input  | Isolation Control Signal Input        |
| 6          | TOFF  | Supply | Internal Reference Supply             |
| 7          | LIM2  | Input  | Loop Current Limiter Control          |
| 8          | LIM1  | Output | Loop Current Limiter Control          |
| 9          | IDC   | Output | Caller ID Control Output              |
| 10         | COM   | Output | Off-hook & ID Commun Output           |
| 11         | OHC   | Output | Off-hook Control Output               |
| 12         | N.C.  | -      | Not Connected                         |
| 13         | N.C.  | -      | Not Connected                         |
| 14         | IREF  | Input  | Current Reference Setting             |
| 15         | VDREF | Supply | Internal Reference Pin                |
| 16         | TER2  | Output | Current Regulator Control Feedback    |
| 17         | TER1  | Output | Current Regulator Control Output      |
| 18         | SET   | Input  | Current Regulator Filter              |
| 19         | VDR   | Supply | Line DC Voltage Regulator             |
| 20         | LINE  | Output | Line AC Signal Output                 |
| 21         | IDG   | Input  | Caller ID Voltage Reference Input     |
| 22         | IDI   | Input  | Caller ID Signal Input                |
| 23         | LINE  | Input  | Line AC Signal Input                  |
| 24         | GAIN  | Input  | Transmit Gain / Trans-Hybrid Loss Set |
| 25         | LCOM  | Ground | Line Side Common Ground               |
| 26         | AIN   | Input  | Analog Transmit Signal Input          |
| 27         | AOUT  | Output | Analog Transmit Signal Output         |
| 28         | N.C.  | -      | Not Connected                         |
| 29         | N.C.  | -      | Not Connected                         |
| 30         | D1    | Input  | Isolation Signal Input                |
| 31         | D2    | Input  | Isolation Signal Input                |
| 32         | LCOM  | Ground | Line Side Common Ground               |

**Note :** Pins 12, 13, 28 and 29 must be left opened.

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## PIN DESCRIPTION

### D1 - D2

These pins input the AC signal modulated at Fmod coming from ST75951 through the capacitive isolation barrier.

### D3 - D4

These pins output the AC signal modulated at Fmod in off-hook mode and at Fmod/2 in CLID mode to ST75951 through the capacitive isolation barrier.

In ring mode, these pins output the ring information, a differential 6V<sub>PP</sub>/1MHz signal.

### D5 - D6

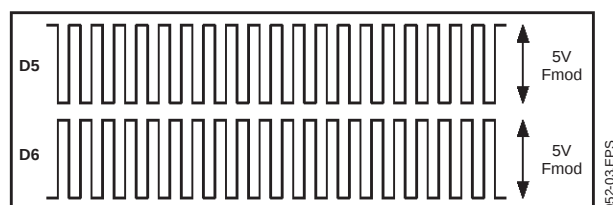
These control pins input a 5V<sub>PP</sub>/Fmod signal coming from ST75951 through the capacitive isolation barrier.

These signals control the off-hook and CLID external transistor switches and are sent to the internal transmit demodulator and receive modulator.

Off-hook mode is enabled with a 5V<sub>PP</sub>/Fmod signal sent on D5 and D6 inputs with an opposite phase (see Figure 1). With a dedicated application it is possible to reduce the input level to 3V<sub>PP</sub>.

CLID mode is enabled with a 5V<sub>PP</sub>/Fmod signal sent on D5 input only (see Figure 2). With a dedicated application it is possible to reduce the input level to 3V<sub>PP</sub>.

Figure 1



### LINE

DC positive line connection and line AC signal output.

### LCOM

Negative line connection.

### LINE

Line AC signal input in off-hook mode.

### AIN - AOUT

The transmit signal coming from AIN pin is injected in AOUT pin to the 2W/4W internal converter stage. The line echo is minimized if R3, connected between LINE and VDR pins is equal to 620Ω.

### GAIN

R1 connected on this pin fixes the transmit gain. The R1 recommended value, on a 600Ω AC line termination, is 82Ω.



### RIN

During the ring burst, a 1MHz oscillator is powered on this pin and a 6V<sub>PP</sub>/1MHz signal is sent on D3 and D4 to indicate the ring presence.

### IREF

Internal reference current source setting, R4 must be equal to 82kΩ.

### VDR

Power supply for the transmit and receive paths in Off-Hook mode.

### VDREF

Internal resistor reference.

### SET

Line gyrator AC/DC filter.

### OHC

When D5 and D6 inputs a 5V<sub>PP</sub>/Fmod signal in opposite phase, this pin puts ON the hook switch external Q1/Q2 transistor stage.

### IDC

When D5 input a 5V<sub>PP</sub>/Fmod signal, this pin puts ON the CLID external Q3/Q4 transistor stage. R2 limits the line current in CLID mode at 1mA max.

### COM

Common output for off-hook and CLID external transistor stages

### TER1 - TER2

These pins control the external Q5 transistor, in which the main part of the line current goes through to meet the line DC,  $V = f(I_L)$ , termination requirements.

### IDI

Line AC signal input in CLID mode.

### IDG

Power supply for the receive path in CLID mode.

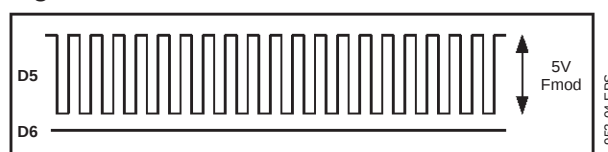
### LIM1 - LIM2

200mA over current detection for device protection.

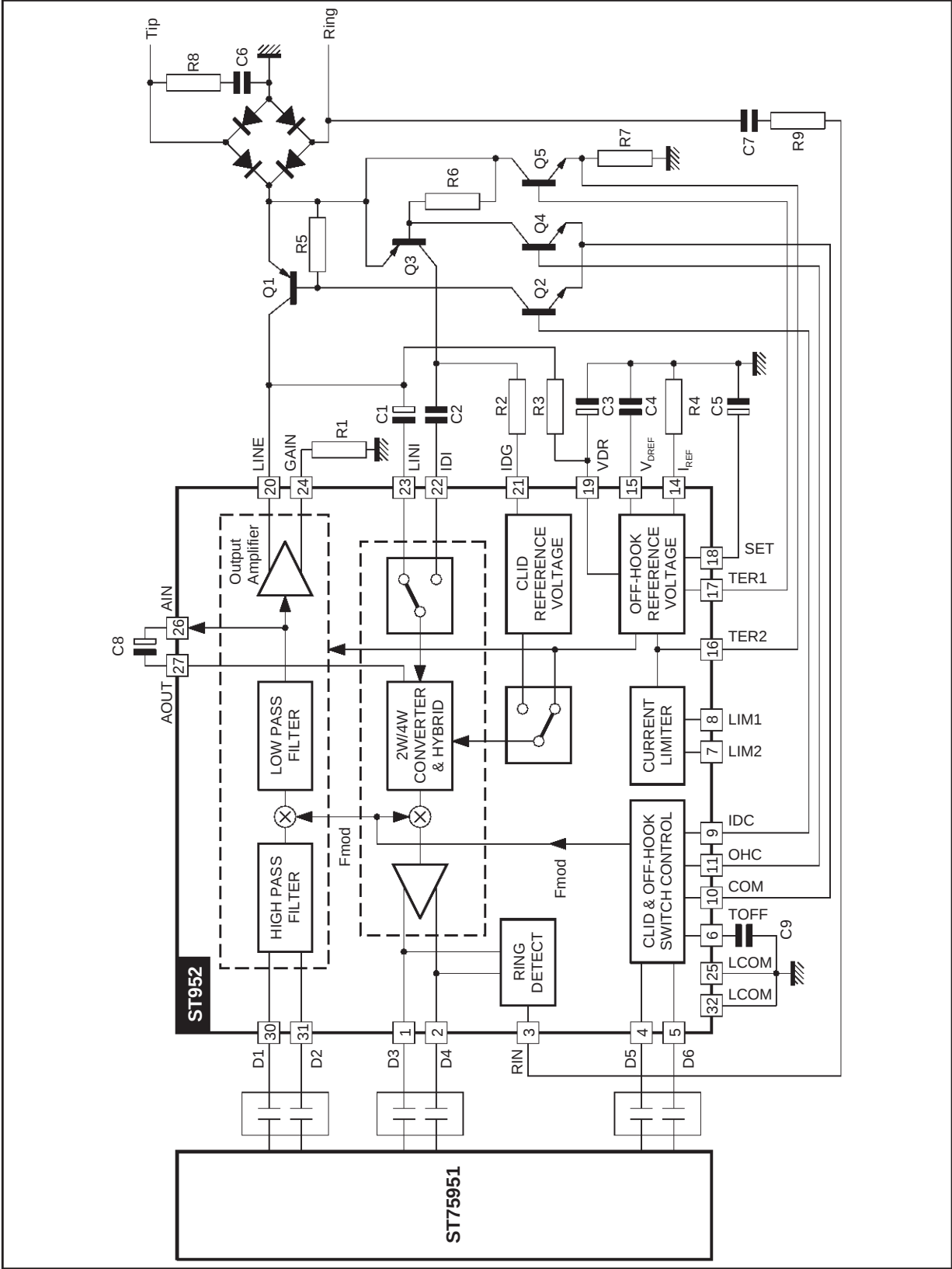
### TOFF

Internal Reference Supply.

Figure 2



BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATING** (AGND = DGND = 0V, all voltages with respect to 0V)

| Symbol      | Parameter                        | Value     | Unit |
|-------------|----------------------------------|-----------|------|
| $V_{MLINE}$ | Positive Line Voltage Continuous | 14        | V    |
| $T_{oper}$  | Operating Temperature            | 0, +70    | °C   |
| $T_{stg}$   | Storage Temperature              | -55, +150 | °C   |

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**THERMAL DATA**

| Symbol        | Parameter                                | Value | Unit |
|---------------|------------------------------------------|-------|------|
| $R_{th(j-a)}$ | Junction-ambient Thermal Resistance Max. | 80    | °C/W |

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**ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ , unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|--------|-----------|-----------------|------|------|------|------|
|--------|-----------|-----------------|------|------|------|------|

## DC AND AC TERMINATION (see Figure 3)

|            |              |                                                                                |    |             |  |          |
|------------|--------------|--------------------------------------------------------------------------------|----|-------------|--|----------|
| $V_{LINE}$ | Line Voltage | $I_L = 20\text{mA}$<br>$I_L = 120\text{mA}$                                    |    | 4.1<br>10.5 |  | V<br>V   |
| ZLOSS      | Return Loss  | $I_L = 20\text{mA}$ , $V_{LAC} = -6\text{dBV}$<br>$f = 200$ to $4000\text{Hz}$ | 24 |             |  | dB<br>dB |

RECEIVE PATH ( $I_L = 20\text{mA}$ ,  $f = 1\text{kHz}$ , see Figure 4)

|      |                                         |                                                                                                       |              |            |              |            |
|------|-----------------------------------------|-------------------------------------------------------------------------------------------------------|--------------|------------|--------------|------------|
| Grx  | Receive Gain                            | $V_{LAC} = 0\text{dBV}$ , $V_{TAC} = 0$                                                               | -0.5         | 0          | 0.5          | dB         |
| Grf  | Receive Frequency Response              | $V_{LAC} = 0\text{dBV}$ , $V_{TAC} = 0$<br>$f = 200$ to $3400\text{Hz}$<br>$f = 50$ to $200\text{Hz}$ | -0.1<br>-0.5 |            | +0.1<br>+0.5 | dB<br>dB   |
| Rxhd | Receive 2nd/3th/4th Harmonic Distortion | $V_{LAC} = 0\text{dBV}$ , $V_{TAC} = 0$<br>$f = 150\text{Hz}$<br>$f = 1000\text{Hz}$                  |              | -79<br>-82 |              | dBV<br>dBV |
| Thl  | Trans-Hybrid Loss                       | $V_{LAC} = 0$ , $V_{TAC} = -6\text{dBV}$ ,<br>$F_{mod} = 1.5\text{MHz}$                               | 30           | 35         |              | dB         |
| Rn   | Receive Noise Floor                     | $V_{LAC} = V_{TAC} = 0$ ,<br>$f = 200\text{-}3400\text{Hz}$ , $100\text{Hz BW}$                       |              | -93        |              | dBV        |

TRANSMIT PATH ( $I_L = 20\text{mA}$ ,  $f = 1\text{kHz}$ ,  $V_{LAC} = 0$ , see Figure 4)

|       |                                          |                                                                       |      |     |      |          |
|-------|------------------------------------------|-----------------------------------------------------------------------|------|-----|------|----------|
| Gtx   | Transmit Gain                            | $V_{TAC} = -6\text{dBV}$                                              | -0.5 | 0   | 0.5  | dB       |
| Gtf   | Transmit Frequency Response              | $V_{TAC} = -6\text{dBV}$ , $f = 200$ to $4000\text{Hz}$               | -0.2 |     | +0.2 | dB       |
| Txhd  | Transmit 2nd/3th/4th Harmonic Distortion | $V_{TAC} = -6\text{dBV}$ , $F_{mod} = 1.5\text{MHz}$                  |      | -82 |      | dBV      |
| Txmax | Max Line Drive Voltage                   |                                                                       |      | 3   |      | $V_{PP}$ |
| Tn    | Transmit Noise Floor                     | $V_{TAC} = 0$ ,<br>$f = 200\text{-}3400\text{Hz}$ , $100\text{Hz BW}$ |      | -93 |      | dBV      |

## POWER AND DC LOGIC INPUT (see Figure 5)

|            |                   |                                                            |     |  |             |        |
|------------|-------------------|------------------------------------------------------------|-----|--|-------------|--------|
| $I_{LINE}$ | Line Current      | ST952 Line Pin + $I_c(Q5)$                                 | 10  |  | 120         | mA     |
| $V_{OFF}$  | Hook Switch Input | D5 and D6 Input<br>Active (Off-hook)<br>Inactive (On-hook) | 2.7 |  | 5.25<br>0.8 | V<br>V |
| $V_{CLID}$ | CLID Input        | D5 Input<br>Active (CLID On)<br>Inactive (On-hook)         | 2.7 |  | 5.25<br>0.8 | V<br>V |

## CALLER ID RECEIVE PATH (see Figure 6)

|           |                   |                           |    |   |    |    |
|-----------|-------------------|---------------------------|----|---|----|----|
| $G_{RID}$ | CLID Receive Gain | $V_{TAC} = -15\text{dBV}$ | -1 | 0 | +1 | dB |
| $I_{LID}$ | CLID Line Current |                           |    |   | 1  | mA |

## RING INDICATOR (see Figure 7)

|                          |                        |                               |    |  |   |        |
|--------------------------|------------------------|-------------------------------|----|--|---|--------|
| $V_{RIOF}$<br>$V_{RION}$ | D3 & D4 Ring indicator | D3 = D4 = 0<br>D3 = D4 = 3VPP | 18 |  | 8 | V<br>V |
|--------------------------|------------------------|-------------------------------|----|--|---|--------|

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**Note** : D3 and D4 are complementary outputs.

Figure 3 : Test 1

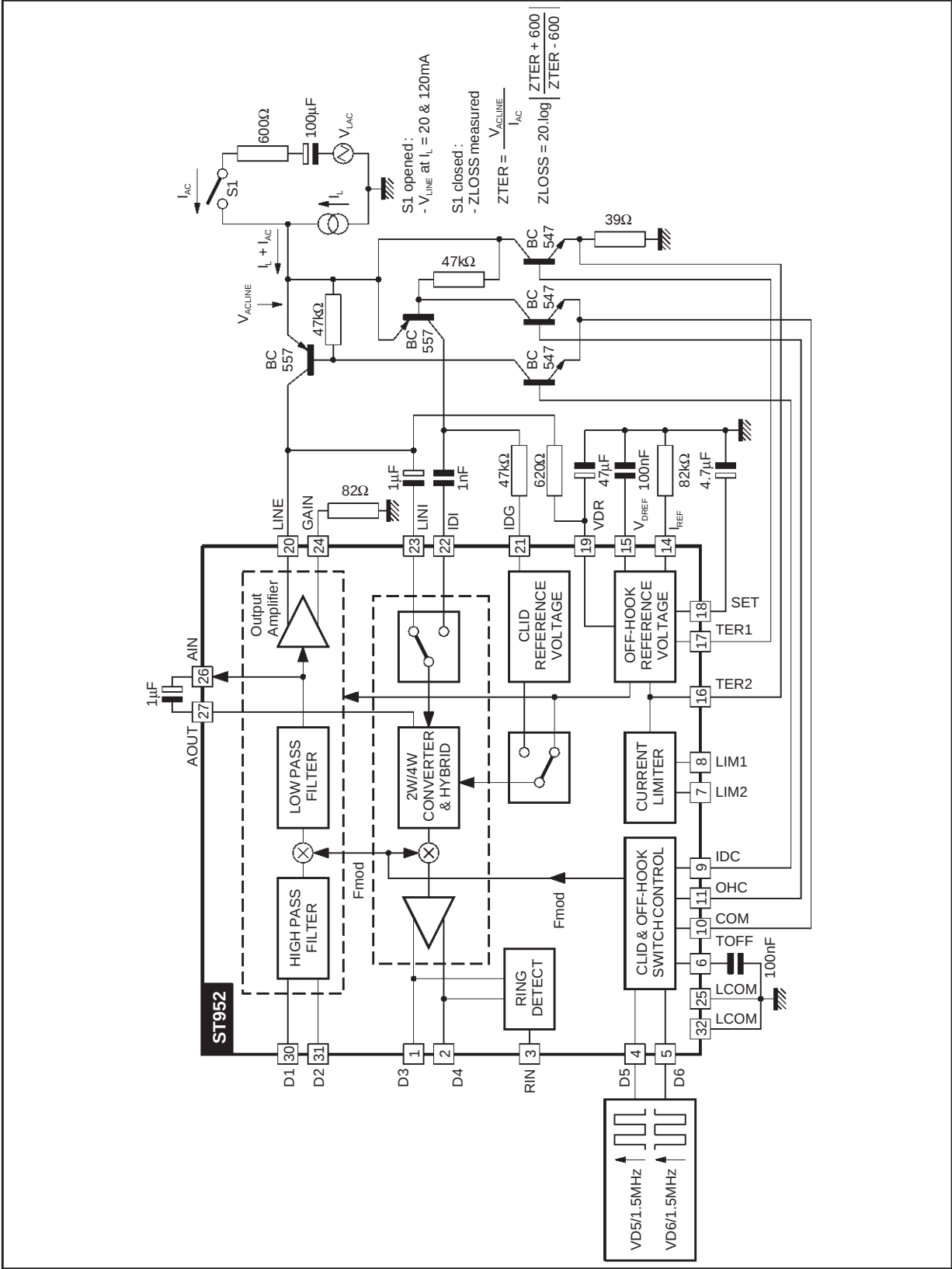


Figure 4 : Test 2

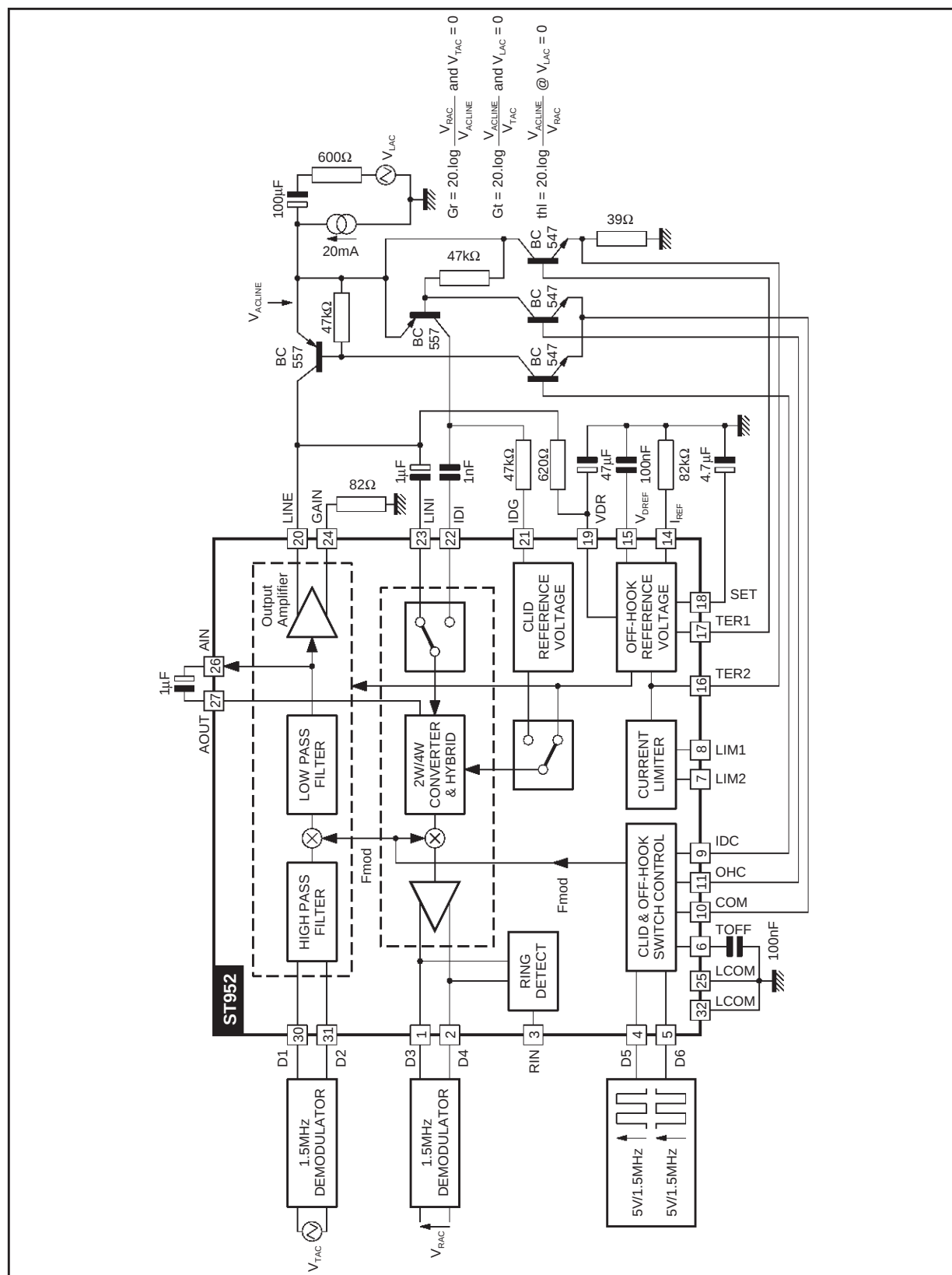


Figure 5 : Test 3

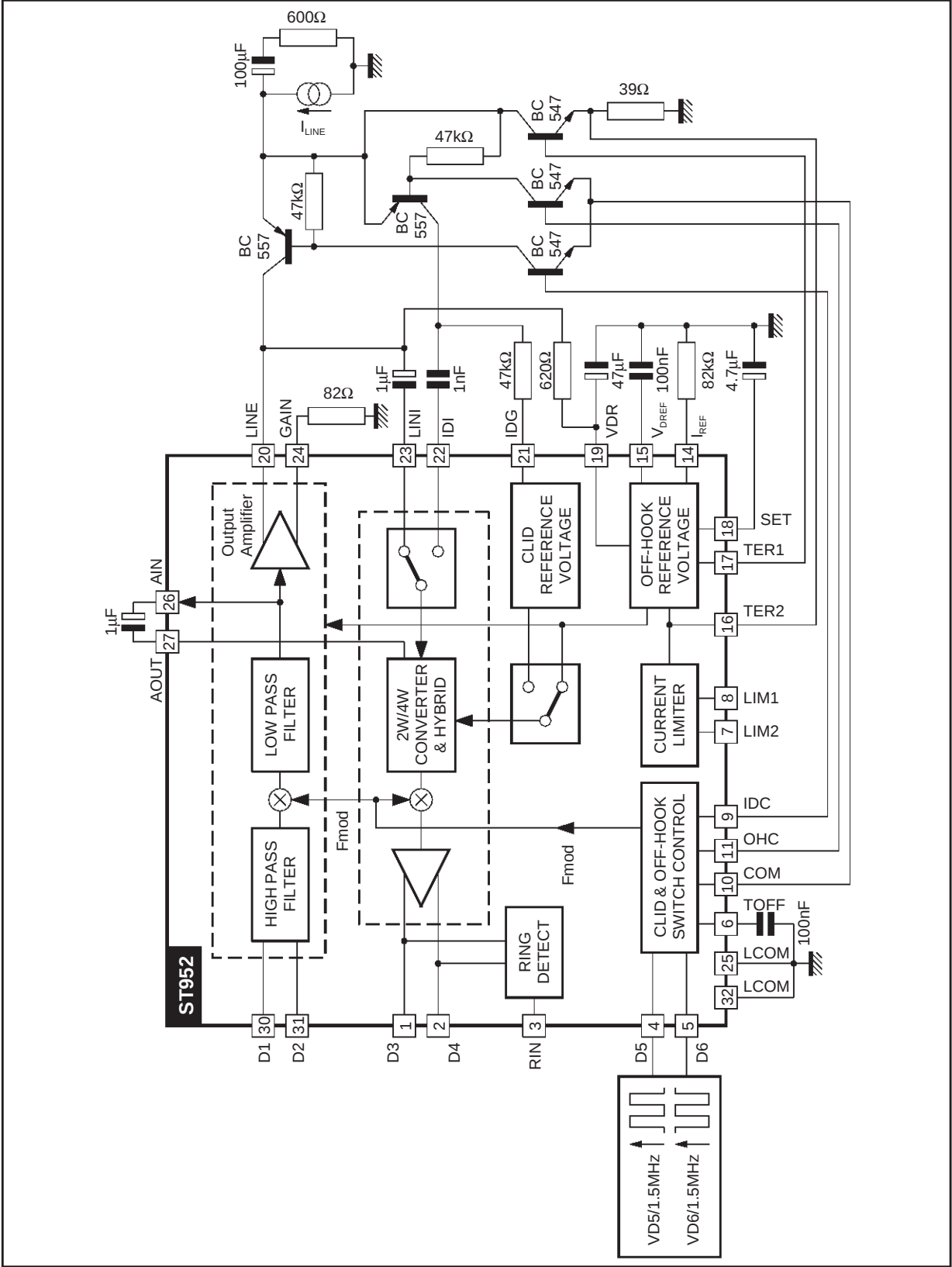
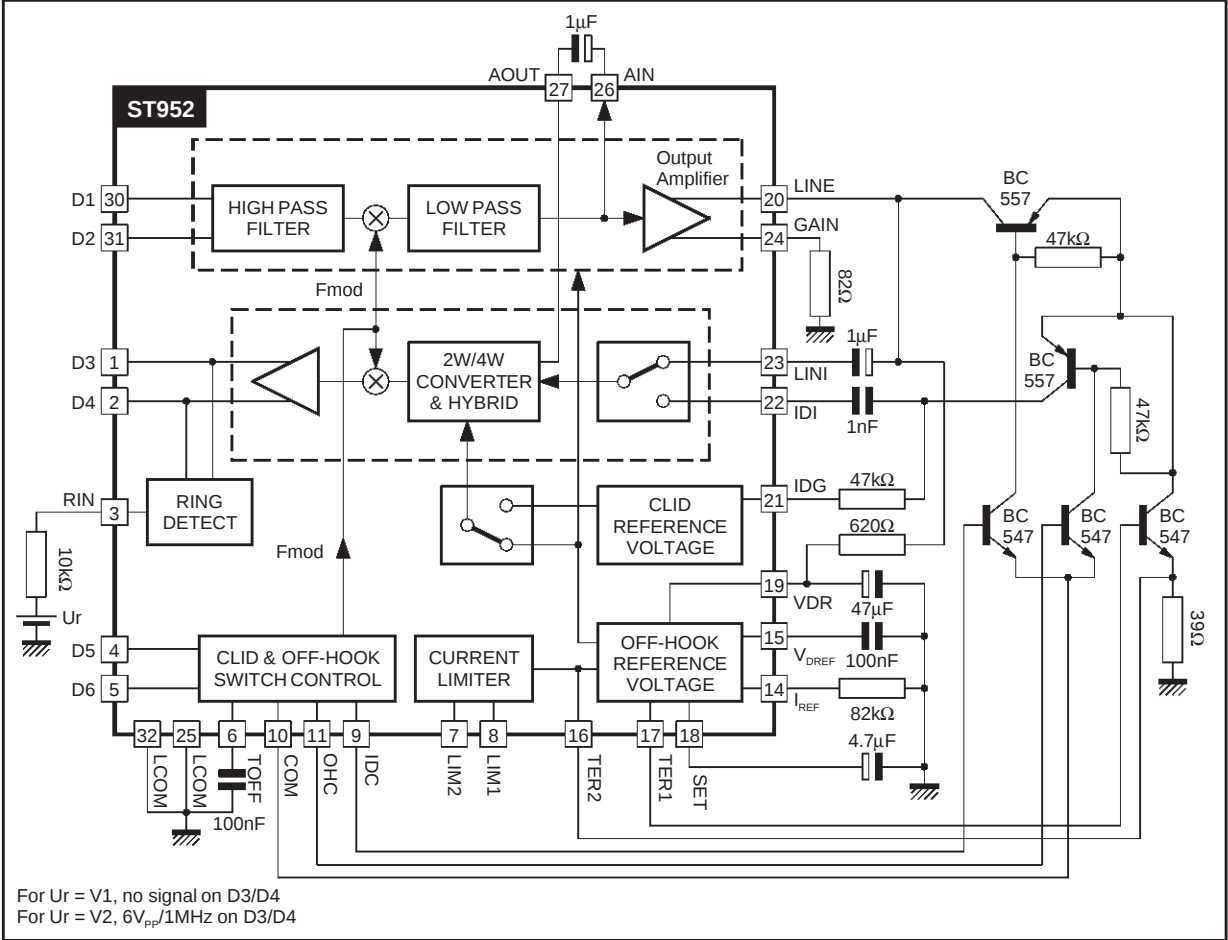
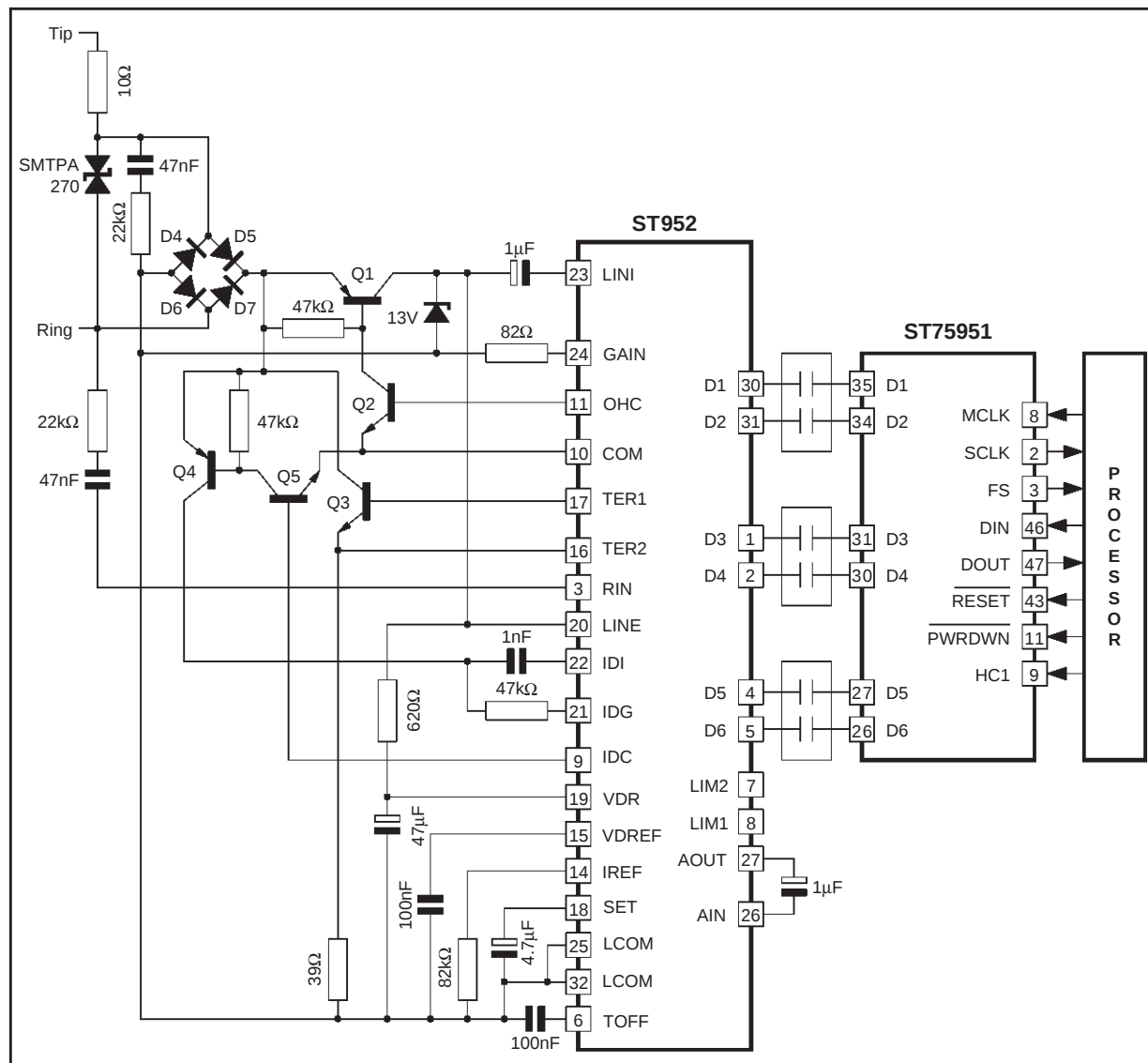




Figure 7 : Test 5



## TYPICAL APPLICATION (5V Supply on ST75951)



952-11EPS

