QRR9801
QUALITY & RELIABILITY REPORT

April 1997 to March 1998 - EPROM, FLASH Memory, EEPROM and NVRAM Products

INTRODUCTION

STMicroelectronics manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; Flash memories in 1.2 to 0.6µ CMOS technology; OTP EPROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAM: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.8µ HCMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from April 1997 to March 1998. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Attilio PANCHIERI

CONTENT

Table 1. Final Average Outgoing Quality (AOQ), April 1997 to March 1998

Process	Electrical ppm				Visual ppm			
	2Q97	3Q97	4Q97	1Q98	2Q97	3Q97	4Q97	1Q98
UV EPROM CMOS NMOS	 19 0	 17 0	 19 0	 20 0	 12 0	 15 20	 11 0	 13 20
OTP EPROM CMOS	20	18	18	20	6	14	11	10
FLASH CMOS	4	0	0	2	4	5	10	6
NVRAM CMOS	0	0	0	0	4	4	5	3
EEPROM CMOS	1	1	2	2	5	4	6	8

Table 2. Failure Rate Predictions (Fit), April 1997 to March 1998

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C ($x 10^6$)	Life Test Failure	Failure rate (Fit) Confidence Level	
	Dev. hrs ($x 10^6$)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -35%	4.73	140	0.6	4.0	1,297	0	0.7	1.8
CMOS E6 - DM	3.81	140	0.6	4.0	1,045	0	0.9	2.2
CMOS E6-10%	1.25	140	0.6	4.0	344	0	2.6	6.7
OTP EPROM								
CMOS E5 -35%	2.67	140	0.6	4.0	690	0	1.3	3.3
FLASH								
CMOS T5 -20%	8.18	140	0.6	4.0	2,120	0	0.4	1.0
CMOS T6	12.79	140	0.6	4.6	3,816	0	0.3	0.1
NVRAM								
CMOS Spectrum	1.82	100	0.7	64	2,324	1	0.8	1.7
HCMOS S3	1.63	100	0.7	64	2,088	1	1.0	1.9
HCMOS 4DZ	2.38	125	0.7	6.0	1,102	0	0.8	2.1
EEPROM								
CMOS F4	1.05	140	0.6	3.0	246	0	3.7	9.3
CMOS F4S	4.09	140	0.6	3.0	962	0	0.9	2.4

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	-	-	-	-	525	0	160	0	80	0	-	-
		– 168 hrs	-	-	-	-	400	0	160	0	80	0	-	-
		– 500 hrs	-	-	-	-	400	0	160	0	80	0	-	-
		– 1000 hrs	-	-	-	-	400	0	160	0	80	0	-	-
Retention Bake	1008	250°C,												
		– 48 hrs	-	-	-	-	400	0	160	0	80	0	-	-
		– 168 hrs	-	-	-	-	400	0	160	0	80	0	-	-
		– 500 hrs	-	-	-	-	400	0	160	0	80	0	-	-

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 1,007 160 160 160 -	 0 0 0 0 -
Retention Bake	1008	250°C, – 48 hrs – 168 hrs – 500 hrs	 160 160 160	 0 0 0

Table 5A. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001 (E)		M27C1024		M27C2001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	4,339	0	850	0	157	0	1,863	0
		– 168 hrs	720	0	80	0	80	0	400	0
		– 500 hrs	720	0	80	0	80	0	400	0
		– 1000 hrs	720	0	80	0	80	0	400	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	720	0	80	0	80	0	400	0
		– 168 hrs	720	0	80	0	80	0	400	0
		– 500 hrs	720	0	80	0	80	0	400	0
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 5B. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (E)		M27C801		M27C4002		M27C256 M87C257	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	80	0	28,893	0	320	0	4,878	0
		– 168 hrs	80	0	480	0	320	0	720	0
		– 500 hrs	80	0	480	0	320	0	720	0
		– 1000 hrs	80	0	480	0	320	0	720	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	80	0	480	0	320	0	720	0
		– 168 hrs	80	0	480	0	320	0	720	0
		– 500 hrs	80	0	480	0	320	0	720	0
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 6. CMOS E6/0.6µm Process (-10% upgrade) UV EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)		M27C1024		M27C2001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	1,811	0	157	0	157	0	160	0
		– 168 hrs	880	0	80	0	80	0	160	0
		– 500 hrs	880	0	80	0	80	0	160	0
		– 1000 hrs	880	0	80	0	80	0	160	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	880	0	80	0	80	0	160	0
		– 168 hrs	880	0	80	0	80	0	160	0
		– 500 hrs	880	0	80	0	80	0	160	0
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 7. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C160 (F)		M27C800 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	5,180	0	20,064	0	28,093	0
		– 168 hrs	560	0	320	0	560	0
		– 500 hrs	560	0	320	0	560	0
		– 1000 hrs	480	0	240	0	480	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	250°C,						
		– 48 hrs	560	0	160	0	640	0
		– 168 hrs	560	0	160	0	640	0
		– 500 hrs	560	0	160	0	640	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,746 3,746 3,696	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,120	0
Resistance to Solvents	2015	4 Solvent Solutions	248	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	175	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 M87C257		M27C512		M27C1001 (E)		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 168 hrs	240	0	780	0	720	0	324	0
		– 500 hrs	240	0	780	0	720	0	324	0
		– 1000 hrs	240	0	720	0	720	0	324	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	240	0	600	0	600	0	264	0
		– 500 hrs	240	0	600	0	540	0	264	0
		– 1000 hrs	180	0	540	0	540	0	264	0
		– 2000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 9B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (E)		M27C4002		M27C516		M27C4001	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 168 hrs	480	0	60	0	240	0	-	-
		– 500 hrs	480	0	60	0	240	0	-	-
		– 1000 hrs	480	0	60	0	120	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	420	0	60	0	240	0	-	-
		– 500 hrs	420	0	60	0	240	0	-	-
		– 1000 hrs	420	0	60	0	120	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 M87C257		M27C512		M27C1001 (E)		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	240	0	780	0	720	0	144	0
		– 500 hrs	240	0	720	0	720	0	144	0
		– 1000 hrs	240	0	720	0	720	0	144	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	105	0	330	0	280	0	142	0
		– 96 hrs	105	0	330	0	280	0	142	0
		– 168 hrs	-	-	25	0	25	0	-	-
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	240	0	720	0	660	0	324	0
		– 96 hrs	240	0	720	0	660	0	324	0
		– 168 hrs	240	0	720	0	660	0	324	0
		– 240 hrs	240	0	720	0	660	0	324	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	240	0	508	0	600	0	295	0
		– 500 cycles	240	0	508	0	600	0	295	0
		– 1000 cycles	240	0	508	0	600	0	295	0
Solderability			(See cumulative data on Table 10B)							
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs								
Resistance to solvents	2015	4 Solvent Solutions								

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (E)		M27C4002		M27C516		M27C4001	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	480	0	60	0	324	0	-	-
		– 500 hrs	480	0	60	0	324	0	-	-
		– 1000 hrs	480	0	60	0	324	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	210	0	25	0	75	0	-	-
		– 96 hrs	210	0	25	0	75	0	-	-
		– 168 hrs	-	-	-	-	50	0	-	-
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	480	0	60	0	240	0	-	-
		– 96 hrs	480	0	60	0	240	0	-	-
		– 168 hrs	480	0	60	0	180	0	-	-
		– 240 hrs	480	0	60	0	120	0	-	-
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	480	0	60	0	240	0	-	-
		– 500 cycles	480	0	60	0	240	0	-	-
		– 1000 cycles	480	0	60	0	120	0	-	-
Solderability										
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 795/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 120/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 304/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 11. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 720 720 600 -	 0 0 0 -
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 720 720 600 -	 0 0 0 -

Table 12. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 720 720 600 -	 0 0 0 -
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 280 280 25 -	 0 0 0 -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 720 720 720 720	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 600 600 540	 0 0 0
Solderability				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	150	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	-	-
Resistance to solvents	2015	4 Solvent Solutions	52	0

Table 13. CMOS E6DM//0.6µm Process OTP EPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001		M27C800		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 300 300 240 -	 0 0 0 -	 120 120 60 -	 0 0 0 -	 120 120 120 -	 0 0 0 -
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 240 240 180 -	 0 0 0 -	 120 120 60 -	 0 0 0 -	 120 120 120 -	 0 0 0 -

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	300	0	120	0	120	0
		– 500 hrs	240	0	120	0	120	0
		– 1000 hrs	240	0	60	0	120	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	130	0	50	0	55	0
		– 96 hrs	130	0	50	0	55	0
		– 168 hrs	25	0	25	0	-	-
		– 240 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	300	0	120	0	120	0
		– 96 hrs	300	0	120	0	120	0
		– 168 hrs	300	0	120	0	120	0
		– 240 hrs	300	0	60	0	120	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	300	0	120	0	60	0
		– 500 cycles	300	0	120	0	60	0
		– 1000 cycles	240	0	60	0	60	0
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 120/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 50/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 56/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	763	0	300	0	182,603	0	55,952	0
		– 168 hrs	600	0	300	0	1,180	0	660	0
		– 500 hrs	540	0	300	0	1,020	0	660	0
		– 1000 hrs	480	0	300	0	1,020	0	600	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	600	0	300	0	960	0	660	0
		– 500 hrs	540	0	300	0	930	0	660	0
		– 1000 hrs	480	0	300	0	930	0	600	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	376	0	60	0
		– 500 hrs	-	-	-	-	376	0	60	0
		– 1000 hrs	-	-	-	-	376	0	-	-
Write/Erase Cycling		1,000 cycles	4,448	0	3,200	0	21,002	0	21,984	0
		10,000 cycles	-	-	-	-	1,362	0	-	-
Retention Bake	1008	150°C, 36 hrs	4,448	0	3,200	0	19,955	0	21,984	0

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 16. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	600	0	300	0	1,044	0	660	0
		– 500 hrs	480	0	300	0	984	0	600	0
		– 1000 hrs	480	0	300	0	984	0	600	0
		– 2000 hrs	-	-	-	-	-	-		-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	270	0	120	0	552	0	330	0
		– 96 hrs	270	0	120	0	552	0	330	0
		– 168 hrs	270	0	120	0	552	0	330	0
		– 240 hrs	90	0	30	0	222	0	90	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	540	0	300	0	1,044	0	600	0
		– 96 hrs	540	0	300	0	1,044	0	600	0
		– 168 hrs	540	0	300	0	984	0	600	0
		– 240 hrs	480	0	300	0	984	0	600	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	418	0	240	0	1,064	0	660	0
		– 500 cycles	418	0	240	0	1,008	0	660	0
		– 1000 cycles	418	0	240	0	978	0	600	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 450/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 115/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 196/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17A. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 M28F410 M28F420		M28F201		M28F210 M28F211 M28F220	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	27,340	0	44,860	0	114,456	0
		– 168 hrs	420	0	600	0	540	0
		– 500 hrs	420	0	600	0	540	0
		– 1000 hrs	420	0	600	0	480	0
Retention Bake (1)	1008	150°C,						
		– 168 hrs	420	0	600	0	870	0
		– 500 hrs	420	0	600	0	870	0
		– 1000 hrs	420	0	600	0	810	0
Retention Bake	1008	250°C,						
		– 168 hrs	180	0	361	0	-	-
		– 500 hrs	180	0	361	0	-	-
		– 1000 hrs	180	0	361	0	-	-
Write/Erase Cycling		1,000 cycles	4,984	0	6,748	0	11,744	0
		10,000 cycles	344	0	319	0	-	-
		100,000 cycles	252	0	-	-	-	-
		200,000 cycles	-	-	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	4,850	0	6,459	0	11,744	0

Notes:In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 17B. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F040 (B) M29W040		M29F400 (B) M29W400		M29F200 (B) M29F100	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,						
		– 24 hrs	159,641	0	41,190	0	17,040	0
		– 168 hrs	1,290	0	240	0	180	0
		– 500 hrs	1,290	0	240	0	180	0
		– 1000 hrs	1,260	0	180	0	120	0
Retention Bake (1)	1008	150°C,						
		– 168 hrs	1,050	0	240	0	180	0
		– 500 hrs	1,050	0	240	0	180	0
		– 1000 hrs	1,050	0	120	0	120	0
Retention Bake	1008	250°C,						
		– 168 hrs	797	0	222	0	51	0
		– 500 hrs	797	0	222	0	51	0
		– 1000 hrs	797	0	222	0	51	0
Write/Erase Cycling		1,000 cycles	30,256	0	5,114	0	1,793	0
		10,000 cycles	1,036	0	607	0	101	0
		100,000 cycles	781	0	368	0	-	-
		200,000 cycles	63	0	47	0	-	-
Retention Bake	1008	150°C, 36 hrs	29,220	0	4,507	0	1,792	0

Notes:In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 18A. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 M28F410 M28F420		M28F201		M28F211 M28F210 M28F220	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	420	0	600	0	540	0
		– 500 hrs	420	0	600	0	540	0
		– 1000 hrs	420	0	600	0	480	0
		– 2000 hrs	60	0	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	180	0	300	0	270	0
		– 96 hrs	180	0	300	0	270	0
		– 168 hrs	180	0	300	0	270	0
		– 240 hrs	150	0	150	0	30	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	420	0	420	0	600	0
		– 96 hrs	420	0	420	0	600	0
		– 168 hrs	420	0	420	0	600	0
		– 240 hrs	420	0	360	0	540	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	397	0	537	0	583	0
		– 500 cycles	397	0	537	0	583	0
		– 1000 cycles	397	0	537	0	523	0
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-
Solderability								
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	(See cumulative data on Table 18B)					
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 18B)					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking

Table 18B. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M29F040 (B) M29W040		M29F400 (B) M29W400		M29F200 (B) M29F100	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 1,200 1,200 1,140 -	 0 0 0 -	 240 240 120 -	 0 0 0 -	 180 180 120 -	 0 0 0 -
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 600 600 600 150	 0 0 0 0	 120 120 120 -	 0 0 0 -	 90 90 90 -	 0 0 0 -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 1,316 1,316 1,286 1,196	 0 0 0 0	 240 240 180 120	 0 0 0 0	 180 180 180 120	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 1,184 1,184 1,064	 0 0 0	 235 232 112	 0 0 0	 120 120 60	 0 0 0
Thermal Shock	1011	–55 to 125°C, – 100 cycles – 500 cycles	 - -	 - -	 - -	 - -	 - -	 - -
Solderability – TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 535/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 244/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking

Table 19. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93C06C ST93C46C		ST95010		ST95020	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,						
		– 24 hrs	12,380	0	-	-	-	-
		– 168 hrs	1,580	0	-	-	-	-
		– 500 hrs	1,580	0	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	1,050	0	-	-	-	-
		– 500 hrs	1,050	0	-	-	-	-
		– 1000 hrs	1,050	0	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	300	0	-	-	-	-
		1,000,000 cycles	200	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	300	0	-	-	-	-

Table 20. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST93C06C ST93C46C	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 960 960 960 -	 0 0 0 -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 600 600 600 600	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 200 cycles –40 to 150°C, – 500 cycles – 1000 cycles	 650 50 - -	 0 0 - -
Soderability – PDIP Package – SO Package – PLCC Package – TSOP Package	 2003 CECC 90,000	 245°C, 5sec, Precondition Steam, 8hrs 215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	 Cumulative Sample/Fail = -/- Cumulative Sample/Fail = -/- Cumulative Sample/Fail = -/- Cumulative Sample/Fail = -/-	
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-	
Resistance to Surface Mount: – SO Package – TSOP Package			 Cumulative Sample/Fail = -/- Cumulative Sample/Fail = -/-	

Table 21A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,										
		– 24 hrs	16,230	0	5,830	0	9,880	0	6,080	0	-	-
		– 168 hrs	2,430	0	2,030	0	1,080	0	680	0	-	-
		– 500 hrs	2,430	0	2,030	0	1,080	0	680	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,										
		– 168 hrs	1,100	0	700	0	550	0	350	0	-	-
		– 500 hrs	1,100	0	700	0	550	0	350	0	-	-
		– 1000 hrs	1,100	0	700	0	550	0	350	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	450	0	200	0	300	0	100	0	-	-
		1,000,000 cycles	300	0	200	0	100	0	100	0	-	-
Retention Bake	1008	150°C, 168 hrs	450	0	200	0	300	0	100	0	-	-

Table 21B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C16 ST25C16		M93C06		M93C46		M24C16		M28C64D M28C64	
			Samp.	Fail	Samp	Fail	Samp	Fail	Samp	Fail	Samp	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,										
		– 24 hrs	880	0	480	0	880	0	480	0	-	-
		– 168 hrs	80	0	80	0	80	0	80	0	-	-
		– 500 hrs	80	0	80	0	80	0	80	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,										
		– 168 hrs	360	0	-	-	-	-	-	-	5,026	0
		– 500 hrs	360	0	-	-	-	-	-	-	5,026	0
		– 1000 hrs	360	0	-	-	-	-	-	-	5,026	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		50,000 cycles	-	-	-	-	-	-	-	-	-	-
		1,000,000 cycles	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	-	-	-	-	-	-

Table 22A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	1,200	0	1,920	0	420	0	240	0
		– 500 hrs	1,200	0	1,920	0	420	0	240	0
		– 1000 hrs	1,200	0	1,920	0	420	0	240	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	1,150	0	1,400	0	400	0	400	0
		– 96 hrs	1,150	0	1,400	0	400	0	400	0
		– 168 hrs	1,150	0	1,400	0	400	0	400	0
		– 240 hrs	1,150	0	1,400	0	400	0	400	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	1,300	0	1,450	0	450	0	400	0
		– 200 cycles	350	0	300	0	100	0	250	0
		– 1000 cycles	-	-	-	-	-		-	-
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	(See cumulative data on Table 22B)							
– SO Package										
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs								
– TSOP Package										
Resistance to solvents	2015	4 Solvent Solutions	(See cumulative data on Table 22B)							
Resistance to Surface Mount:										
– SO Package			(See cumulative data on Table 22B)							
– TSOP Package										
– PLCC Package										

Table 22B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C16 ST25C16		M28C64 M28C64D		M93C46	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	960	0	-	-	-	-
		– 500 hrs	960	0	-	-	-	-
		– 1000 hrs	960	0	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	1,010	0	3,360	0	100	0
		– 96 hrs	1,010	0	3,360	0	100	0
		– 168 hrs	1,010	0	3,360	0	100	0
		– 240 hrs	1,010	0	3,360	0	100	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	1,010	0	2,880	0	100	0
		– 200 cycles	360	0	240	0	100	0
		– 1000 cycles	360	0	240	0	-	-
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003		Cumulative Sample/Fail = 197/0					
– SO Package		245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 225/0					
– PLCC Package	CECC 90,000		Cumulative Sample/Fail = 250/0					
– TSOP Package		215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 1,280/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 220/0					
Resistance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 10,570/0					
– TSOP Package			Cumulative Sample/Fail = 3,480/0					
– PCC Package			Cumulative Sample/Fail = 925/0					

Table 23. CMOS SPECTRUM/2.0µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 1,932 1,903 1,720	 0 1(a) 0

Note: a. Particle induced gate oxide break down in p-channel of memory cell.

Table 24. CMOS SPECTRUM/2.0µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 828 673 523	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 160 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	76	0

Table 25. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 2,143 1,741 1,387	 1(a) 0 0

Note: Fail a. Mechanical domage on metal 2 write signal.

Table 26. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 905 905 751	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 400 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	72	0

Table 27. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	266	0	2,541	0
		– 500 hrs	266	0	2,521	0
		– 1000 hrs	-	-	1,979	0
		– 2000 hrs	-	-	-	-

Table 28. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -	 308 308 231	 0 0 0
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 66 66 -	 0 0 -	 - - -	 - - -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 345 345 345	 0 0 0	 971 791 631	 0 0 0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 68/0			

Table 29. ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	45	0	40	0
		– 500 hrs	45	0	40	0
		– 1000 hrs	45	0	39	0
		– 2000 hrs	-	-	-	-

Table 30. ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests, April 1997 to March 1998

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 21 21 -	 0 0 -	 42 42 -	 0 0 -
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 21 21 -	 0 0 -	 - - -	 - - -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 47 47 47	 0 0 0	 - - -	 - - -
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-			

Table 31. Statistical Process Control: CMOS E5/0.8μm Process UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	1Q98	4Q97	3Q97	2Q97
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	2.2	1.98	1.85	1.86
Silicon Nitride Thickness	1.7	1.51	1.59	1.60
Field Oxide Thickness	2.61	2.37	2.24	1.47
Gate Oxide Thickness	2.06	1.74	1.34	1.47
Interpoly Oxide Thickness	2.4	2.28	1.77	1.56
Intermediate Dielectric Thickness	1.71	1.97	1.75	1.77
Polysilicon I Thickness	1.91	1.63	1.55	1.48
Active Area Critical Dimensions	2.51	1.43	2.17	1.38
Policide Critical Dimensions	1.6	1.59	1.79	1.59

Key Process Parameters	1Q98	4Q97	3Q97	2Q97
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	1.74	1.44	1.38	1.65
VT P-Channel Square Tr.	2.56	1.84	1.72	1.50
VT Natural Square Tr.	4.74	2.75	3.12	2.97
VT Memory Cell	2.22	1.52	1.41	1.32
I_{DON} N-Channel	3.1	2.48	2.61	2.23
N+ Active Area Contact Chain	9.67	7.37	6.60	5.92
AL-W Silicide Contact Chain Resistance	5.99	3.38	2.98	2.86

(*) One side limit only.

Table 32. Statistical Process Control: CMOS E6DM/0.6µm Process UV EPROM and OTP EPROM, Phoenix - USA PF1 Diffusion Line

Key Process Parameters	1Q98	4Q97		
	CPK	CPK	CPK	CPK
Pad Oxide Thickness	1.97	1.71		
Silicon Nitride Thickness	1.63	1.46		
Field Oxide Thickness	2.86	2.49		
Gate Oxide Thickness	2.18	2.69		
Interpoly Oxide Thickness	1.35	1.44		
Intermediate Dielectric Thickness	1.34	1.35		
Polysilicon I Thickness	4.56	6.21		
Active Area Critical Dimensions	2.34	2.24		
Policide Critical Dimensions	2.64	2.35		

Key Process Parameters	1Q98	4Q97		
	CPK	CPK	CPK	CPK
VT N-Channel Square Tr.	3.09	3.26		
VT P-Channel Square Tr.	1.67	1.64		
VT Natural Square Tr.	3.92	3.99		
VT Memory Cell	1.61	1.36		
I_{DON} N-Channel	1.73	1.44		
N+ Active Area Contact Chain	4.61	5.02		
AL-W Silicide Contact Chain Resistance	1.59	1.33		

Table 33. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	1Q98	4Q97	3Q97	
	CPK	CPK	CPK	CPK
Field Oxide Thickness	2.15	2.25	2.33	
Polysilicon I Thickness	2.96	2.65	2.89	
Gate Oxide Thickness (1)	1.82	1.87	1.28	
Tunnel Oxide Thickness	2.23	2.35	2.23	
ONO Bottom Oxide Thickness	2.22	1.44	1.50	
ONO Nitride Thickness	1.92	1.66	1.66	
ONO Top Oxide Thickness	2.67	2.41	3.22	
Active Area Critical Dimensions	2.96	1.54	1.50	
Polysilicon II Critical Dimensions	1.69	1.63	1.92	

Notes:1. Exhaust problems (progressive obstruction) solved in week 45 by rebuilding part of the exaust, to avoid this problems detectors have been installed.

Key Process Parameters	1Q98	4Q97	3Q97	
	CPK	CPK	CPK	CPK
VT N-Channel 25 x 25 µm	2.77	2.42	2.06	
VT P-Channel 25 x 25 µm	1.69	1.54	1.75	
BV N-Channel 25 x 0.8 µm	1.63	3.23	4.75	
BV P-Channel 25 x 0.9 µm	3.68	3.87	3.00	
VT Memory Cell 0.8 x 0.8 µm	1.36	1.87	1.78	
I_{DON} N-Channel 25 x 0.8 µm	2.02	2.00	2.23	
Al+N+ Contact Chain	4.58	3.86	3.93	
AL-W Silicide Contact Chain Resistance	1.81	4.07	4.01	

Table 34. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	1Q 98/4Q 97 (2)		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	-	-	1.65	1.60	1.69	1.67	2.01	1.96
Polysilicon I Thickness (1)	-	-	1.22	1.14	1.35	1.25	1.20	1.16
Gate Oxide Thickness	-	-	1.78	1.55	1.94	1.78	1.91	1.83
Tunnel Oxide Thickness	-	-	2.04	1.86	1.77	1.65	1.91	1.87
ONO Bottom Oxide hickness	-	-	1.46	1.44	1.42	1.39	1.55	1.49
ONO Nitride Thickness	-	-	1.59	1.52	1.66	1.60	1.52	1.49
ONO Top Oxide Thickness	-	-	2.02	2.02	1.58	1.57	1.93	1.86
Active Area Critical Dimensions	-	-	1.39	1.34	1.63	1.38	1.64	1.64
Polysilicon II Critical Dimensions	-	-	1.38	1.33	1.36	1.36	1.60	1.51

Notes: 1. The furnace temperature control system alignment is going to be implemented.
2. No production.

Key Process Parameters	1Q 98/4Q 97 (1)		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	-	-	1.63	1.36	1.66	1.52	1.74	1.36
VT P-Channel 25 x 25 µm	-	-	1.59	1.42	1.51	1.48	1.45	1.41
BV N-Channel 25 x 0.8 µm	-	-	2.15	1.82	1.59	1.39	1.92	1.45
BV P-Channel 25 x 0.9 µm	-	-	3.25	2.48	2.42	1.84	4.36	3.31
VT Memory Cell 0.8 x 0.8 µm	-	-	1.70	1.66	2.19	1.73	1.51	1.43
I_{DON} N-Channel 25 x 0.8 µm	-	-	2.45	2.12	1.53	1.49	1.80	1.60
Al+N+ Contact Chain	-	-	4.19	3.12	2.43	1.48	4.45	2.72
Al-W Silicide Contact Chain Resistance	-	-	3.62	3.01	2.83	2.31	1.98	1.70

Note: 1. No production.

Table 35A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	1Q 98	4Q 97	3Q 97	2Q 97
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.77	1.59	1.42	1.67
First Poly Thickness	1.04 (2)	1.46	1.19 (1)	1.39
Gate Oxide HV Thickness	2.48	1.69	1.83	1.78
Tunnel Oxide Thickness	1.92	2.36	1.64	1.65
Gate Oxide LV Thickness	1.94	1.49	1.37	1.44
ONO Bottom Oxide Thickness (3)	1.33	1.15	1.45	1.55
ONO Nitride Thickness	1.88	1.35	1.49	1.60
ONO Top Oxide Thickness	1.90	1.78	1.68	1.44
Active Area CD	2.15	1.66	1.49	1.40
Second Poly CD	1.35	1.38	1.43	1.62

Notes: 1. The furnace temperature control system alignment is going to be implemented.
2. The low value of CPK is due to low run uniformity on 2 furnace. A modification of hardware has been done on the furnace with good results. At the end of this month the same modification will be done also on the other furnace.
3. The recipe has been transferred from tubes with atmoscan to tubes with cantilever. We had a deterioration of thickness uniformity along the load. Tests have been completed to evaluate the possibility to transfer the recipe in a vertical tube allowing much better thickness control. This evaluation was completed and the process has been loaded on the Vtube starting from the end of January. We are confident to recover this value within the 1Q 98.

Table 35B. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	1Q 98	4Q 97	3Q 97	2Q 97
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	3.42	2.82	2.20	1.97
LV-PCh LVS (10 x 0.9) BV	3.10	2.55	2.55	3.09
LV-PCh LVS (10 x 0.9) Saturation Current	1.68	1.85	1.94	2.08
LV-PCh SQ. VTh	1.68	1.54	1.39	1.41
HV-NCh (10 x 1.2) LVS BV	2.02	2.32	1.59	1.99
HV-NCh SQ. VTh	1.82	1.66	1.61	1.65
HV-NCh (10 x 1.2) LVS Saturation Current	2.38	2.26	2.45	2.57
HV-PCh (10 x 1.3) BV	2.61	3.18	2.18	2.79
HV-PCh (10 x 1.3) Saturation Current	2.02	2.51	1.90	1.51
HV-PCh SQ. VTh (1)	1.33	1.20	1.37	1.37
UV Erased Cell VTh	1.64	1.43	1.35	1.40
N+ Contact Chain	1.67	1.84	2.00	2.04
Silicide Contact Chain	2.08	1.96	2.32	2.96
LV-NCh (10 x 0.8) BV	3.28	5.31	2.18	1.94

Note: 1. The problem is correlated with a tail of transistor dose implant that pass through the poly 1. We have already implemented a Poly implant energy modification, but this change is not sufficient to solve the problem. A trial is going to be issued to evaluate the change of poly1 thickness.

Table 36A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Process Parameters	1Q98	4Q97		
	CPK	CPK	CPK	CPK
Field Oxide Thickness	1.85	1.91		
First Poly Thickness	1.49	1.51		
Gate Oxide HV Thickness (1)	1.34	1.21		
Tunnel Oxide Thickness	1.84	1.80		
Gate Oxide LV Thickness	1.33	1.36		
ONO Bottom Oxide Thickness	1.33	1.54		
ONO Nitride Thickness	1.78	2.09		
ONO Top Oxide Thickness	2.3	2.05		
Active Area CD	1.79	1.33		
Second Poly CD	1.47	1.50		

Note: 1. Process alignment is running.

Table 36B. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Process Parameters	1Q98	4Q97		
	CPK	CPK	CPK	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	5.77	2.54		
LV-PCh LVS (10 x 0.9) BV	2.61	1.35		
LV-PCh LVS (10 x 0.9) Saturation Current	1.67	2.00		
LV-PCh SQ. VTh	1.78	1.53		
HV-NCh (10 x 1.2) LVS BV	1.57	1.49		
HV-NCh SQ. VTh (1)	0.98	1.45		
HV-NCh (10 x 1.2) LVS Saturation Current	4.15	2.35		
HV-PCh (10 x 1.3) BV	2.31	1.62		
HV-PCh (10 x 1.3) Saturation Current	4.38	1.73		
HV-PCh SQ. VTh	1.44	1.38		
UV Erased Cell VTh	1.68	1.55		
N+ Contact Chain	3.84	3.84		
Silicide Contact Chain (2)	0.92	1.36		
LV-NCh (10 x 0.8) BV	2.27	2.32		

Note: 1. Low CPK due to ox tunnel equipment, now replaced.
2 Low CPK due to one w deposition chamber equipment adjustment in progress.

Table 37. Statistical Process Control: UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	1Q 98	4Q 97	3Q 97	2Q 97
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	16.11	40.18	37.14	45.75
Stud Pull	1.67	1.40	1.71	1.35
Bond Strength (W.B.)	5.67	5.50	5.29	4.01
SN Thickness (Tin Plate)	1.71	1.39	1.48	1.58

Table 38. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	1Q 98	4Q 97	3Q 97	2Q 97
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	1.78	2.24	3.13	2.13
Ball Shear (W.B.)	2.00	2.07	1.89	2.54
Bond Strength (W.B.)	1.88	1.85	1.57	1.86
Coplanarity	2.83	2.53	3.55	4.06
Plating Thickness	2.24	2.17	2.00	1.47

Table 39. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	1Q 98	4Q 97	3Q 97	2Q 97
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.22	3.30	4.18	3.46
Ball Shear (W.B.)	2.13	2.09	2.05	1.88
Bond Strength (W.B.)	1.49	1.52	1.62	1.47
Plating Thickness	2.14	2.85	3.56	2.77