APPLICATION NOTE

NOTES ON USING THE ST623XB/ST628XB UART

by 8-bit Micro Application Team

1 AVOIDING A SPURIOUS INTERRUPT DURING RESET

Care must be taken if during RESET, the reception RXD/PD4 line is stuck at zero. In this case, a high-to-low transition will be latched inside the UART cell due to the RESET structure, even if no real falling edge occured on RXD/PD4 line. This active falling edge will be acknowledged by the UART cell as a valid receive start bit. 88 UART clocks (8 clocks per bit) are then needed to receive one burst of 11 bits (1 start bit + 8 bit data + 1 parity bit + 1 stop bit). The Receive Interrupt flag RXRDY (bit7 of UART Control Register) is set to 1 after all 11 bits have been received and if enabled, a Receive interrupt is generated. To avoid this early UART interrupt, enabling of the UART receive interrupt should ONLY occur after a software delay sequence insterted just after the RESET jump instruction. The RXRDY flag must also be cleared before or when enabling UART Receive Interrupt for the first time. The length of the time delay depends on the selected operating Baud rate (bit BR2..BR0 of UART Control Register). The following tables show the required timing with respect to the selected baud rate:

BR2	BR1	BR0	F_{OSC} division	F_{OSC}=8MHz	Time Delay Required
0.00	0.00	0.00	6656	1200	9.6ms
0.00	0.00	1.00	3328	2400	4.8ms
0.00	1.00	0.00	1664	4800	2.4ms
0.00	1.00	1.00	832	9600	1.2ms
1.00	0.00	0.00	416	19200	600µs
1.00	0.00	1.00	256	31200	400µs
1.00	1.00	0.00	208	38400	300µs
1.00	1.00	1.00	RESERVED	RESERVED	RESERVED

BR2	BR1	BR0	F_{OSC} division	F_{OSC}=4MHz	Time Delay Required
0.00	0.00	0.00	6656	600	19.2ms
0.00	0.00	1.00	3328	1200	9.6ms
0.00	1.00	0.00	1664	2400	4.8ms
0.00	1.00	1.00	832	4800	2.4ms
1.00	0.00	0.00	416	9600	1.2ms
1.00	0.00	1.00	256	15600	740µs
1.00	1.00	0.00	208	19200	600µs
1.00	1.00	1.00	RESERVED	RESERVED	RESERVED

The following delay loop sequence is proposed :

```
Reset  ldi Uartcr, 0Ch ; Select the faster Baud rate (Uart control reg.)
       ldi count, 03h; for count = 01h, the tempo takes approximately
       call tempo; 100us. In this example, time out is for 300us
       ; at FOSC = 8MHz
Start  ldi Uartcr, 30h; Now clear RXRDY flag (bit7) and can enable
       ; UART interrupts
       ... ...


tempo  ld A, count; total temporisation: 62cyc*count + 8cyc + 8cyc
       jrz endtemp
loop1  ldi X, 08h
loop2  dec X; Ex: need 62cyc for 100us at FOSC = 8Mhz
       jrnz loop2
       dec count
       nop
       nop
       jrnz loop1
endtempret


.org 0FFEh
jp Reset
```

IMPORTANT NOTES:

The configuration (BR2=1, BR1=1, BR0=0) for a faster baud rate should be chosen after reset in order to use a short time delay.

This early UART receive interrupt feature can be used to detect after reset if the RXD/PD4 line is low (stuck at '0') or not.