SGS-THOMSON MICROELECTRONICS

QRR9704
QUALITY & RELIABILITY REPORT

January 1997 to December 1997- EPROM, FLASH Memory, EEPROM and NVRAM Products

INTRODUCTION

ST Microelectronics manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; Flash memories in 1.2 to 0.6µ CMOS technology; OTP EPROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAM: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.8µ HCMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from January 1997 to December 1997. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Attilio PANCHIERI

CONTENT

Table 1. Final Average Outgoing Quality (AOQ), January 1997 to December 1997

Process	Electrical ppm				Visual ppm			
	3Q97	2Q97	1Q97	4Q97	3Q97	2Q97	1Q97	4Q97
UV EPROM								
CMOS	17	19	17	19	15	12	16	11
NMOS	0	0	0	0	20	0	18	0
OTP EPROM								
CMOS	18	20	19	18	14	6	7	11
FLASH								
CMOS	0	4	17	0	5	4	0	10
NVRAM								
CMOS	0	0	0	0	4	4	3	5
EEPROM								
CMOS	1	1	3	2	4	5	9	6

Table 2. Failure Rate Predictions (Fit), January 1997 to December 1997

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C (x 10^6)	Life Test Failure	Failure rate (Fit) Confidence Level	
	Dev. hrs (x 10^6)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -35%	4.72	140	0.6	4.0	1,295	0	0.7	1.8
CMOS E6 - DM	3.83	140	0.6	4.0	1,051	0	0.9	2.1
OTP EPROM								
CMOS E5 -35%	1.85	140	0.6	4.0	481	0	1.9	4.8
FLASH								
CMOS T5 -20%	8.83	140	0.6	4.0	2,289	0	0.4	1.0
CMOS T6	10.8	140	0.6	4.6	2,802	0	0.3	0.8
NVRAM								
CMOS Spectrum	1.58	100	0.7	64	2,030	0	0.4	1.1
HCMOS S3	1.64	100	0.7	64	2,102	1	0.9	1.8
HCMOS 4DZ	2.25	125	0.7	6.0	1,038	0	0.9	2.2
EEPROM								
CMOS F4	1.19	140	0.6	3.0	279	0	3.2	8.2
CMOS F4S	4.31	140	0.6	3.0	1,014	0	0.9	2.3

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	-	-	-	-	402	0	644	0	160	0	-	-
		– 168 hrs	-	-	-	-	402	0	644	0	160	0	-	-
		– 500 hrs	-	-	-	-	320	0	328	0	160	0	-	-
		– 1000 hrs	-	-	-	-	320	0	328	0	160	0	-	-
Retention Bake	1008	250°C,												
		– 48 hrs	-	-	-	-	356	0	350	0	80	0	-	-
		– 168 hrs	-	-	-	-	356	0	350	0	80	0	-	-
		– 500 hrs	-	-	-	-	356	0	350	0	80	0	-	-

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	619	0
		– 168 hrs	80	0
		– 500 hrs	90	0
		– 1000 hrs	80	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	160	0
		– 168 hrs	160	0
		– 500 hrs	160	0

Table 5A. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001 (E)		M27C1024		M27C2001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	4,768	0	1,004	0	157	0	2,941	0
		– 168 hrs	918	0	80	0	80	0	400	0
		– 500 hrs	688	0	80	0	80	0	400	0
		– 1000 hrs	608	0	80	0	80	0	400	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	704	0	80	0	80	0	400	0
		– 168 hrs	704	0	80	0	80	0	400	0
		– 500 hrs	704	0	80	0	80	0	400	0
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 5B. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (E)		M27C801		M27C4002		M27C256 M87C257	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	80	0	28,336	0	741	0	4,502	0
		– 168 hrs	80	0	616	0	664	0	652	0
		– 500 hrs	80	0	336	0	384	0	592	0
		– 1000 hrs	80	0	336	0	384	0	512	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	80	0	588	0	392	0	596	0
		– 168 hrs	80	0	588	0	392	0	596	0
		– 500 hrs	80	0	588	0	392	0	596	0
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 6. CMOS E6/0.6µm Process (-10% upgrade) UV EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 1,567 720 720 640 -	 0 0 0 0 -
Retention Bake	1008	250°C, – 48 hrs – 168 hrs – 500 hrs – 1000 hrs	 720 720 720 -	 0 0 0 -

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 7. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C160 (F)		M27C800 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	6,457	0	23,440	0	28,037	0
		– 168 hrs	480	0	344	0	432	0
		– 500 hrs	400	0	344	0	432	0
		– 1000 hrs	320	0	344	0	352	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	250°C,						
		– 48 hrs	480	0	358	0	516	0
		– 168 hrs	480	0	358	0	516	0
		– 500 hrs	400	0	358	0	516	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,408 3,408 2,910	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,180	0
Resistance to Solvents	2015	4 Solvent Solutions	244	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	175	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 M87C257		M27C512		M27C1001 (E)		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 168 hrs	180	0	660	0	699	0	339	0
		– 500 hrs	180	0	660	0	639	0	339	0
		– 1000 hrs	180	0	600	0	639	0	339	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	180	0	480	0	579	0	279	0
		– 500 hrs	180	0	480	0	459	0	279	0
		– 1000 hrs	120	0	420	0	459	0	279	0
		– 2000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 9B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (E)		M27C4002		M27C516		M27C4001	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 168 hrs	543	0	84	0	300	0	15	0
		– 500 hrs	543	0	84	0	300	0	15	0
		– 1000 hrs	423	0	84	0	300	0	15	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	423	0	84	0	300	0	15	0
		– 500 hrs	423	0	84	0	300	0	15	0
		– 1000 hrs	363	0	84	0	300	0	15	0
		– 2000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 M87C257		M27C512		M27C1001 (E)		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	180	0	660	0	699	0	339	0
		– 500 hrs	180	0	600	0	639	0	339	0
		– 1000 hrs	180	0	600	0	639	0	339	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	75	0	280	0	270	0	150	0
		– 96 hrs	75	0	280	0	270	0	150	0
		– 168 hrs	-	-	-	-	25	0	-	-
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	180	0	600	0	699	0	180	0
		– 96 hrs	180	0	600	0	699	0	180	0
		– 168 hrs	180	0	600	0	639	0	180	0
		– 240 hrs	180	0	600	0	639	0	180	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	180	0	588	0	579	0	310	0
		– 500 cycles	180	0	588	0	579	0	310	0
		– 1000 cycles	180	0	588	0	579	0	310	0
Solderability			See cumulative data on Table 10B							
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs								
Resistance to solvents	2015	4 Solvent Solutions								

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 10B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (E)		M27C4002		M27C516		M27C4001	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	483	0	84	0	300	0	15	0
		– 500 hrs	423	0	84	0	300	0	15	0
		– 1000 hrs	423	0	84	0	300	0	15	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	217	0	37	0	265	0	8	0
		– 96 hrs	217	0	37	0	265	0	8	0
		– 168 hrs	-	-	-	-	265	0	-	-
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	483	0	84	0	300	0	15	0
		– 96 hrs	483	0	84	0	300	0	15	0
		– 168 hrs	483	0	84	0	300	0	15	0
		– 240 hrs	423	0	84	0	300	0	15	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	444	0	75	0	300	0	15	0
		– 500 cycles	444	0	75	0	300	0	15	0
		– 1000 cycles	384	0	75	0	300	0	15	0
Solderability										
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 815/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 125/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 344/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 11. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 540 540 480 -	 0 0 0 -
Retention Bake	1008	150°C, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 540 540 480 -	 0 0 0 -

Table 12. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	540	0
		– 500 hrs	540	0
		– 1000 hrs	480	0
		– 2000 hrs	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,		
		– 48 hrs	205	0
		– 96 hrs	205	0
		– 168 hrs	-	-
		– 240 hrs	-	-
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	540	0
		– 96 hrs	540	0
		– 168 hrs	540	0
		– 240 hrs	480	0
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	420	0
		– 500 cycles	420	0
		– 1000 cycles	360	0
Solderability				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	125	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	-	-
Resistance to solvents	2015	4 Solvent Solutions	48	0

Table 13. CMOS E6DM//0.6µm Process OTP EPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001		M27C800		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 168 hrs	180	0	60	0	120	0
		– 500 hrs	180	0	-	-	60	0
		– 1000 hrs	180	0	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	150°C,						
		– 168 hrs	120	0	60	0	120	0
		– 500 hrs	120	0	-	-	60	0
		– 1000 hrs	120	0	-	-	60	0
		– 2000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 14. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C800		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	180	0	60	0	120	0
		– 500 hrs	180	0	-	-	60	0
		– 1000 hrs	180	0	-	-	60	0
		– 2000 hrs	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	80	0	-	-	25	0
		– 96 hrs	80	0	-	-	25	0
		– 168 hrs	-	-	-	-	-	-
		– 240 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	180	0	-	-	60	0
		– 96 hrs	180	0	-	-	60	0
		– 168 hrs	180	0	-	-	60	0
		– 240 hrs	180	0	-	-	60	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	180	0	-	-	-	-
		– 500 cycles	180	0	-	-	-	-
		– 1000 cycles	180	0	-	-	-	-
Solderability								
– PLCC/TSOP Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 100/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 25/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 40/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	583	0	278	0	218,476	0	64,224	0
		– 168 hrs	420	0	240	0	1,044	0	587	0
		– 500 hrs	420	0	240	0	944	0	527	0
		– 1000 hrs	360	0	240	0	854	0	527	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	480	0	300	0	930	0	597	0
		– 500 hrs	480	0	300	0	930	0	537	0
		– 1000 hrs	420	0	300	0	870	0	537	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	134	0	60	0
		– 500 hrs	-	-	-	-	134	0	60	0
		– 1000 hrs	-	-	-	-	134	0	-	-
Write/Erase Cycling		1,000 cycles	4,347	0	4,315	0	23,384	0	19,195	0
		10,000 cycles	-	-	-	-	1,275	0	-	-
Retention Bake	1008	150°C, 36 hrs	4,347	0	4,315	0	22,460	0	19,195	0

Notes:In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 16. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	480	0	300	0	957	0	594	0
		– 500 hrs	480	0	300	0	957	0	534	0
		– 1000 hrs	420	0	300	0	837	0	534	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	240	0	150	0	510	0	298	0
		– 96 hrs	240	0	150	0	510	0	298	0
		– 168 hrs	240	0	150	0	510	0	298	0
		– 240 hrs	180	0	120	0	450	0	298	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	300	0	180	0	480	0	300	0
		– 96 hrs	300	0	180	0	480	0	300	0
		– 168 hrs	300	0	180	0	420	0	300	0
		– 240 hrs	240	0	180	0	360	0	300	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	418	0	300	0	957	0	589	0
		– 500 cycles	358	0	300	0	957	0	529	0
		– 1000 cycles	358	0	300	0	957	0	414	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability										
– TSOP/PLCC Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 475/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 125/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 204/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 M28F410 M28F420		M29F040 M29W040		M28F201		M28F210 M28F211 M28F220	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V,f = 500kHz,								
		– 24 hrs	49,809	0	138,748	0	60,390	0	81,514	0
		– 168 hrs	857	0	1,230	0	624	0	300	0
		– 500 hrs	857	0	1,230	0	624	0	300	0
		– 1000 hrs	857	0	1,170	0	564	0	300	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	997	0	1,205	0	620	0	444	0
		– 500 hrs	997	0	1,205	0	620	0	444	0
		– 1000 hrs	997	0	1,205	0	560	0	444	0
Retention Bake	1008	250°C,								
		– 168 hrs	545	0	178	0	361	0	-	-
		– 500 hrs	545	0	178	0	361	0	-	-
		– 1000 hrs	545	0	178	0	361	0	-	-
Write/Erase Cycling		1,000 cycles	11,053	0	27,780	0	8,660	0	9,435	0
		10,000 cycles	606	0	849	0	445	0	-	-
		100,000 cycles	192	0	329	0	64	0	-	-
		200,000 cycles	-	-	128	0	-	-	-	-
Retention Bake	1008	150°C, 36 hrs	10,928	0	28,136	0	8,245	0	9,435	0

Notes:In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 18. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 M28F410 M28F420		M29F040 M29W040		M28F201		M28F211 M28F210 M28F220	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	852	0	1,173	0	624	0	300	0
		– 500 hrs	852	0	1,113	0	624	0	300	0
		– 1000 hrs	852	0	1,113	0	564	0	300	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	398	0	562	0	342	0	150	0
		– 96 hrs	398	0	562	0	342	0	150	0
		– 168 hrs	398	0	562	0	342	0	150	0
		– 240 hrs	368	0	382	0	222	0	30	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	852	0	1,175	0	624	0	444	0
		– 96 hrs	852	0	1,175	0	624	0	444	0
		– 168 hrs	852	0	1,175	0	624	0	444	0
		– 240 hrs	852	0	1,175	0	624	0	444	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	829	0	996	0	561	0	367	0
		– 500 cycles	829	0	936	0	501	0	367	0
		– 1000 cycles	829	0	936	0	501	0	367	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability										
– TSOP/SO Packages	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 415/0							
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 192/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking

Table 19. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C02 ST24W02		ST24C08		ST93C06C ST93C46C		ST95010		ST95020	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,										
		– 24 hrs	-	-	-	-	13,800	0	-	-	-	-
		– 168 hrs	-	-	-	-	1,800	0	-	-	-	-
		– 500 hrs	-	-	-	-	1,800	0	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,										
		– 168 hrs	-	-	-	-	1,200	0	-	-	-	-
		– 500 hrs	-	-	-	-	1,200	0	-	-	-	-
		– 1000 hrs	-	-	-	-	1,200	0	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	-	-	-	-	600	0	-	-	-	-
		1,000,000 cycles	-	-	-	-	200	0	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	600	0	-	-	-	-

Table 20. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C02 ST24W02		ST24C08		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	-	-	-	-	1,700	0
		– 500 hrs	-	-	-	-	1,700	0
		– 1000 hrs	-	-	-	-	1,700	0
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	-	-	-	-	1,200	0
		– 96 hrs	-	-	-	-	1,200	0
		– 168 hrs	-	-	-	-	600	0
		– 240 hrs	-	-	-	-	600	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	-	-	-	-	150	0
		– 200 cycles	-	-	-	-	-	-
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Soderability								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = -/-					
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = -/-					
– PLCC Package			Cumulative Sample/Fail = -/-					
– TSOP Package			Cumulative Sample/Fail = -/-					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-					
Resistance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = -/-					
– TSOP Package			Cumulative Sample/Fail = -/-					

Table 21. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24LC21		ST24C16 ST25C16		ST24E32 ST25E32	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,														
		– 24 hrs	15,200	0	8,350	0	10,600	0	8,750	0	-	-	-	-	-	-
		– 168 hrs	2,200	0	2,350	0	1,600	0	750	0	-	-	-	-	-	-
		– 500 hrs	2,200	0	2,350	0	1,600	0	750	0	-	-	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,														
		– 168 hrs	1,000	0	800	0	700	0	350	0	-	-	360	0	-	-
		– 500 hrs	1,000	0	800	0	700	0	350	0	-	-	360	0	-	-
		– 1000 hrs	1,000	0	800	0	700	0	350	0	-	-	360	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	450	0	500	0	800	800	300	0	-	-	-	-	-	-
		1,000,000 cycles	300	0	200	0	100	100	100	0	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	450	0	500	0	800	800	300	0	-	-	-	-	-	-

Table 22A. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	1,140	0	1,980	0	660	0	300	0
		– 500 hrs	1,140	0	1,980	0	660	0	300	0
		– 1000 hrs	1,140	0	1,980	0	660	0	300	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	1,000	0	1,300	0	550	0	250	0
		– 96 hrs	1,000	0	1,300	0	550	0	250	0
		– 168 hrs	1,000	0	1,300	0	550	0	250	0
		– 240 hrs	1,000	0	1,300	0	550	0	250	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	200	0	50	0	-	-	100	0
		– 200 cycles	200	0	50	0	-	-	100	0
		– 1000 cycles	-	-	-	-	-	-	-	-
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability			See cumulative data on Table 22B							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hrs								
– SO Package										
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hrs								
– TSOP Package										
Resistance to solvents	2015	4 Solvent Solutions								
Resistance to Surface Mount:										
– SO Package										
– TSOP Package										
– PCC Package										

Table 22B. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24E32 ST25E32		ST24C16 ST25C16		M28C64	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	-	-	1,020	0	-	-
		– 500 hrs	-	-	1,020	0	-	-
		– 1000 hrs	-	-	1,020	0	-	-
		– 2000 hrs	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	400	0	1,010	0	2,760	0
		– 96 hrs	400	0	1,010	0	2,760	0
		– 168 hrs	400	0	1,010	0	2,760	0
		– 240 hrs	400	0	1,010	0	2,760	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	-	-	360	0	2,640	0
		– 200 cycles	-	-	360	0	240	0
		– 1000 cycles	-	-	360	0	-	-
		–40 to 150°C,						
		– 500 cycles	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-
Solderability								
– PDIP Package	2003		Cumulative Sample/Fail = 244/0					
– SO Package		245°C, 5sec, Precondition Steam, 8hrs	Cumulative Sample/Fail = 248/0					
– PLCC Package	CECC 90,000		Cumulative Sample/Fail = 175/0					
– TSOP Package		215°C, 3sec, Precondition Dry Air, 150°C, 16hrs	Cumulative Sample/Fail = 1,280/0					
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 204/0					
Resistance to Surface Mount:								
– SO Package			Cumulative Sample/Fail = 7,950/0					
– TSOP Package			Cumulative Sample/Fail = 3,330/0					
– PCC Package			Cumulative Sample/Fail = 565/0					

Table 23. CMOS SPECTRUM/2.0µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 2,044 1,649 1,390	 0 0 0

Table 24. CMOS SPECTRUM/2.0µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 585 363 286	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 158 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	72	0

Table 25. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f = 1MHz, – 168 hrs – 500 hrs – 1000 hrs	 2,148 1,754 1,398	 1(a) 0 0

Note: Fail a. Mechanical domage on metal 2 write signal.

Table 26. HCMOS S3/1.2µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 875 798 644	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 160 - -	 0 - -
Resistance to solvents	2015	4 Solvent Solutions	68	0

Table 27. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	266	0	2,533	0
		– 500 hrs	266	0	1,977	0
		– 1000 hrs	266	0	1,801	0
		– 2000 hrs	-	-	-	-

Table 28. HCMOS 4DZ/0.8µm Process ZEROPOWER NVRAM Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y M48T559Y	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -	 - - -	 - - -
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 66 66 -	 0 0 -	 - - -	 - - -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 345 345 345	 0 0 0	 798 718 638	 0 0 0
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 60/0			

Table 29. ZEROPOWER HYBRID MODULE Reliability Data, Die Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f = 1MHz,				
		– 168 hrs	45	0	40	0
		– 500 hrs	45	0	40	0
		– 1000 hrs	45	0	40	0
		– 2000 hrs	-	-	-	-

Table 30. ZEROPOWER HYBRID MODULE Reliability Data, Package Related Tests, January 1997 to December 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48Z512A M48Z2M1		M48Z128 M48Z30	
			Samp.	Fail	Samp.	Fail
Temperature,Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 21 21 -	 0 0 -	 20 20 -	 0 0 -
Hast	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs – 240 hrs	 21 21 -	 0 0 -	 - - -	 - - -
Temperature Cycling	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 47 47 47	 0 0 0	 - - -	 - - -
Resistance to solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-			

Table 31. Statistical Process Control: CMOS E5/0.8μm Process UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	4Q 97		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	2.00	1.98	2.01	1.85	1.95	1.86	1.86	1.84
Silicon Nitride Thickness	1.62	1.51	1.60	1.59	1.60	1.60	1.54	1.52
Field Oxide Thickness	2.50	2.37	2.38	2.24	1.52	1.47	1.98	1.96
Gate Oxide Thickness	1.82	1.74	1.46	1.34	1.51	1.47	1.46	1.46
Interpoly Oxide Thickness	2.31	2.28	1.84	1.77	1.66	1.56	1.62	1.61
Intermediate Dielectric Thickness	1.99	1.97	1.82	1.75	1.80	1.77	1.90	1.86
Polysilicon I Thickness	1.74	1.63	1.63	1.55	1.49	1.48	1.34	1.33
Active Area Critical Dimensions	1.56	1.43	2.24	2.17	1.39	1.38	1.83	1.68
Policide Critical Dimensions	1.76	1.59	1.81	1.79	1.59	1.59	1.95	1.61

Key Process Parameters	4Q 97		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel Square Tr.	2.22	1.44	1.92	1.38	2.15	1.65	2.20	1.72
VT P-Channel Square Tr.	2.53	1.84	2.48	1.72	1.52	1.50	2.07	1.32
VT Natural Square Tr.	3.24	2.75	3.46	3.12	3.23	2.97	3.52	3.28
VT Memory Cell	1.67	1.52	1.52	1.41	1.68	1.32	1.53	1.50
I_{DON} N-Channel	2.60	2.48	2.65	2.61	2.31	2.23	2.49	2.40
N+ Active Area Contact Chain	(*)	7.37	(*)	6.60	(*)	5.92	(*)	2.85
AL-W Silicide Contact Chain Resistance	(*)	3.38	(*)	2.98	(*)	2.86	(*)	2.27

(*) One side limit only.

Table 32. Statistical Process Control: CMOS E5/0.8µm Process UV EPROM and OTP EPROM, Phoenix - USA PF1 Diffusion Line

Key Process Parameters	4Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	1.71	1.71						
Silicon Nitride Thickness	1.58	1.46						
Field Oxide Thickness	2.66	2.49						
Gate Oxide Thickness	2.69	2.69						
Interpoly Oxide Thickness	1.44	1.44						
Intermediate Dielectric Thickness	1.42	1.36						
Polysilicon I Thickness	6.36	6.21						
Active Area Critical Dimensions	2.90	2.03						
Policide Critical Dimensions	2.39	2.29						

Key Process Parameters	4Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel Square Tr.	2.29	2.18						
VT P-Channel Square Tr.	1.89	1.40						
VT Natural Square Tr.	2.86	2.55						
VT Memory Cell	1.53	1.34						
I_{DON} N-Channel	3.60	3.18						
N+ Active Area Contact Chain	6.19	5.99						
AL-W Silicide Contact Chain Resistance	4.21	3.22						

Table 33. Statistical Process Control: CMOS E6DM/0.6µm Process UV EPROM and OTP EPROM, Phoenix - USA PF1 Diffusion Line

Key Process Parameters	4Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	1.71	1.71						
Silicon Nitride Thickness	1.58	1.46						
Field Oxide Thickness	2.66	2.49						
Gate Oxide Thickness	2.69	2.69						
Interpoly Oxide Thickness	1.44	1.44						
Intermediate Dielectric Thickness	1.38	1.35						
Polysilicon I Thickness	6.36	6.21						
Active Area Critical Dimensions	2.53	2.24						
Policide Critical Dimensions	2.49	2.35						

Key Process Parameters	4Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel Square Tr.	3.70	3.26						
VT P-Channel Square Tr.	2.82	1.64						
VT Natural Square Tr.	4.39	3.99						
VT Memory Cell	1.64	1.36						
I_{DON} N-Channel	2.19	1.44						
N+ Active Area Contact Chain	5.59	5.02						
AL-W Silicide Contact Chain Resistance	3.00	1.33						

Table 34. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	4Q 97		3Q 97					
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	2.29	2.25	2.27	2.33				
Polysilicon I Thickness	2.78	2.65	2.93	2.89				
Gate Oxide Thickness (1)	1.91	1.87	1.34	1.28				
Tunnel Oxide Thickness	2.36	2.35	2.32	2.23				
ONO Bottom Oxide Thickness	1.51	1.44	1.53	1.50				
ONO Nitride Thickness	2.00	1.66	1.77	1.66				
ONO Top Oxide Thickness	2.55	2.41	3.28	3.22				
Active Area Critical Dimensions	2.00	1.54	1.85	1.50				
Polysilicon II Critical Dimensions	1.96	1.63	2.20	1.92				

Notes:1. Exhaust problems (progressive obstruction) solved in week 45 by rebuilding part of the exaust, to avoid this problems detectors have been installed.

Key Process Parameters	4Q 97		3Q 97					
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.64	2.42	2.37	2.06				
VT P-Channel 25 x 25 µm	2.47	1.54	2.56	1.75				
BV N-Channel 25 x 0.8 µm	(*)	3.23	(*)	4.75				
BV P-Channel 25 x 0.9 µm	(*)	3.87	(*)	3.00				
VT Memory Cell 0.8 x 0.8 µm	1.89	1.87	1.95	1.78				
I_{DON} N-Channel 25 x 0.8 µm	2.28	2.00	2.59	2.23				
Al+N+ Contact Chain	(*)	3.86	(*)	3.93				
AL-W Silicide Contact Chain Resistance	(*)	4.07	(*)	4.01				

(*) One side limit only.

Table 35. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	4Q 97 (2)		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness			1.65	1.60	1.69	1.67	2.01	1.96
Polysilicon I Thickness (1)			1.22	1.14	1.35	1.25	1.20	1.16
Gate Oxide Thickness			1.78	1.55	1.94	1.78	1.91	1.83
Tunnel Oxide Thickness			2.04	1.86	1.77	1.65	1.91	1.87
ONO Bottom Oxide hickness			1.46	1.44	1.42	1.39	1.55	1.49
ONO Nitride Thickness			1.59	1.52	1.66	1.60	1.52	1.49
ONO Top Oxide Thickness			2.02	2.02	1.58	1.57	1.93	1.86
Active Area Critical Dimensions			1.39	1.34	1.63	1.38	1.64	1.64
Polysilicon II Critical Dimensions			1.38	1.33	1.36	1.36	1.60	1.51

Notes: 1. The furnace temperature control system alignment is going to be implemented.
2. No production.

Key Process Parameters	4Q 97 (1)		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm			1.63	1.36	1.66	1.52	1.74	1.36
VT P-Channel 25 x 25 µm			1.59	1.42	1.51	1.48	1.45	1.41
BV N-Channel 25 x 0.8 µm			2.15	1.82	1.59	1.39	1.92	1.45
BV P-Channel 25 x 0.9 µm			3.25	2.48	2.42	1.84	4.36	3.31
VT Memory Cell 0.8 x 0.8 µm			1.70	1.66	2.19	1.73	1.51	1.43
I_{DON} N-Channel 25 x 0.8 µm			2.45	2.12	1.53	1.49	1.80	1.60
Al+N+ Contact Chain			4.19	3.12	2.43	1.48	4.45	2.72
Al-W Silicide Contact Chain Resistance			3.62	3.01	2.83	2.31	1.98	1.70

Note: 1. No production.

Table 36A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	4Q 97		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.65	1.59	1.46	1.42	1.69	1.67	1.95	1.90
First Poly Thickness (1)	1.58	1.46	1.21	1.19	1.45	1.39	1.20	1.16
Gate Oxide HV Thickness	1.81	1.69	1.85	1.83	1.94	1.78	1.91	1.83
Tunnel Oxide Thickness	2.43	2.36	1.66	1.64	1.77	1.65	1.91	1.87
Gate Oxide LV Thickness (2)	1.73	1.49	1.39	1.37	1.54	1.44	1.31	1.18
ONO Bottom Oxide Thickness (3)	1.17	1.15	1.49	1.45	1.72	1.55	1.52	1.45
ONO Nitride Thickness	1.49	1.35	1.53	1.49	1.66	1.60	1.52	1.45
ONO Top Oxide Thickness	1.86	1.78	1.70	1.68	1.54	1.44	1.93	1.86
Active Area CD	1.75	1.66	1.51	1.49	1.47	1.40	1.72	1.65
Second Poly CD	1.44	1.38	1.44	1.43	1.64	1.62	1.44	1.41

Notes: 1. The furnace temperature control system alignment is going to be implemented.
2. The low value is due to the introduction of this recipe on a vertical furnace. The optimization of the recipe is going on.
3. The recipe has been transferred from tubes with atmoscan to tubes with cantilever. We had a deterioration of thickness uniformity along the load. Tests have been completed to evaluate the possibility to transfer the recipe in a vertical tube allowing much better thickness control. This evaluation was completed and the process has been loaded on the Vtube starting from the end of January. We are confident to recover this value within the 1Q 98.

Table 36B. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	4Q 97		3Q 97		2Q 97		1Q 97	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	3.09	2.82	2.26	2.20	2.01	1.97	1.86	1.82
LV-PCh LVS (10 x 0.9) BV	2.46	2.55	2.61	2.55	3.13	3.09	2.03	1.97
LV-PCh LVS (10 x 0.9) Saturation Current	2.17	1.85	1.96	1.94	2.08	2.08	1.60	1.56
LV-PCh SQ. VTh	1.72	1.54	1.41	1.39	1.46	1.41	1.42	1.38
HV-NCh (10 x 1.2) LVS BV	2.84	2.32	1.63	1.59	2.01	1.99	2.01	1.91
HV-NCh SQ. VTh	1.68	1.66	1.63	1.61	1.69	1.65	1.83	1.77
HV-NCh (10 x 1.2) LVS Saturation Current	3.41	2.26	2.47	2.45	2.59	2.57	1.44	1.38
HV-PCh (10 x 1.3) BV	3.24	3.18	2.23	2.18	2.83	2.79	2.40	2.36
HV-PCh (10 x 1.3) Saturation Current	3.06	2.51	1.92	1.90	1.55	1.51	2.52	2.48
HV-PCh SQ. VTh (1)	1.28	1.20	1.39	1.37	1.41	1.37	1.39	1.35
UV Erased Cell VTh	1.82	1.43	1.38	1.35	1.44	1.40	1.65	1.61
N+ Contact Chain	2.44	1.84	2.20	2.00	2.10	2.04	3.53	3.49
Silicide Contact Chain	2.32	1.96	2.36	2.32	3.04	2.96	2.81	2.73
LV-NCh (10 x 0.8) BV	7.51	5.31	2.20	2.18	1.96	1.94	1.65	1.61

Note: 1. The problem is correlated with a tail of transistor dose implant that pass through the poly 1. We have already implemented a Poly implant energy modification, but this change is not sufficient to solve the problem. A trial is going to be issued to evaluate the change of poly1 thickness.

Table 37A. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Process Parameters	4Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.94	1.91						
First Poly Thickness	1.61	1.51						
Gate Oxide HV Thickness (1)	1.59	1.21						
Tunnel Oxide Thickness	1.80	1.80						
Gate Oxide LV Thickness	1.44	1.36						
ONO Bottom Oxide Thickness	1.59	1.54						
ONO Nitride Thickness	2.13	2.09						
ONO Top Oxide Thickness	2.21	2.05						
Active Area CD	1.58	1.33						
Second Poly CD	1.74	1.50						

Note: 1. Process alignment is running.

Table 37B. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Catania - Italy M5 Diffusion Line

Key Process Parameters	4Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
LV-NCh LVS (10 x 0.8) Saturation Current	2.60	2.54						
LV-PCh LVS (10 x 0.9) BV	1.70	1.35						
LV-PCh LVS (10 x 0.9) Saturation Current	2.30	2.00						
LV-PCh SQ. VTh	1.80	1.53						
HV-NCh (10 x 1.2) LVS BV	(*)	1.49						
HV-NCh SQ. VTh	2.01	1.45						
HV-NCh (10 x 1.2) LVS Saturation Current	2.52	2.35						
HV-PCh (10 x 1.3) BV	2.38	1.62						
HV-PCh (10 x 1.3) Saturation Current	2.19	1.73						
HV-PCh SQ. VTh	1.59	1.38						
UV Erased Cell VTh	1.88	1.55						
N+ Contact Chain	4.85	3.84						
Silicide Contact Chain	1.76	1.36						
LV-NCh (10 x 0.8) BV	(*)	2.32						

(*) One side limit only.

Table 38. Statistical Process Control: UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	4Q 97	3Q 97	2Q 97	1Q 97
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	40.18	37.14	45.75	16.02
Stud Pull	1.40	1.71	1.35	1.69
Bond Strength (W.B.)	5.50	5.29	4.01	4.07
SN Thickness (Tin Plate)	1.39	1.48	1.58	1.50

Table 39. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	4Q 97	3Q 97	2Q 97	1Q 97
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	2.24	3.13	2.13	-
Ball Shear (W.B.)	2.07	1.89	2.54	-
Bond Strength (W.B.)	1.85	1.57	1.86	-
Coplanarity	2.53	3.55	4.06	-
Plating Thickness	2.17	2.00	1.47	-

Table 40. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	4Q 97	3Q 97	2Q 97	1Q 97
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.30	4.18	3.46	-
Ball Shear (W.B.)	2.09	2.05	1.88	-
Bond Strength (W.B.)	1.52	1.62	1.47	-
Plating Thickness	2.85	3.56	2.77	-