

## Designing with L4971, 1.5A High Efficiency DC-DC Converter

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### INTRODUCTION

The L4971 is a 1.5A monolithic dc-dc converter, step- down , operating at fix frequency continuous mode. It is realised in BCD60 II technology, and it is available in two plastic packages, MINIDIP and SO16L.

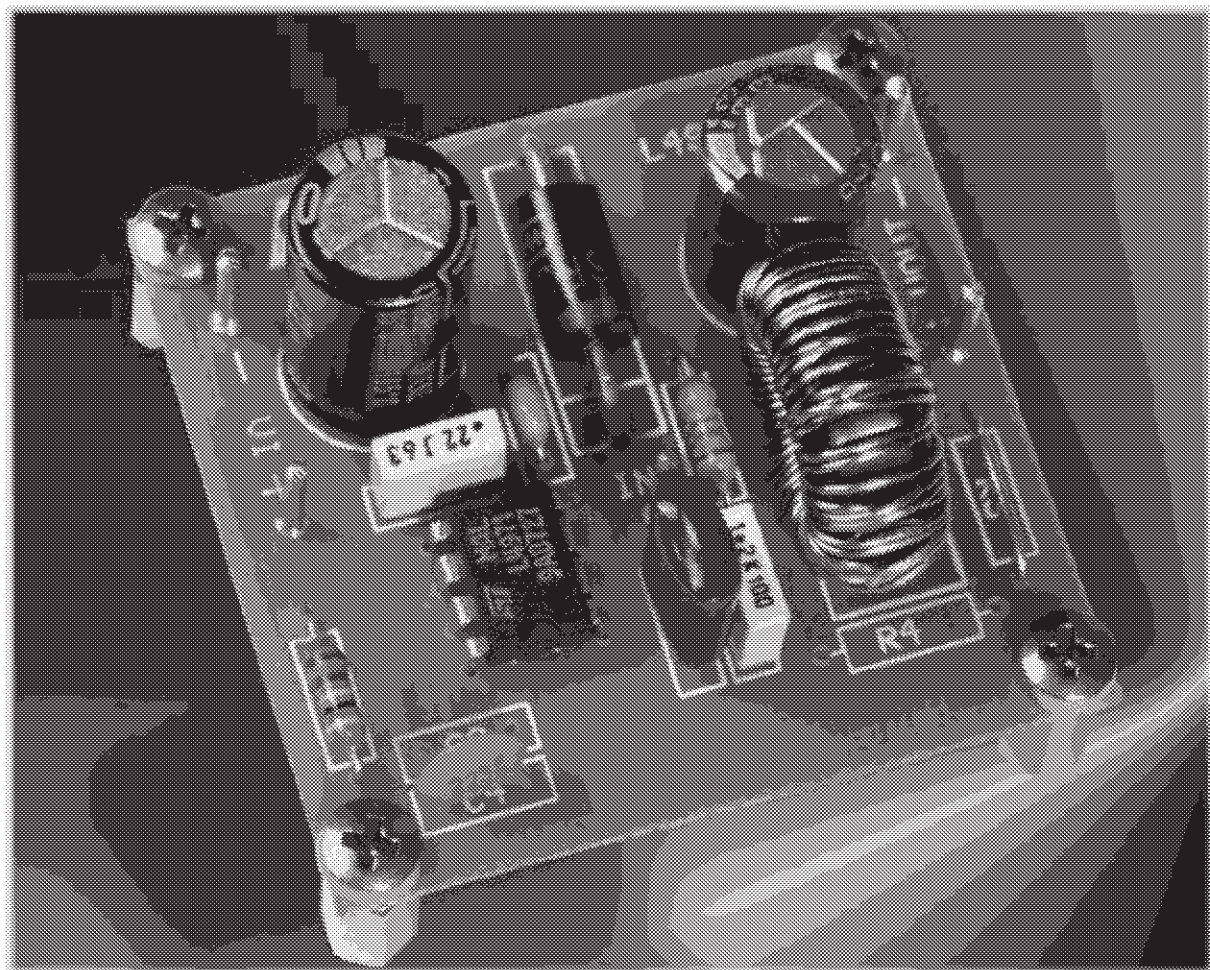
One direct fixed output voltage at  $3.3V \pm 1\%$  is available, adjustable for higher output voltage values, till 40V, by an external voltage divider.

The operating input supply voltage ranges from 8V to 55V, while the absolute value, with no load, is 60V.

New internal design solutions and superior technology performance allow to generate a device with improved efficiency in all the operating conditions and with reduced EMI due to an innovative internal driving circuit, and reduced external component counts.

While internal limiting current and thermal shutdown are today considered standard protection functions, mandatory for a safe load supply, oscillator with voltage feedforward improves line regulation and overall control loop.

Soft-start avoids output overvoltages at turn-on, while, shorting this pin to ground, the device is completely disabled, going into zero consumption state.

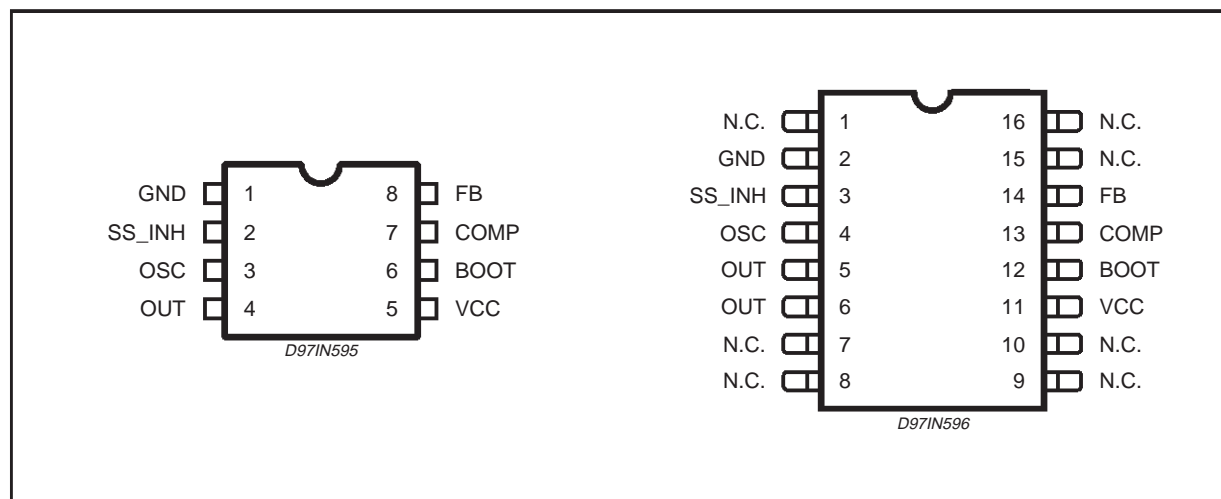


### DEVICE DESCRIPTION

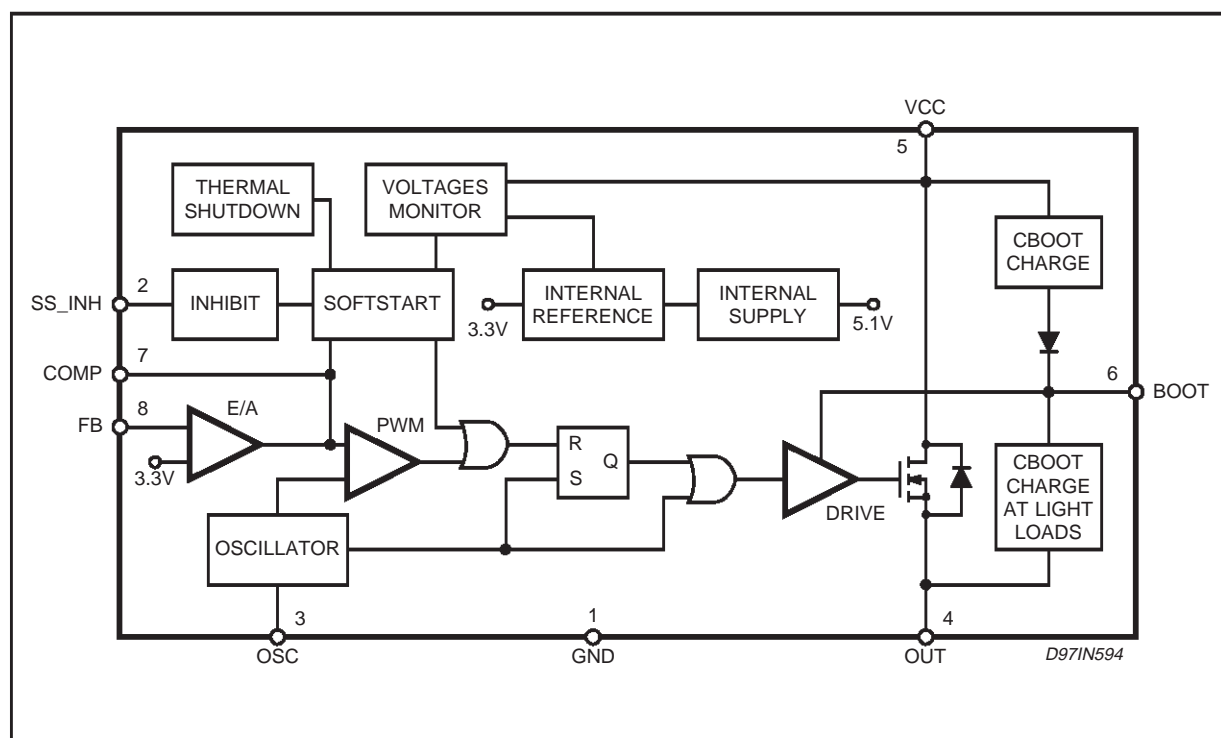
For a better understanding of the device and its working principles, a short description of the main building blocks is given here below, with packaging options and complete block diagram.

Figure 1 shows the two packaging options, with the pin function assignments.

**Figure 1. Pins connection.**



**Figure 2. Block diagram.**



### Power supply & Voltage reference

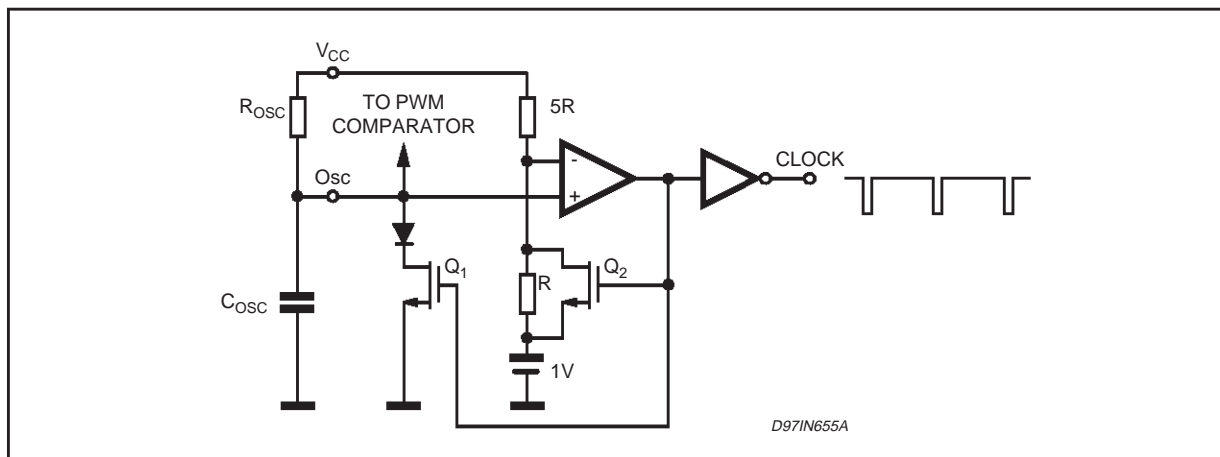
The device is provided with an internal stabilised power supply (of about 12V typ.) that powers the analog and digital control blocks and the bootstrap section.

From this preregulator, a 3.3V reference voltage  $\pm 2\%$ , is internally available.

### Oscillator and voltage feedforward.

Just one pin is necessary to implement the oscillator function, with inherent voltage feedforward.

**Figure 3. Oscillator internal circuit.**



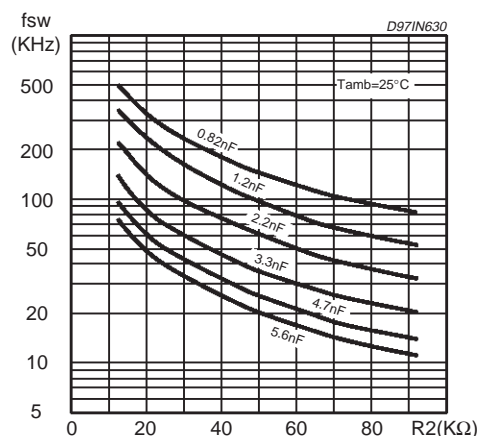
A resistor  $R_{osc}$  and a capacitor  $C_{osc}$  connected as shown in fig. 3, allow the setting of the desired switching frequency in agreement with the below formula:

$$F_{SW} = \frac{1}{R_{osc} \cdot C_{osc} \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

Where  $F_{SW}$  is in kHz,  $R_{osc}$  in  $\Omega$  and  $C_{osc}$  in F.

The oscillator capacitor,  $C_{osc}$ , is discharged by an internal mos transistor with  $100\Omega$  of  $R_{dson}$  (Q1) and during this period the internal threshold is set at 1V by a second mos, Q2. When the oscillator voltage capacitor reaches the 1V threshold, the output comparator turns off the mos Q1 and turns on the mos Q2, restarting the  $C_{osc}$  charge.

**Figure 4. Switching frequency vs.  $R_{osc}$  and  $C_{osc}$ .**



The oscillator block, shown in fig.4, generates a sawtooth wave signal that sets the switching frequency of the system.

This signal, compared with the output of the error amplifier, generates the PWM signal that will modulate the conduction time of the power output stage.

The way the oscillator has been integrated, does not require additional external components to benefit of the voltage feedforward function.

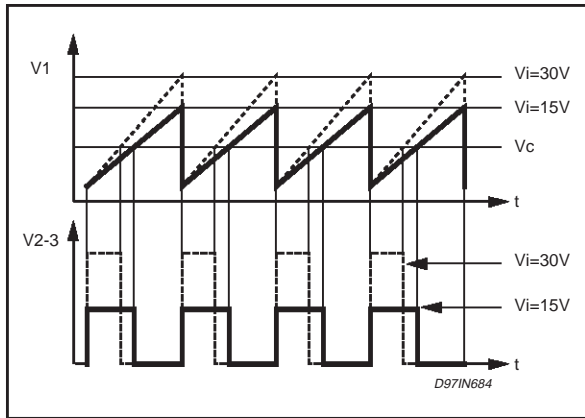
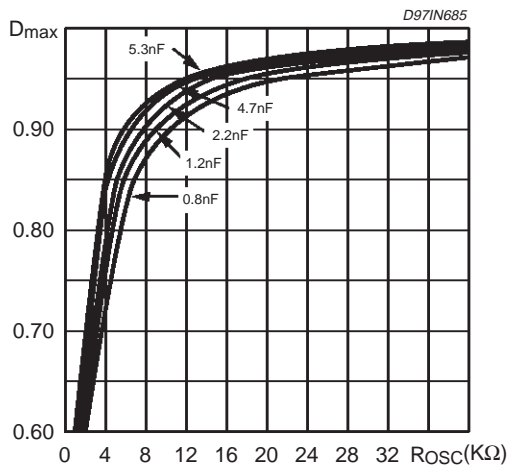
The oscillator peak-to-valley voltage is proportional to the supply voltage, and the voltage feedforward is operative from 8V to 55V of input supply.

$$\Delta V_{osc} = \frac{V_{CC} - 1}{6}$$

Also the  $\Delta V/\Delta t$  of the sawtooth is directly proportional to the supply voltage. As  $V_{CC}$  increases, the  $T_{on}$  time of the power transistor decreases in such a way to provide to

the choke, and finally also the load, the product  $Volt \times sec$  constant.

Fig 5 shows how the duty cycle varies as a result of the change on the  $\Delta V/\Delta t$  of the sawtooth with the  $V_{CC}$ .

**Figure 5. Voltage Feedforward Function.**

**Figure 6. Maximum Duty Cycle vs R<sub>osc</sub> and C<sub>osc</sub> as parameter**


the controller reduces the on-time till the value of  $T_B = 300\text{ns}$  that is a blanking time in which the current limit protection does not trigger. This minimum time is necessary to avoid undesirable intervention of the protection due to the spike current generated during the recovery time of the freewheeling diode.

In this condition, because of this fixed blanking time, the output current is given by:

$$I_{\max} = \frac{[V_{CC} \cdot T_B \cdot F_{sw} - V_f \cdot (1 - T_B \cdot F_{sw})]}{[R_o + (R_D + R_L) (1 - T_B \cdot F_{sw}) + (R_{dson} + R_L) T_B \cdot F_{sw}]}$$

In fig 7.1, the pulse by pulse protection is sufficient to limit the current.

In fig 7.2 the pulse by pulse protection is no more effective to limit the current due to the minimum  $T_{on}$  fixed by the blanking time  $T_B$ , and the hiccup protection intervenes because the output peak current reaches the relative threshold.

At the pulse by pulse intervention (point A) the output voltage drops because of the  $T_{on}$  reduction, and the current is almost constant. Going versus the short circuit condition, the current is only limited by the series resistances  $R_D$  and  $R_L$  (see relation above) and could reach the hiccup threshold (point B), set 20% higher than the pulse by pulse. Once the hiccup limiting current is operating, in output short circuit condition, the delivered average output current decreases dramatically at very low values (point C).

The output of the error amplifier doesn't change in order to maintain the output voltage constant and in regulation.

With this function on board, the output response time is greatly reduced in presence of an abrupt change on the supply voltage, and the output ripple voltage at the mains frequency is greatly reduced too.

In fact, the slope of the ramp is modulated by the input ripple voltage, generally present in the order of some tens of Volt, for both off-line and dc-dc converters using mains transformers.

The charge and discharge time are approximable to:

$$T_{ch} = R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right)$$

$$T_{dis} = 100 \cdot C_{osc}$$

The maximum duty cycle is a function of  $T_{ch}$ ,  $T_{dis}$  and an internal delay and is expressed by the equation:

$$D_{\max} = \frac{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) - 80 \cdot 10^9}{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

It is represented in figure 6.

### Current Protection

The L4971 has two current limit levels, pulse by pulse and hiccup modes.

Increasing the output current till the pulse by pulse limiting current threshold ( $I_{th1}$  typ. value of 2.5A)

Increasing the output current till the pulse by pulse limiting current threshold ( $I_{th1}$  typ. value of 2.5A)

Figure 7. 1. Output Characteristic

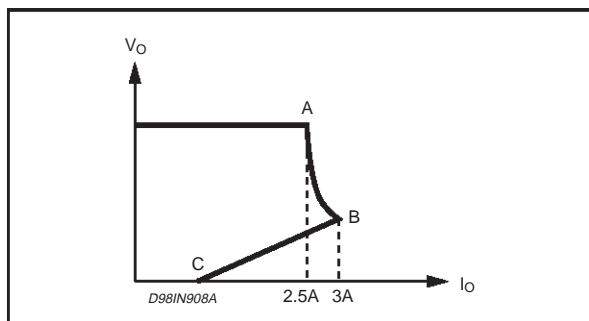


Figure 7.2. Output Characteristic

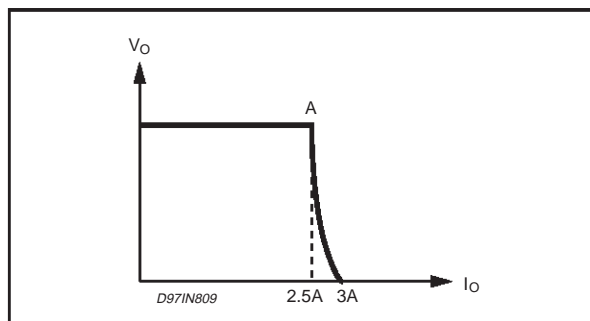


Figure 8. Current Limit internal schematic circuit.

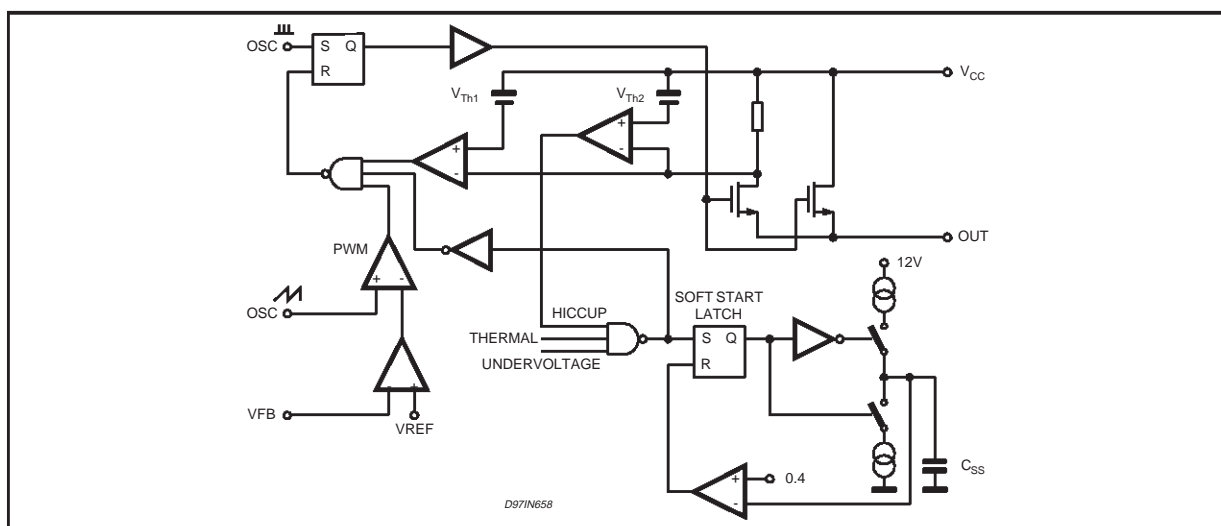


Fig. 8 shows the internal current limiting circuitry.  $V_{th1}$  is the pulse by pulse while  $V_{th2}$  is the hiccup threshold.

The sense resistor is in series with a small mos realised as a partition of the main DMOS.

The  $V_{th2}$  comparator (20% higher than  $V_{th1}$ ) sets the soft start latch, initialising the discharge of the soft start capacitor with a constant current (about 22 $\mu$ A). Reaching about 0.4V, the valley comparator resets the soft start latch, restarting a new recharge cycle.

Fig. 9 Shows the typical waveforms of the current in the output inductor and the soft start voltage (pin 2).

During the recharging of the soft start capacitor, the  $T_{on}$  increases gradually and, if the short circuit is still present, when  $T_{on} > T_B$  and the output peak current reaches the threshold, the hiccup protection intervenes again. So, the value of the soft start capacitor must not be too high (in this case the  $T_{on}$  increases slowly thus taking much time to reach the  $T_B$  value) to avoid that during the soft start slope, the current exceeds the limit before the protection activation.

The following diagrams of Fig10a and Fig10b show the maximum allowed soft-start capacitor as a function of the input voltage, inductor value and switching frequency. A minimum value of the soft start capacitance is necessary to guarantee, in short circuit condition, the functionality of the limiting current circuitry. Infact, with a capacitor too small, the frequency of the current peaks (see figure 9) is high and the mean current value in short circuit increases.

Example: for a maximum input voltage of 55V at 100kHz, with an inductor of 260 $\mu$ H, it is possible to use



Figure 9. Output current and soft-start voltage

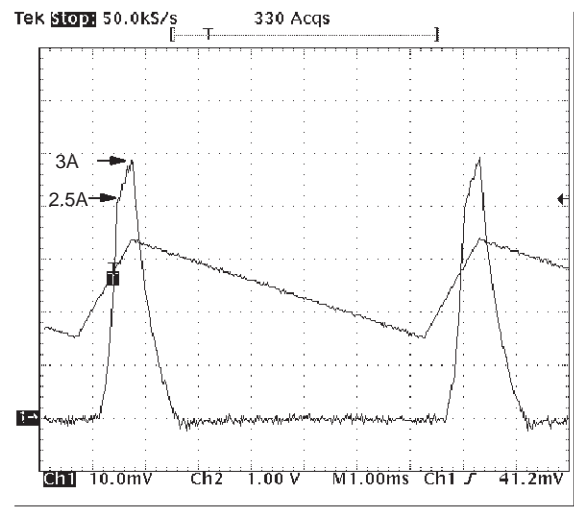
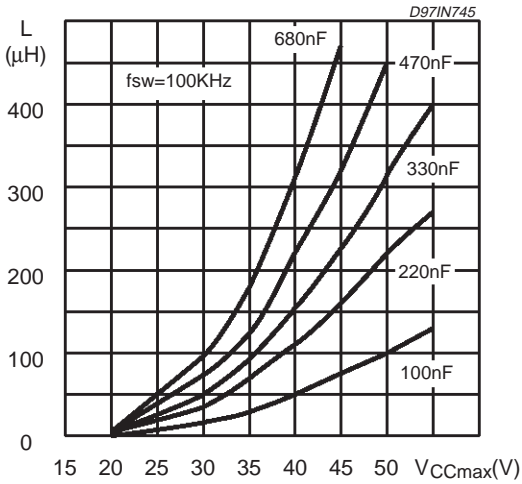


Figure 10a. Maximum Soft Start  
Capacitance with  $f_{sw} = 100\text{kHz}$





## AN937 APPLICATION NOTE

Turning  $V_{CC}$  off, the soft-start capacitor is discharged with a constant  $10\mu A$  (S2 closed, S3 closed, S1 and S4 open), from the moment when  $V_{CC}$  is crossing the UVLO off threshold.

The final discharge value is 1.2V.

In case of the  $C_{SS}$  is discharged using an external grounded element when the voltage at  $C_{SS}$  reaches the threshold of 1.3V Comp2 resets the flip flop, S1 is closed, S2 is opened and the  $40\mu A$  current generator is activated.

The external switch, sinking some mA, discharges the soft-start under the 1.2V Comp1 threshold, opening S3 and closing S4. At this point the device is in disable, sourcing only  $5\mu A$  through pin 2.

When the external grounding element is removed, the device restarts charging the soft start capacitance, initially, with  $5\mu A$  till the voltage reaches the 1.8V threshold and Comp1 connects the  $40\mu A$  charging current generator.

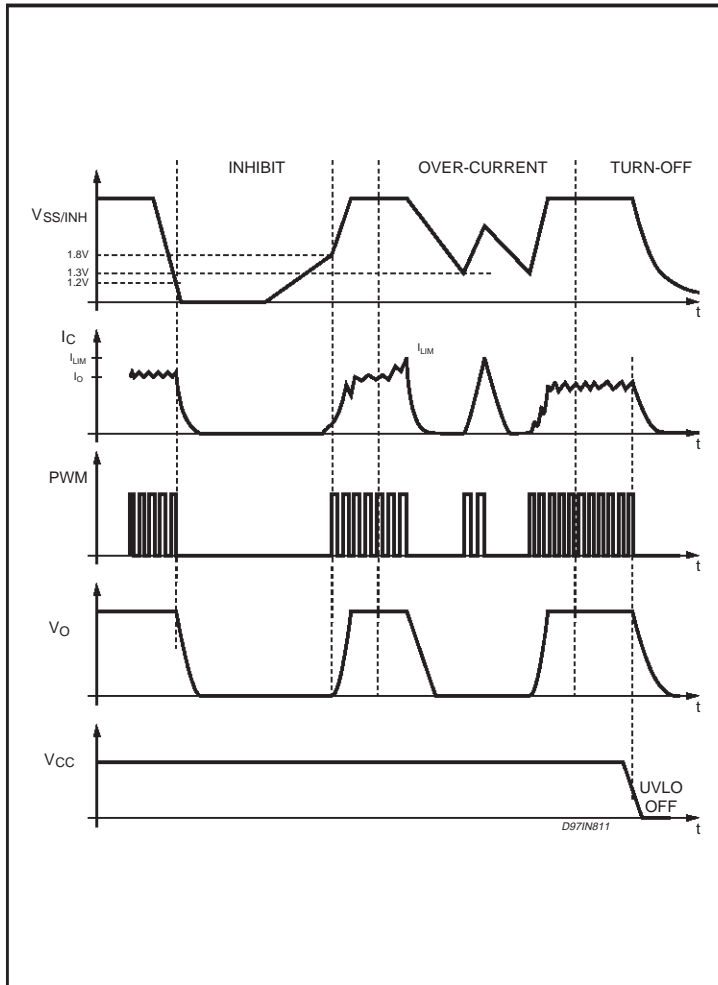
In case of thermal shutdown or overcurrent protection intervention the power is turned off and the flip flop turns off S2 and turns on S1. The soft-start is discharged till the voltage reaches the 1.3V threshold, and Comp2 resets the flip flop. S1 is closed, S2 is opened and the soft-start capacitance is charged again.

Fig 11a shows the systems signals during Inhibit, overcurrent and  $V_{CC}$  turn off.

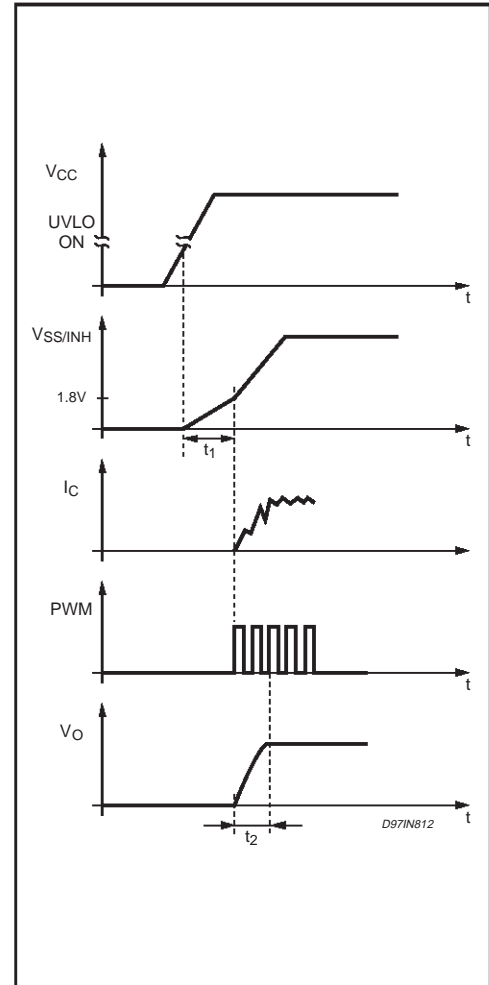
$t_1$  and  $t_2$  can be calculated by the following equations:

$$t_1 = 0.36 \cdot C_{SS}; \quad t_2 = \frac{V_o}{I_{ch} \cdot 6 \cdot D_{max}} \cdot C_{SS}$$

**Figure 11a. Timing Diagram in Inhibit, overcurrent and turn off condition**



**Figure 11b. Start up sequence.**





where  $D_{max}$  is 0.95,  $C_{ss}$  is in  $\mu F$  and  $I_{ch}$  is in  $\mu A$ .

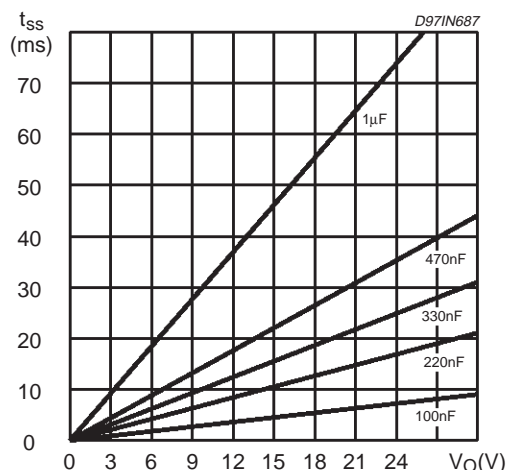
Soft-start time ( $t_2$ ) versus output voltage and  $C_{ss}$  is shown in Fig12.

Thanks to the voltage feedforward, the start-up time ( $t_2$ ) is not affected by the input voltage.

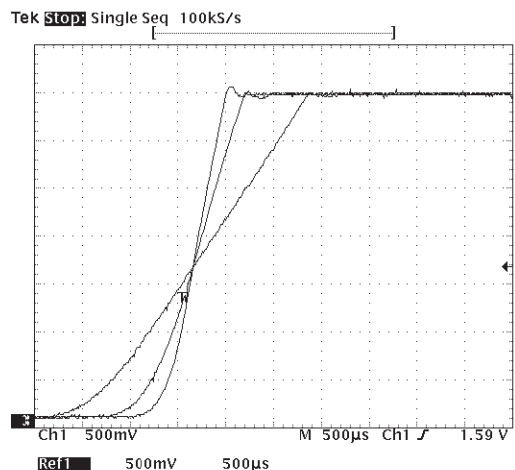
Fig13 shows the output voltage start-up using different soft-start capacitance values:

It is mandatory a minimum capacitor value of 22nF. The pin 2 cannot be left open.

**Figure 12. Soft start time( $t_2$ ) vs  $V_O$  and  $C_{ss}$**



**Figure 13. Output rising voltage with  $C_{ss}$  56nF, 100nF, 220nF.**



### Feedback disconnection

In case of feedback disconnection, the duty cycle increases versus the max allowed value bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this dangerous condition, the device is forcing a little current (1.4 $\mu A$  typical) out of the pin 8 (E/A Feedback). If the feedback is disconnected, open loop, and the impedance at pin 8 is higher than 3.5M Ohm, the voltage at this pin goes higher than the internal reference voltage located on the non-inverting error amplifier input, and turns-off the power device.

### Zero load

In normal operation, the output regulation is also guaranteed because the bootstrap capacitor is recharged, cycle by cycle, by means of the energy flowing into the choke.

Under light load conditions, this topology tends to operate in burst mode, with random repetition rate of the bursts.

An internal new function makes this device capable of keeping the output voltage in full regulation with 1mA of load current only.

Between 1mA and 500 $\mu A$ , the output is kept in regulation up to 8% above the nominal value.

Here the circuitry providing the control :

- 1- a comparator located on the bootstrap section is sensing the bootstrap voltage; when this is lower than 5V, the internal power VDMOS is forced ON for one cycle and OFF for the next.
- 2- during this operation mode, i.e. 500 $\mu A$  of load current, the E/A control is lost. To avoid output over-voltages, a comparator with one input connected to pin 8, and the second input connected to a threshold 8% higher than nominal output, turns OFF the internal power device the output is reaching that threshold.

When the output current, or rather, the current flowing into the choke, is lower than 500 $\mu A$ , that is also the consumption of the bootstrap section, the output voltage starts to increase, approaching the supply voltage.

### Output Overvoltage Protection (OVP)

The output overvoltage protection, OVP, is realised by using an internal comparator, which input is connected to pin 8, the feedback, that turns-off the power stage when the OVP threshold is reached.

This threshold is typically 8% higher than the feedback voltage.

When a voltage divider is requested for adjusting the output voltage, the OVP intervention will be set at:

$$V_{ovp} = 1.08 \cdot V_{fb} \cdot (R_a + R_b) / R_b$$

where  $R_a$  is the resistor connected to the output.

### Power Stage

The power stage is realised by a N-channel D-mos transistor with a  $V_{dss}$  in excess of 60V and typ  $R_{dson}$  of 290mOhm (measured at to device pins).

To minimise the  $R_{dson}$ , means also minimise the conduction losses.

But also the switching losses have to be taken into consideration mainly for the two following reasons:

- a- they are affecting the system efficiency and the device power dissipation
- b- because they generate EMI.

### TURN - ON

At turn-on of the power element, or better, the rise time of the current ( $di/dt$ ) at turn-on is the most critical parameter to compromise.

At a first approach, it looks that the faster it is the rise time and the lower are the turn-on losses.

It's not completely true.

There is a limit, and it's introduced by the recovery time of the recirculation diode.

Above this limit, about 100A/usec, only disadvantages are obtained:

- 1- turn-on overcurrent is decreasing efficiency and system reliability
- 2- big EMI increasing.

The L4971 has been developed with a special focus on this dynamic area.

An innovative and proprietary gate driver, with two different timings, has been introduced.

When the diode reverse voltage is reaching about 3V, the gate is sourced with low current (see fig 14) to assure the complete recovery of the diode without generating unwanted extra peak currents and noise.

After this threshold, the gate drive current is quickly increased, producing a fast rise time till the peak current, so maintaining the efficiency very high.

### TURN - OFF

The turn-off behaviour, is shown at Fig 14.

Fig 15 shows the details of the internal power stage and driver, where at Q2 is demanded the turn-off of the power switch, S.

### TYPICAL APPLICATION

Fig. 16 shows the typical application circuit, where the input supply voltage,  $V_{cc}$ , can range from 8 to 55V operating, and the output voltage adjustable from 3.3V to 40V.

The selected components, and in particular input and output capacitors, are able to sustain the device voltage ratings, and the corresponding RMS currents.

### Electrical Specification

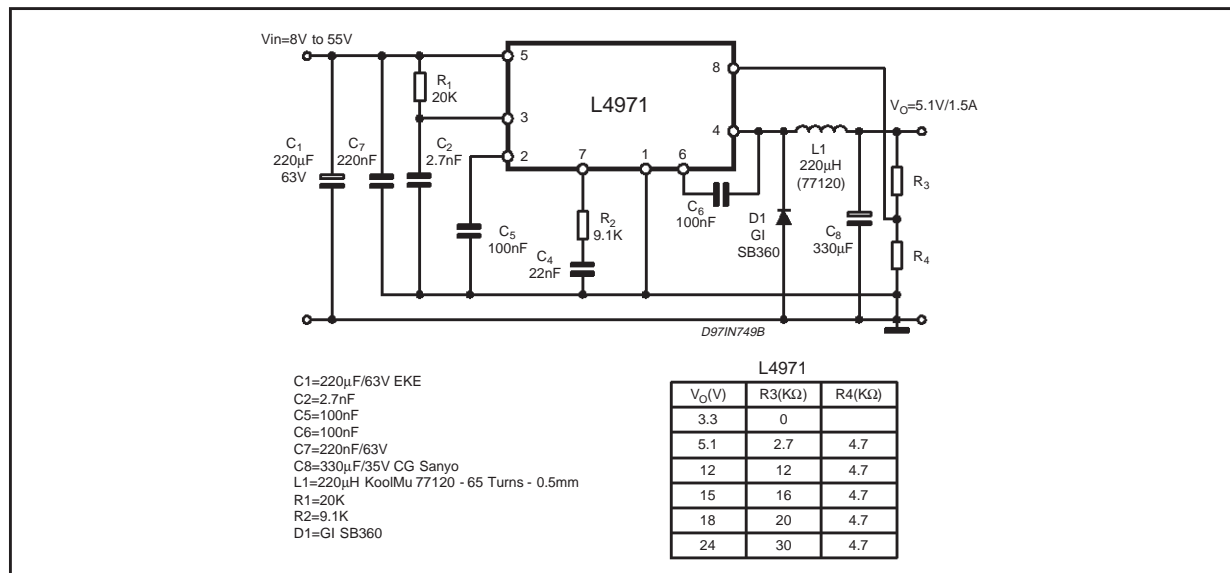
Input Voltage range	8V-55V
Output Voltage	5.1V $\pm$ 3% (Line, Load and Temperature)



## AN937 APPLICATION NOTE

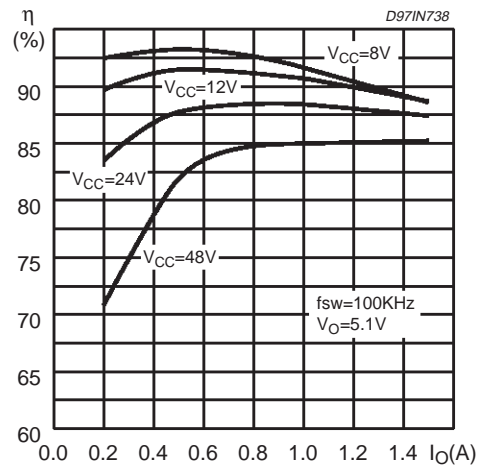
Output ripple	20mV
Output Current range	1mA-1.5A
Max Output Ripple current	15% I <sub>omax</sub>
Current limit	2.5A
Switching frequency	100kHz

**Figure 16. Application Circuit**



Target Efficiency	85% @ 1.5A V <sub>i</sub> =55V
	91% @ 0.5A V <sub>i</sub> =12V

**Figure 17. Efficiency vs Output Current**



### Main components description

#### INPUT CAPACITOR

The input capacitors have to be able to support the max input operating voltage of the device and the max rms input current.

The input current is squared and the quality of these capacitors has to be very high to minimise its power dissipation generated by the internal ESR, improving the system reliability. Moreover, input capacitors are also affecting the system efficiency.

The max I<sub>rms</sub> current flowing through the input capacitors is:

$$I_{rms} = I_o \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

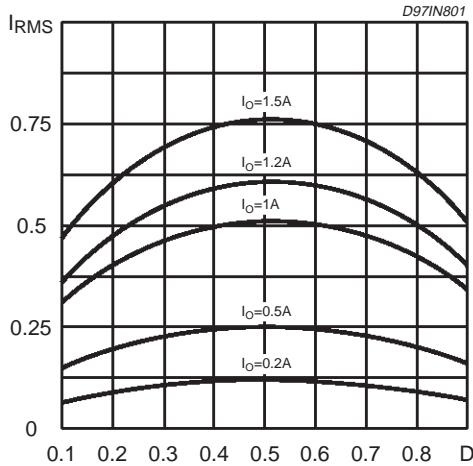
where  $\eta$  is the expected system efficiency, D is the duty cycle and I<sub>o</sub> the output dc current. This function reaches the maximum value at D = 0.5 and the equivalent rms current is equal to I<sub>o</sub>/2.

The following diagram is the graphical representation of the above equation, with an estimated efficiency of 85% at different output currents.

The maximum and minimum duty cycles are:

$$D_{\max} = \frac{V_o + V_f}{V_{\text{in min}} + V_f} = 0.66$$

**Figure 18. Input Capacitance rms current vs duty cycle**



$$D_{\min} = \frac{V_o + V_f}{V_{\text{in max}} + V_f} = 0.1$$

where  $V_f$  is the freewheeling diode forward voltage.

This formula is not taking into account the power mos  $R_{\text{ds on}}$ , considering negligible the inherent voltage drop, respect input and output voltages.

At full load, 1.5A and  $D = 0.5\%$  the rms capacitor current to be sustained is of 0.75A.

The selected EKE 220 $\mu$ F/63V Roderstain is able to support this current.

### Inductor Selection

The inductor ripple current is fixed at 10% of  $I_{\text{omax}}$  and is 0.15A, the inductor needed is:

$$L_o = (V_o + V_f) \cdot \frac{(1 - D_{\min})}{\Delta I_o \cdot f_{\text{sw}}} = 310\mu\text{H} \quad (\text{eq1})$$

The  $L_o \cdot I_o^2$  is 0.58 and the size core chose is 77120 (125 $\mu$ ) Magnetics KoolM $\mu$  material and are wiring 65Turns. At full load the magnetising force is about 25 Oersted, the inductance value is reduced at about  $L = 220\mu\text{H}$  and the ripple current increases at 0.24A (16%  $I_{\text{omax}}$ ).

It is possible to graficate the Eq 1 as a function of  $V_o$  and  $V_{\text{in max}}$  at 100kHz and 200kHz (see Fig19a-b).

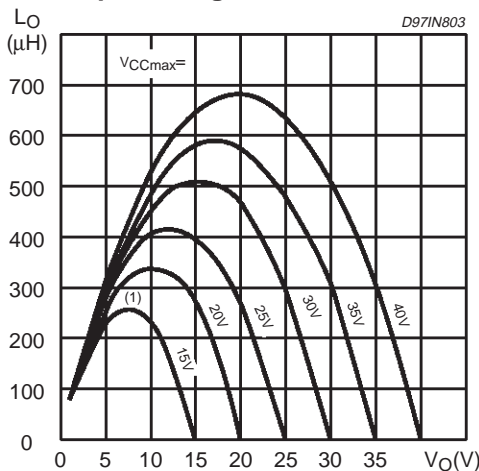
These curves are useful to define the inductor value immediately.

Example: With a maximum input voltage of 15V at 100kHz, fixed the curve (1) in Fig19a and with an output voltage of 5V the inductor needed is 220 $\mu$ H.

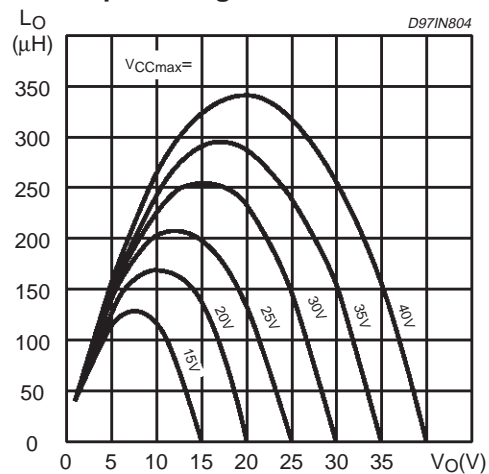
### -core losses

Core losses are proportional to the magnetic flux swing into the core material. To evaluate the flux swing is used the following formula:

**Figure 19a. Inductor needed as a function of maximum input voltage and output voltage at  $f_{\text{sw}}=100\text{kHz}$**



**Figure 19b. Inductor needed as a function of maximum input voltage and output voltage at  $f_{\text{sw}}=200\text{kHz}$**



## AN937 APPLICATION NOTE

$$\Delta B = \frac{L \cdot \Delta I_o \cdot 10^4}{N_o \cdot A_{le}} = 423 \text{ Gauss}$$

where  $A_{le}$  is the core cross section [ $m^2$ ].

The chosen core material family has an empirical equation to calculate the losses:

$$P_L = \Delta B^2 \cdot f_{sw}^{1.5} \cdot V_L \cdot 10^2 = 141 \text{ mW}$$

Where  $\Delta B$  is in KGauss,  $f_{sw}$  in kHz and  $V_L$  is the core volume in  $cm^3$ . The core increasing temperature is:

$$\Delta T = \left( \frac{P_L}{13.6} \right)^{0.833} = 7^\circ C$$

### Output Capacitor

The selection of  $C_{out}$  is driven by the output ripple voltage required, 1% of  $V_o$ . This is defined by the output capacitance ESR and with the maximum ripple current (0.24A) the maximum ESR is:

$$ESR = \Delta V_o / \Delta I_o = 0.051 / 0.24 = 212 \text{ m}\Omega$$

The selected capacitance is 330 $\mu$ F/35V CG Sanyo with  $ESR = 86 \text{ m}\Omega$  and the ripple voltage is 0.40% of  $V_o$  (20mV).

The drop due to a fast load variation of 1A produce an output drop of :

$$ESR \cdot \Delta I_o = 86 \text{ mV}$$

that is the 1.6% of the output voltage.

Output capacitance has to support a load transient until the inductor current reaches the increased current. The output drop during an output current variation is:

$$\Delta V_o = \frac{(\Delta I_o)^2 \cdot L_o}{2 \cdot C_o \cdot (V_{inmin} \cdot D_{max} - V_o)} \quad \text{Eq(2)}$$

Where  $\Delta I_o$  is the current load variation (0.5A to 1.5A),  $D_{max}$  is the maximum duty cycle (95%),  $V_o$  is 5.1V and  $L_o$  is 220 $\mu$ H.

Equation 2, normalised by  $V_o$  is represented in the following diagram( Fig. 20) as a function of the minimum input voltage.

These curves are represented for different output capacitor 100 $\mu$ F, 220 $\mu$ F, 2x220 $\mu$ F, 2x330 $\mu$ F.

### Compensation Network

The complete control loop block diagram is shown in fig. 21

**Figure 20. Output drop vs minimum input voltage**

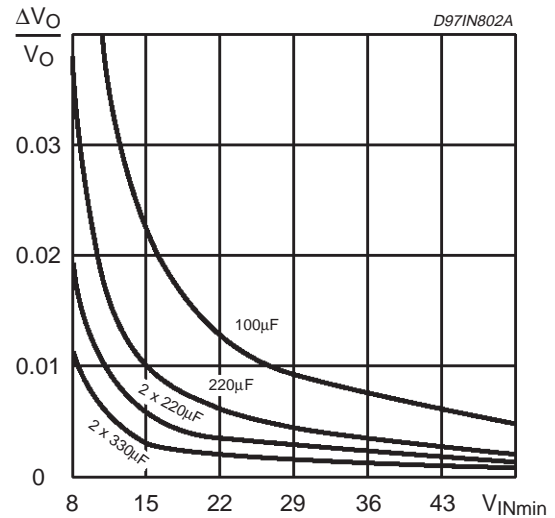
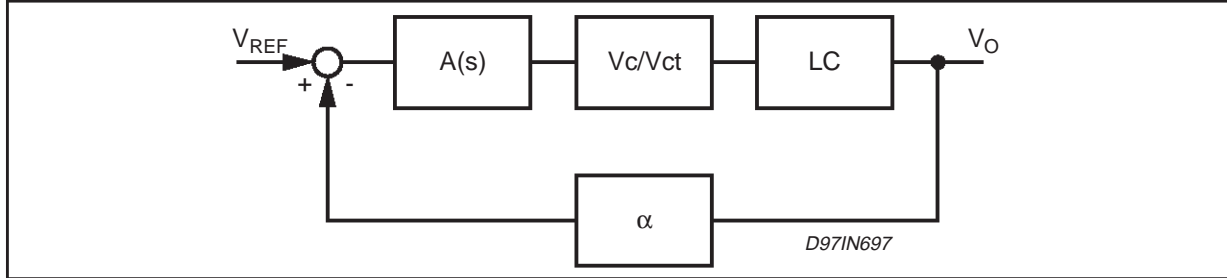




Figure 21. Block diagram compensation loop

T  
h

the transfer functions described are:

### Error amplifier and compensation block

$$A(s) = \frac{A_{vo} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot C_o \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot C_o + R_c \cdot C_c) + 1}$$

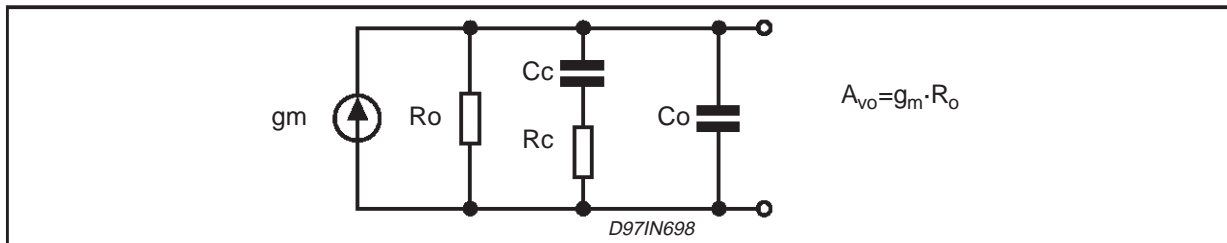
$C_o$  is the parallel between the output capacitance and the external capacitance of the Error Amplifier  
 $R_c$  and  $C_c$  are the compensation values

### LC filter

$$A_o(s) = \frac{1 + R_{esr} \cdot C_{out} \cdot s}{L \cdot C_{out} \cdot s^2 + R_{esr} \cdot C \cdot s + 1}$$

Figure 22. Error Amplifier Compensation Circuit

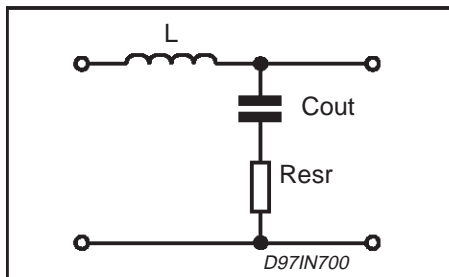
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### WM gain

$$\frac{V_{cc}}{V_{ct}} = \frac{V_{cc} \cdot 6}{V_{cc} - 1} \approx 6$$

Figure 23. Output Filter



where  $V_{ct}$  is the peak to peak sawtooth oscillator

### Voltage divider

$$\alpha = \frac{R_4}{R_3 + R_4}$$

The Error Amplifier basic characteristics are:

$$R_o = 1.2M\Omega$$

$$A_{vo} = 60dB$$

$$C_o = 220pF$$

The poles and zeros value are:

$$F_o = \frac{1}{2 \cdot \pi \cdot R_{esr} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot 0.086 \cdot 330 \cdot 10^{-6}} = 5.6\text{KHz}$$

$$F_p = \frac{1}{2 \cdot \pi \cdot \sqrt{L} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot \sqrt{220 \cdot 10^{-6}} \cdot 330 \cdot 10^{-6}} = 590\text{Hz}$$

$$F_{ocomp} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 795\text{Hz}$$

$$F_{p1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 1.2 \cdot 10^6 \cdot 22 \cdot 10^{-9}} = 6.02\text{Hz}$$

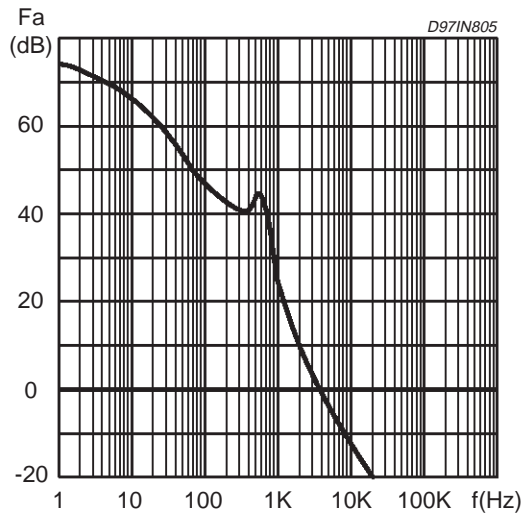
$$F_{p2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 80\text{KHz}$$

The compensation is realised choosing the  $F_{ocomp}$  nearly the frequency of the double pole due to the LC filter.

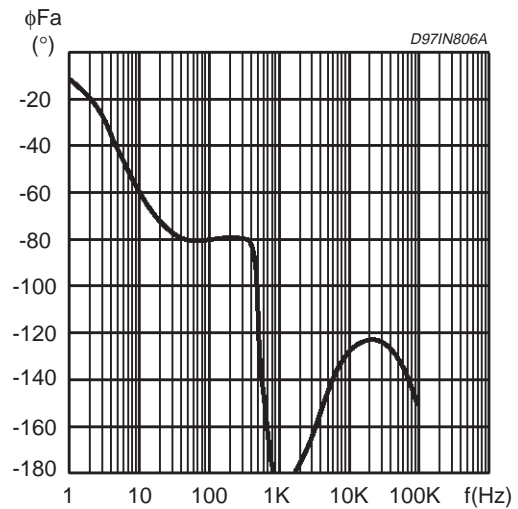
Using compensation network  $R1 = 9.1\text{K}$ ,  $C6 = 22\text{nF}$  and  $C5 = 220\text{pF}$  obtain the Gain and Phase Bode plot of Figg. 24-25. Is possible to omit  $C5$  because does not influence the system stability but is useful only to reduce the noise. The cut off frequency and a phase margin are:

$$F_c = 3.7\text{KHz}; \text{ Phase margin} = 21^\circ$$

**Figure 24. Gain Bode open loop plot**



**Figure 25. Phase Bode open loop plot**



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