SGS-THOMSON MICROELECTRONICS

USER'S MANUAL

ST75C52 - ST75C520

SUMMARY **Page**

I - PRELIMINARY

The ST75C52/520 includes FAX, modem and voice modes.

In FAX mode the chip works as a G3 synchronous half-duplex modem including all the possibilities to work on the public telephone networks. With a microcontroller (such as SANYO LC82141) a complete G3 facsimile system can be built including all the functions (image processor, motor interface, PIO...). Tones can be sent or detected using programmable tone generators and detectors.

In Modem mode FSK full-duplex communications using V.23, V.21, Bell 103 modulation/demodulation on PSTN or leased lines are possible.

In voice mode the user can record or send messages using PCM A-law standard.

Tones (DTMF...) can be sent and/or detected.

This component satisfies the communication requirements specified in ITU-T recommandations V.33 [(1)], V.17, V.29 (T104), V.27 ter (with short train), V.21 ch2, V.21, V.23, or Bell 103 and communication at a data rate of 14400, 12000, 9600, 7200, 4800, 2400, 300, 1200/75 is possible.

Convention :

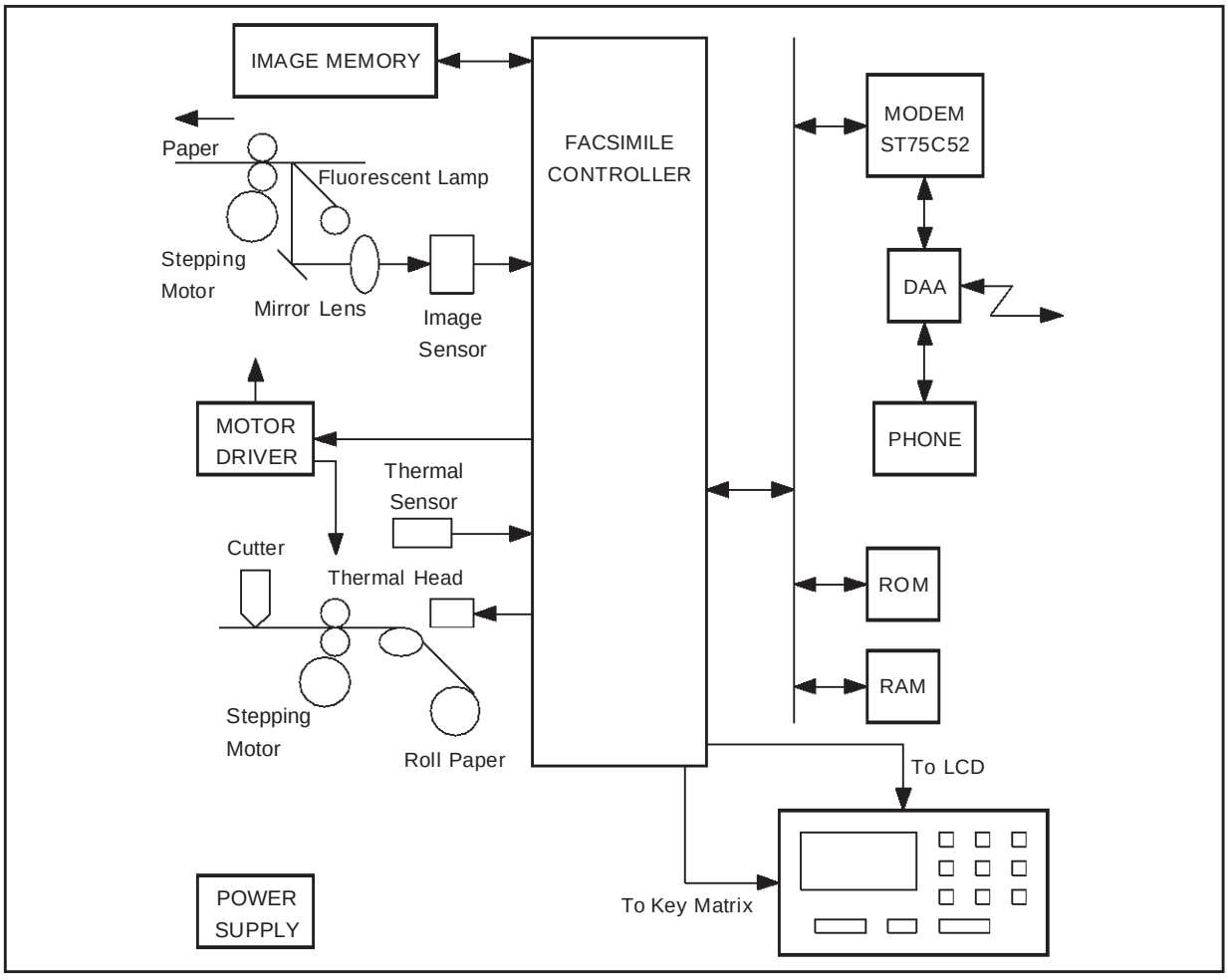
- default value or parameter will be followed by a *,
- all addresses are in hexadecimal,
- all numbers starting with a $ are hexadecimal, % are binary numbers, others are decimal numbers,
- bold italic words refer to key words used in the ST75C52/520 Data Sheet.

Note 1 : The ST75C52/520 only supports V.33 in a half duplex mode.

I.1 - FAX Architecture

The Figure 1 is an example of facsimile system (using thermal printer type) built with the ST75C52/520.

Figure 1



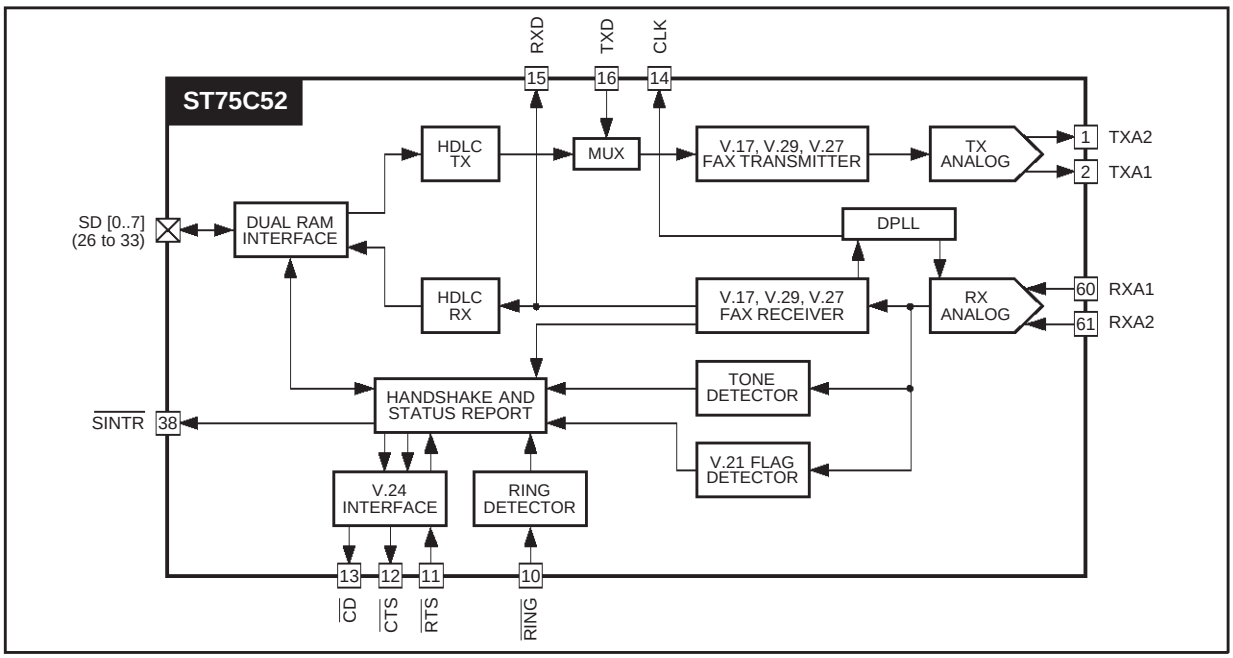
II - FEATURES

II.1 - Basic Functions

The ST75C52/520 provides the following functions :

- modulations for FAX implementation : ITU-T V.17, V.29, V.27 ter, V.21 ch2,
- basic low speed full duplex FSK modulations for special applications (VIDEOTEX, ...) : ITU-T V.23, V.21 and BELL 103,
- high speed modulations for faster FAX equipments : V.17, V.33 with the possibility to use the standard carrier frequency of 1800Hz or an optional frequency of 1700Hz,
- the optional short train sequence can be used in V.17 (for FAX equipment), V.29 (T104) recommendation) and V.27 ter for high speed VIDEOTEX application,
- integrated implementation on one single Digital Signal Processor (DSP) chip including intergrated Delta Sigma Modem Analog Front End (MAFE),
- single 5V power supply,
- a low power mode provides the possibility to reduce the power consumption till 5mW (typ),
- the DSP firmware allows a lot of operations such as :
  - full implementation of the V.17, V.33, V.29, V.27 ter handshakes,
  - real time status monitoring and full diagnostic capability,
  - auto dial and auto answer capability,
  - programmable tone detection and FSK V.21 flag pattern detection during high speed reception,
  - programmable call progress and call waiting tone detectors including DTMF,
  - programmable tone generators (DTMF and others),
  - programmable class detection capability,
  - voice mode using A-law to record or send messages,
  - full implementation of the HDLC protocol.
- the analog interface provides a wide dynamic range (> 48dB),
- initialisation and managment of the ST75C52/520 with commands given though the Dual Port Ram (DPR) interface,
- a versatile User Interface proposes different possibilities :
  - data transmission/reception with serial interface or with parallel interface,
  - parallel mode in synchronous transparent mode or in HDLC mode using in both cases 2x8 bytes data buffer in transmission and 2x8 bytes data buffer in reception,
  - connection with 8-bit data processor (both MOTOROLA or INTEL timing),
  - synchronization between the ST75C52/520 and the host processor by using interruption mode for different functions (transmission, reception, error detection, status managment, command acknowledge),
  - two 8-bit DACS for constellation display without any external components.

Figure 2 : Functional Diagram



II.2 - System Architecture

Figure 3 shows the basic connection between the ST75C52/520 and the different elements : telephone line interface, processor, synchronous/asynchronous serial, ...

Power

The modem/fax chip requires only one +5V Digital and Analog supply.

Hybrid and Telephone Line Interface

The sigma delta convertor provides the carrier on **TxA1** and **TxA2**. The far end carrier will be received on **RxA1** and **RxA2**. Both transmit and receive path are differential for better performance at low level. A hybrid interface must be used to connect the analog interface to the telephone line interface. At this point the hybrid interface and the line interface will be adjusted to meet the different technical requirements in each country (for example the reference impedance for the return loss can be real or complex, DC current features will be different ...). The incomming call detection could be easily facilitated using the **RING** detection of the ST75C52/520.

Serial Interface

Data communications in both half duplex and fullduplex modes are possible using the serial interface. The serial interface is optional since all the operations can be done through the DPR in parallel mode.

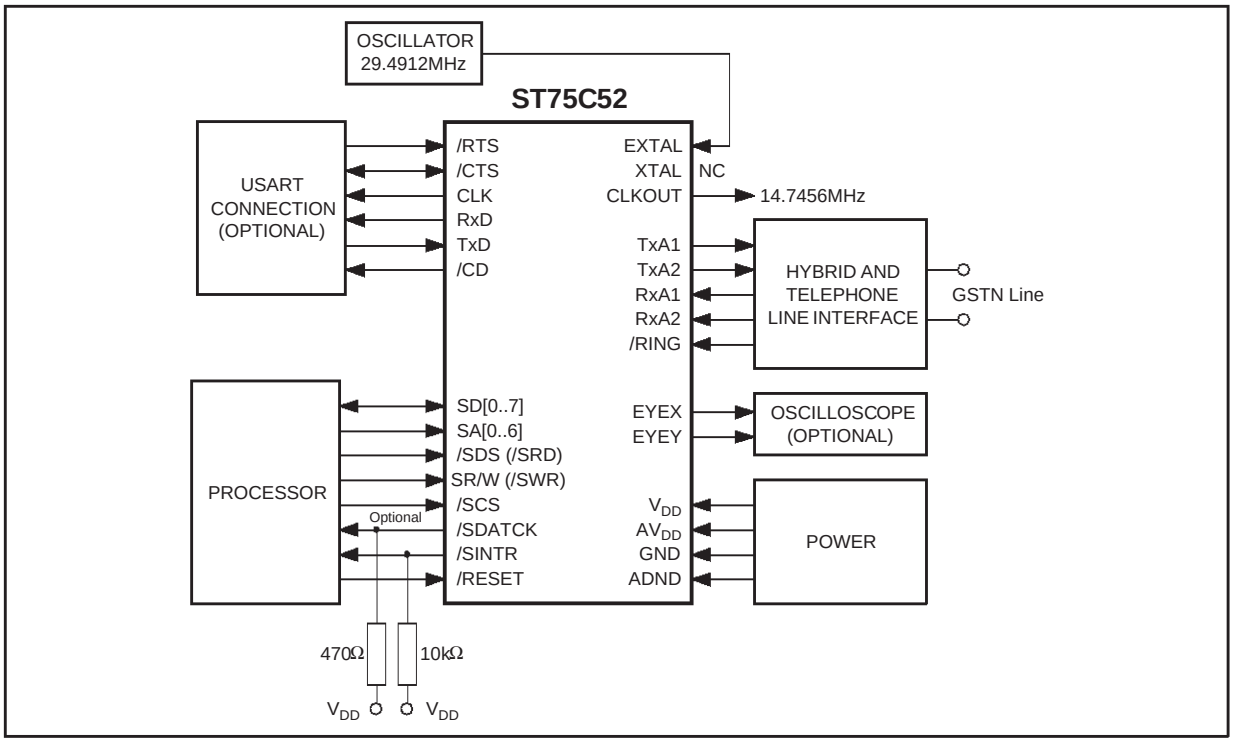
Processor Interface

Signals provide the possibility to use 8-bit data processors with both mode MOTOROLA and INTEL type. The processor can control the hardware initialisation with the **RESET** Pin. synchronization during read or write access are done with the **SDTACK** signal. Main program processor can be interrupted for special or priority purpose (data reception, status change...) with the **SINTR** signal. Both **SDTACK** and **SINTR** are open drain signals (external resistors must be installed) and must be tied to V_{DD} with 10kΩ for **SINTR** and 470Ω for **SDTACK**.

Oscillator

The ST75C52/520 provides the possibility to use a crystal on **EXTAL** and **XTAL** pin or an external oscillator can be used and connected to **EXTAL** pin. The nominal value is CLK = 29.4912MHz. When using a crystal we recommend to install a third harmonic quartz which is cheaper than a fundamental quartz. **CLKOUT** gives the internal ST75C52/520 (14.7456MHz or CLK/2).

Figure 3 : System Connection



II.3 - Operations

In this chapter we remind the user the main operations performed with the ST75C52/520.
Refer to the others chapters for more details.

II.3.1 - Modulation Method, Transmission Speed, Carrier Frequency

The modem implementation is fully compatible with current FAX modulation recommendations.
The modulation can be either Trellis Coded Modulation (TCM) as in V.17 14400, 12000, 9600, 7200 bps rates, Quadrature Amplitude Modulation (QAM) as in V.29 9600, 7200, 4800 and Differential Phase Shift Keying (DPSK) as in V.27 ter 4800 and 2400bps rates.
Frequency Shift Keying (FSK) modulations are also supported for V.21 ch2 300bps rate, full duplex V.21 300/300bps rates, full duplex V.23 75/1200 and 1200/75bps rates and BELL 103 300/300bps rate.

The Table 1 summarizes the different modes with their features.

II.3.2 - Transmitter Description

Data coming from the Data Terminal Equipment (DTE) both in parallel mode or in serial mode pass through the following modules shown on the Figure 4.

The different steps in transmission are :
- scrambling the data (scrambler block),
- coding the scrambled information (Diff encoder and trellis encoder block),
- conversion from real encoded data to complex encoded data (Signal mapping block),
- pulse shaping in a dedicated filter to avoid symbol interference (Pulse shaping block),
- modulation over the required carrier. After that we keep the real part of the signal,
- improve performance by using compromise equalizer (Comp equalizer block). Three compromise equalizers are available,
- selection of transmit gain,
- digital to analog conversion with a sigma delta convertor (D/A block).

II.3.3 - Receiver Description

The received carrier coming from the line is passed through the following modules showed in the Figure 5.

The different steps in reception are :
- analog to digital conversion with a sigma delta convertor (A/D block),
- filtering of the received information (RCV filter block) with result given on complex format,
- automatic control of the gain in reception (AGC block),
- equalization due to line impairment (equalizer block),
- slicer which gives real data for the decoder,
- decoder using first a Viterbi decoder (Viterbi decoder block) and second a differential decoder (diff decoder block),
- descrambling the data to obtain the initial sent data.

Table 1

Mode	Modulation	Carrier Frequency in Hz	Data Rate in bps ± 0/01%	Baud or Symbols/Sec	Bits per Symbol	Constellation Points
V.33/V.17 14400	TCM	1700 (2) 1800 (1)	14400	2400	6	128
V.33/V.17 12000	TCM	1700 (2) 1800 (1)	12000	2400	5	64
V.17 9600	TCM	1700 (2) 1800 (1)	9600	2400	4	32
V.17 7200	TCM	1700 (2) 1800 (1)	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27ter 4800	DSPK	1800	4800	1600	3	8
V.27ter 2400	DSPK	1800	2400	1200	2	4
V.21 High	FSK	1650,1850	300	300	1	-
V.21 Low	FSK	980,1180	300	300	1	-
V.23 High	FSK	1300,2100	1200	1200	1	-
V.23 Low	FSK	390,450	75	75	1	-
V.21 ch2	FSK	1650,1850	300	300	1	-

Notes : 1. ITU-T recommended carrier
2. Optional carrier

Figure 4

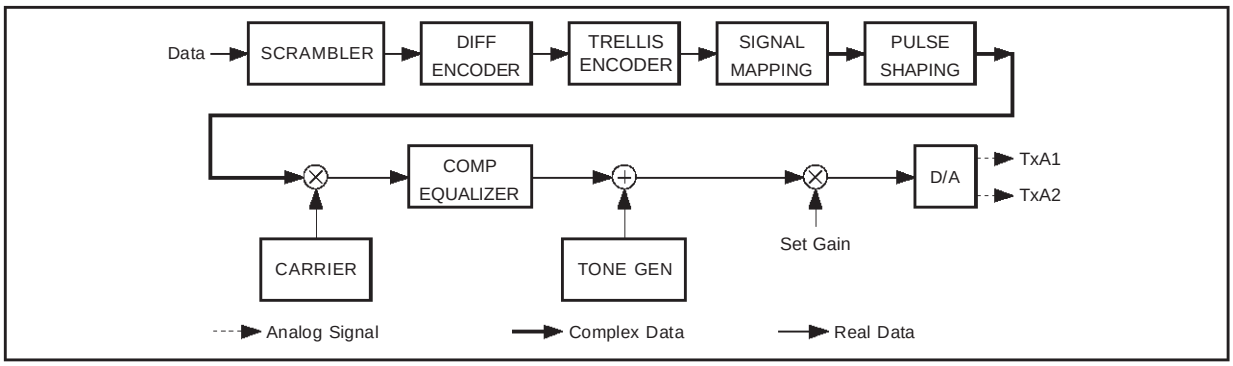
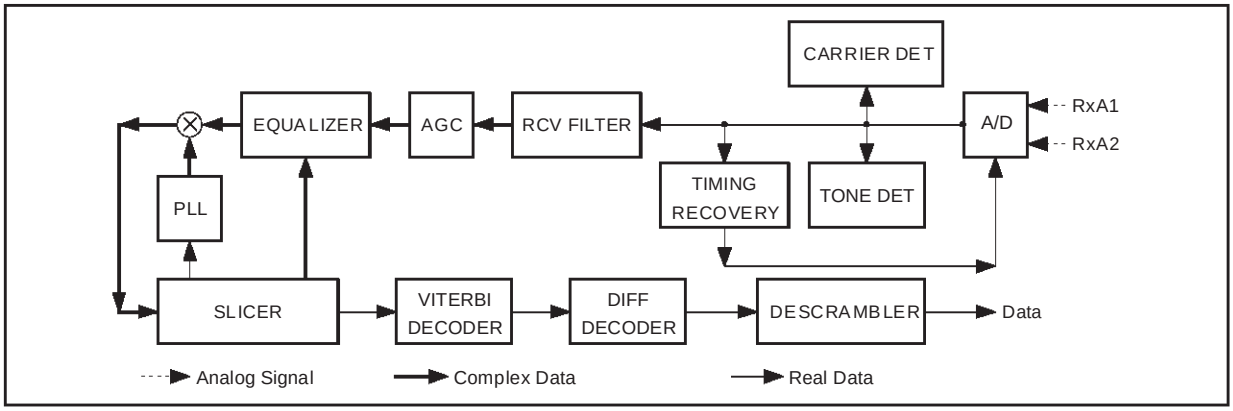


Figure 5



II.3.4 - Tone Generator Description

Four tones can be simultaneously generated by the ST75C52/520. The tones are determined by their frequencies and by the output amplitude level. A set of specific commands is also available for DTMF generation (using two of the four generators available).

II.3.5 - Tone Detector Description

Sixteen tones can be simultaneously detected by the ST75C52/520. Each of the tones to be detected is defined by the coefficients of a 4th order programmable IIR filter. Detection thresholds are also programmable from -45dBm up to -10dBm. DTMF detection is also available and is performed by a specific filter section that requires no programming.

II.3.6 - DTMF Detector Description

A DTMF Detector is included in the ST75C52/520, it allows detection of valid DTMF Digits. A valid DTMF tone is defined as a dual Tone with a total power higher than -35dBm, a duration higher than 40ms and a differential amplitude within 8dB (negative or positive).

II.3.7 - Voice Mode

The ST75C52/520 voice mode allows the implementation of enhanced telephone functions like answering machines. The incoming voice is sampled at a rate of 9600Hz. The samples, received from the line are PCM A-law coded and written into the dual port RAM. The outgoing samples are decompressed using the same A-law and output to the telephone line.

II.3.8 - Analog Loop Back Test Mode

In any transmission standard and serial data format, the ST75C52/520 can be configured for analog loop back test. This mode of operation is for test purposes only.

II.3.9 - Low Power Mode

A sleep state can be obtained by a **SLEEP** command. This is very interesting to reduce power consumption when no activity is detected by the processor in charge of the fax system equipment. The ST75C52/520 can be awakened with the **RESET** signal or the **RING** signal, or a dummy write into the Dual Port Ram. An interruption can be sent by the ST75C52/520.

The ST75C52 can only be awakened with the **RESET** signal.

II.3.10 - Reset

After a hadware reset, or an **INIT** command, the ST75C52/520 clears all its internal memories, clears the whole dual RAM and starts to initialize the delta sigma analog convertors. As soon as these initialization are completed, the ST75C52/520 clears the dual RAM address 0 (**COMSYS**), generates an interrupt **IT6 (command acknoledge)** and is programmed to send and receive tones, the bit clock and the sample clock are programmed to 9600Hz. The total duration of the reset sequence is about 5ms. After that time the ST75C52/520 is ready to execute commands sent by the host micro-controller.

We suggest that the **RESET** signal is managed by the host micro-controller using a general purpose output port. In such a case the **RESET** signal could be equal to 0 till the micro-controller initialize it to 1 at the entry point of the main program, and software initialization could be done both by the **RESET** or the **INIT** command.

For a hardware reset the signal **RESET** must be tide to GND at least 700ns (see Figure 6).

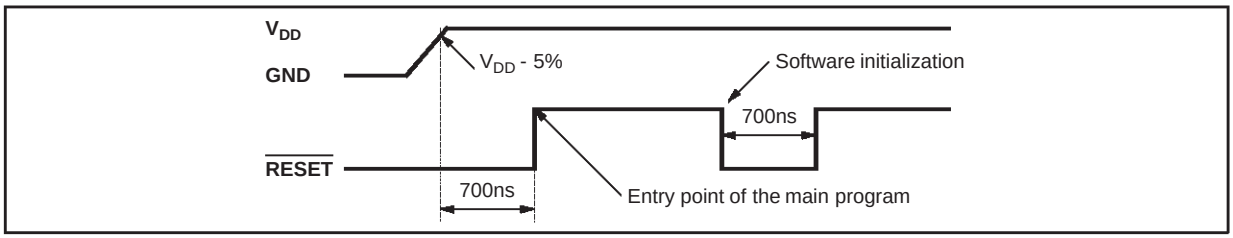
II.3.11 - Analog Interface

The modem designer must provide a proper hybrid interface to the ST75C52/520. Analog hybrid examples are given in this User's Manual. The inputs and the outputs of the MAFE are differential, achieving thus a better noise immunity. The D/A converter output amplifier includes a single pole low-pass filter, its cut-off frequency is : Fc -3dB # 19200Hz. Continuous-time filtering of the analog differential output is necessary using an off-chip amplifier and a few passive components.

II.3.12 - Host Interface

The host interface is seen by the micro-controller as a 64x8 RAM, with additional registers accessible through a 7-bit address space. A selection pin (**INT/MOT**) allows to configure the host bus for either INTEL or MOTOROLA type control signals.

Figure 6



Note : The interrupt registers ITMASK and ITSRCR are not changed by an **INIT** command.

II.4 - Hardware Block Diagram

Figure 7

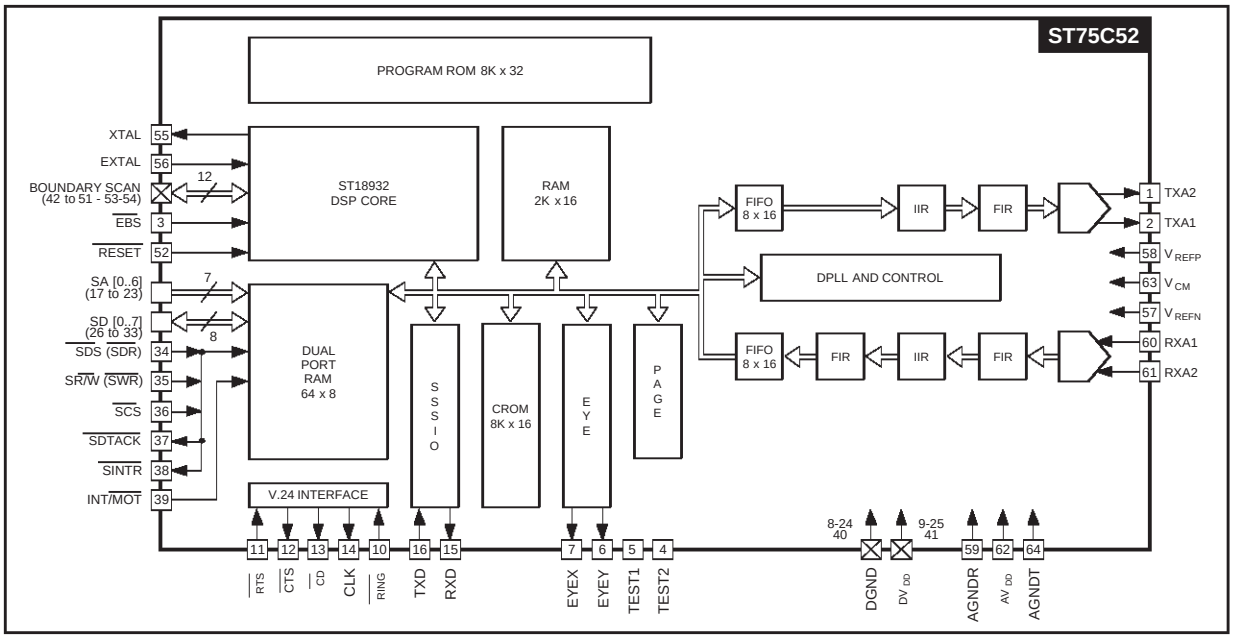


Table 2 : Pin Connections

Pin Name	Type	Pin Number
TxA2	Output	1
TxA1	Output	2
$\overline{EBS}$	Input	3
TEST2	To be left open	4
TEST1	To be left open	5
EYEY	Output	6
ETEX	Output	7
GND	Ground	8
V_{DD}	Digital +5V	9
$\overline{RING}$	Input	10
$\overline{RTS}$	Input	11
$\overline{CTS}$	Output	12
$\overline{CD}$	Output	13
CLK	Output	14
Rxd	Output	15
TxD	Input	16
SA0	Input	17
SA1	Input	18
SA2	Input	19
SA3	Input	20
SA4	Input	21
SA5	Input	22
SA6	Input	23
GND	Ground	24
V_{DD}	Digital +5V	25
SD0	Input / Output	26
SD1	Input / Output	27
SD2	Input / Output	28
SD3	Input / Output	29
SD4	Input / Output	30
SD5	Input / Output	31
SD6	Input / Output	32

Pin Name	Type	Pin Number
SD7	Input / Output	33
$\overline{SDS}$ ($\overline{SRD}$)	Input	34
SR/$\overline{W}$ ($\overline{SWR}$)	Input	35
$\overline{SCS}$	Input	36
$\overline{SDTACK}$	Output open Drain	37
$\overline{SINTR}$	Output open Drain	38
INT/$\overline{MOT}$	Input	39
GND	Ground	40
V_{DD}	Digital +5V	41
SCIN	Input	42
SCCLK	Input	43
MCI	Output	44
RDYS	Output	45
MC2	Input	46
MC1	Input	47
MC0	Input	48
EOS	Input	49
BOS	Input	50
SCOUT	Output	51
$\overline{RESET}$	Input	52
$\overline{HALT}$	Input	53
CLKOUT	Output	54
XTAL	Output	55
EXTAL	Input	56
V_{REFN}	Input	57
V_{REFP}	Input	58
AGNDR	Analog Ground	59
RxA1	Input	60
RxA2	Input	61
AV_{DD}	Analog +5V	62
VCM	Input / Output	63
AGNDT	Analog Ground	64

III - G3 FAX EQUIPMENT

III.1 - T.30 Protocol

The ITU-T recommendation T.30 explains the procedures for the facsimile transmission over the public telephone network. The recommandation describes how to initiate, transmit (receive) and close a fax communication.
T.30 recommandation uses five phases called A, B, C, D, E.

Phase A : communication establishment
Phase B : preliminary operations for indentification , request and recognition of the possibilities (group, speed, resolution, ...)
Phase C : high speed message transmission with eventually phase adjust and synchronization
Phase D : post-message procedure including end message, confirmation and procedures for multiple documents
Phase E : end of communication

III.1.1 - Phase A

Four methods are possible for the establishment (manual to manual, manual to automatic, automatic to manual, and automatic to automatic). Manual means a human action while automatic means a machine attempt.
Here are details for an automatic to automatic establishment (usually done by complete facsimile system).

Calling Unit	Answering Unit
Off-Hook	
Dialtone detection	
Dials the Fax number	
Sends the calling tone (CNG tone at 1100Hz) and waits to the answer tone (CED tone at 2100Hz)	Incoming call detection off-Hook sends the answer tone (CED at 2100Hz)

Remark : some of manufactures wait for the preamble (HDLC flag with V.21 ch2 modulation) instead of the CED tone.

III.1.2 - Phase B

The preliminary procedure uses the following sequence :
- the answering unit sends the preamble, the identification signal,
- the calling unit waits for the preamble, identification signal and answers with a command signal,
- the transmitting unit sends a training at high speed (V.17 or V.29 or V.27 ter),
- the receiving unit answers to confirm that the training was correct.

The identification, command and answer signals are sent using HDLC protocol over V.21 ch2 Frequency Shift Keying (FSK) modulation.
The preamble is a series of HDLC flags during one second ±15%.

Remark : Identification, command and answer signals are called normalized HDLC frames. Some others frames which are optional can be sent including special information (FAX phone number...) before the identification signal.

Here is an example for phase B where the calling unit wants to send page(s).

Calling Unit	Answering Unit
Detect carrier	Send V.21 ch2 carrier
Get preamble	Send preamble
Get DIS frame	Send DIS frame
Detect loss of carrier	Cut off carrier
Send V.21 ch2 carrier	Detect carrier
Send preamble	Get preamble
Send DCS frame	Get DCS frame
Cut off carrier	
Set up to high speed	Set up to high speed
Send V.17 carrier	Detect V.17 carrier
Send TCF data	Get TCF data
Cut off carrier	
Detect carrier	Send V.21 ch2 carrier
Detect preamble	Send preamble
Get CFR frame	Send CFR frame
Detect loss of carrier	Cut off carrier

DIS frame : Digital Identification Signal (DIS) sent by the answering unit to inform the calling unit about its possibilities (group, data rate, resolution...).

DCS frame : Digital Command Signal (DCS) sent by the calling unit to inform the answering unit about the choices for this facsimile communication.

TCF : Training Check Frame (TCF) sent by the calling unit. During TCF the calling unit sends a series of zeroes for a time duration of 1.5s ±10%.

CFR : Configuration to Receive (CFR) is sent by the answering unit to inform the calling unit of a complete successful preliminary procedure (go to phase C). In case where the training fails the answering unit will send the Failure to Train frame (FTT) instead of the CFR frame. In such a case the protocol goes to the DCS step untill the CFR is received by the calling unit.

III.1.3 - Phase C

After completed training in phase B the data are transferred at high speed. The data are com-Pressed with the standard Modified Huffman (MH) or Modified Read (MR) algorithm before being sent. At the receive end the data will be decompressed.

Phase C starts with End of Line (EOL) character. The data following the first EOL until the end of the line. A new line begins with another EOL character. Six EOL characters mean the end of the document transmission and Return To Control (RTC) command.

Normally data are sent in the high speed (V.17 or V.29 or V.27 ter) mode in phase C but a classification signal in the low speed mode (V.21 ch2 with HDLC) may be sent if the handshake fails (CFR was sent by the answering unit but not received by the calling unit due to line distortion...). In such a case the calling unit will return to the procedure to perform DCS (Digital Command Signal). Therefore, the facsimile must wait in high speed mode and with low speed flag detection active.

Calling Unit	**Answering Unit**
Send V.17 carrier	Detect carrier
Send page data	Receive data
Cut off carrier	Detect loss of carrier

III.1.4 - Phase D

Phase D determines whether to terminate or continue Data Tranmission using the HDLC protocol using V.21 ch2 modulation.

Typically the calling unit will send End Of Message (EOM) or Multiple Page signal (MPS) or End Of Procedure (EOP) signal. The answering unit responds to an EOM, MPS or EOP signal with a Message Confirmation (MCF) command.

EOM frame : Informs that it is the end of the page and asking for parameters renegotiation, the protocol FAX goes to phase B.

MPS frame : Signals to the answering unit that there are more pages.

EOP frame : Signals to the answering unit the end of the data transmission (no more pages).

Here is an example with the End Of Procedure signal sent by the calling unit.

Calling Unit	**Answering Unit**
Send V.21 ch2 carrier	Detect carrier
Send preamble	Detect preamble
Send EOP frame	Receive EOP
Cut off carrier	
Detect carrier	Send V.21 ch2 carrier
Receive preamble	Send preamble
Get MCF frame	Send MCF frame
Detect loss of carrier	Cut off carrier

III.1.5 - Phase E

Phase E is executed with an HDLC format cutoff command signal (usually Disconnect (DCN) command).

Calling Unit	**Answering Unit**
Send V.21 ch2 carrier	Detect carrier
Send preamble	Detect preamble
Send DCN frame	Receive DCN
Cut off the carrier	
Hang up	Hang up

III.2 - G3 Transmission (Setup and Training)

III.2.1 - Transmit in High Speed Mode (HM)

The high speed mode uses V.17 or V.29 or V.27 ter ITU-T standards. For each modulation method more than one data rate is possible but only one will be chosen at the end of phase B. We simply summarize hereafter the different possibilities for every modulation. The parameters (P1 to P4) for the CONF command are given too.

Be careful that the V.17 long train is only used at the first time (in PHASE B) when sending the TCF signal. After that the short train option must be used. To select the short train sequence use the MODC command with the first parameter equal to $40 and to select the long train sequence use the same command with the first parameter equal to $00.

In this example we do not select the transmit equalizer, the RTS signal is not used and the standard 1800Hz ITU-T carrier is chosen in V.17.

Modulation	**Data Rate (bps)**	**CONF**	**P1**	**P2**	**P3**	**P4**
V.17	14400	CONF	$0F	$09	$00	$04
V.17	12000	CONF	$0F	$09	$00	$02
V.17	9600	CONF	$0F	$09	$00	$01
V.17	7200	CONF	$0F	$09	$80	$00
V.29	9600	CONF	$0F	$08	$00	$01
V.29	7200	CONF	$0F	$08	$80	$00
V.29	4800	CONF	$0F	$08	$40	$00
V.27 ter	4800	CONF	$0F	$07	$40	$00
V.27 ter	2400	CONF	$0F	$07	$20	$00

The typical sequence to set up the ST75C52/520 could be :

STEP_1 : Select modulation, data rate with **CONF** command.

STEP_2 : Start the training sequence with the **HSHK** command. It is also possible to start the training sequence with the **RTS** Pin if the ST75C52/520 is setup for such a control (**CONF_V24** bit 7 in the first parameter of **CONF** command must be equal to 1). RTS signal can be used in both mode parallel and serial.

STEP_3 : Check that **STA_H** (bit 0 in **STATUS[1]** of Modem General Status) equals 1 (this step is optional).

STEP_4 : Wait until **STA_106** (bit 2 in **STATUS[0]** of Modem General Status) equals 1.

STEP_5 : In parallel mode to use interrupts for data transmission enable **IT2** interrupt with Interrupt Mask Register **ITMASK** doing ITMASK = ITMASK or $84.

Start to transmit Data :
IF parallel mode
SERIAL 01
FORM 00
fill the first buffer (buffer 0)
enable **IT2**
send **XMIT 1** command
send Data with TX buffers every **IT2** interrupt
else
send Data on **TxD** pin

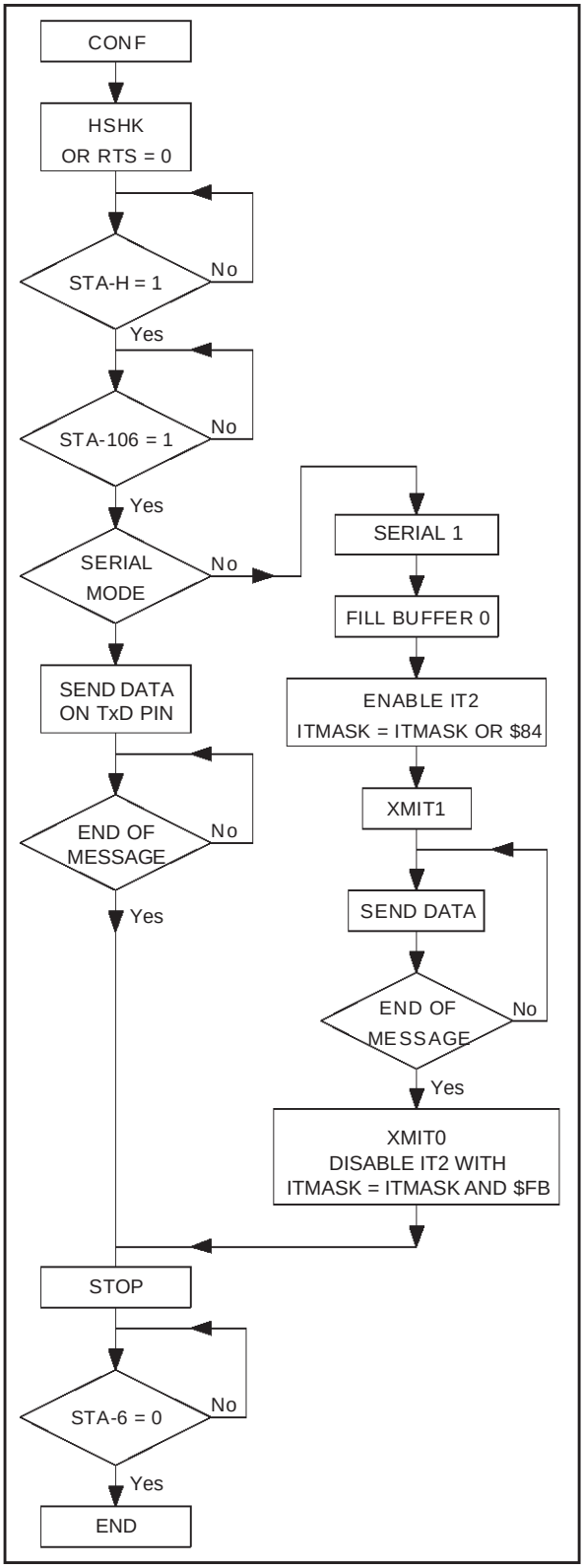
STEP_6 : Stop transmitting Data. In parallel mode send **XMIT 0** command. Disable **IT2** interrupt with Interrupt Mask Register **ITMASK** doing ITMASK = ITMASK and $FB.

STEP_7 : Stop sending carrier with **STOP** command.

STEP_8 : Wait end of ITU-T stop sequence (**STA_106 = 0**).

The following flow chart summarizes the above sequence.

Figure 8



III.2.2 - Transmit in Low Speed Mode (LM)

The low speed uses channel 2 of the V.21 ITU-T standard in phase B, D and E to send signal with HDLC protocol over the PSTN network.

The ST75C52/520 gives two posibilities :

- The HDLC is done with an external component. In such a case the transmit data are sent with the serial mode (TxD Pin).
- The ST75C52/520's HDLC controller is used to send data. The ST75C52/520 must be setup for parallel mode and HDLC format.

The typical sequence to set up the ST75C52/520 in parallel mode with HDLC could be :

STEP_1 : Select V.21 ch2 with **CONF $0F $0D $00 $00** command (in this example the **RTS** signal is not used).

STEP_2 : Start to send the carrier with **HSHK** command.

STEP_3 : Check that **STA_H** (bit 0 in **STATUS[1]** of Modem General Status) equal 1 (this step is optional).

STEP_4 : Wait until **STA_106** (bit 2 in **STATUS[0]** of Modem General Status) equal 1.

STEP_5 : Select parallel mode with **SERIAL 1** command.
Select HDLC format with **FORM 2** command.

STEP_6 : Send preamble (the HDLC controller sends flags during one second). To do that send **XMIT 1** command and wait one second.

STEP_7 : To use interrupts for data transmission enable **IT2** interrupt with Interrupt mask register **ITMASK** doing ITMASK = ITMASK or $84.

Start to transmit data :
Fill the first Tx buffer (buffer 0).
Setup **BUFF_SFRM** (bit 4 of the transmit buffer status word **DTTSB0**) to 1 to indicate Start of Frame.
Enable **IT2**
Continue to send data with Tx buffers (**BUFF_SFRM** and **BUFF_EFRM** respectively bit 4, 5 of **DDTTSB0** and **DDTSB1** must be equal to 0).

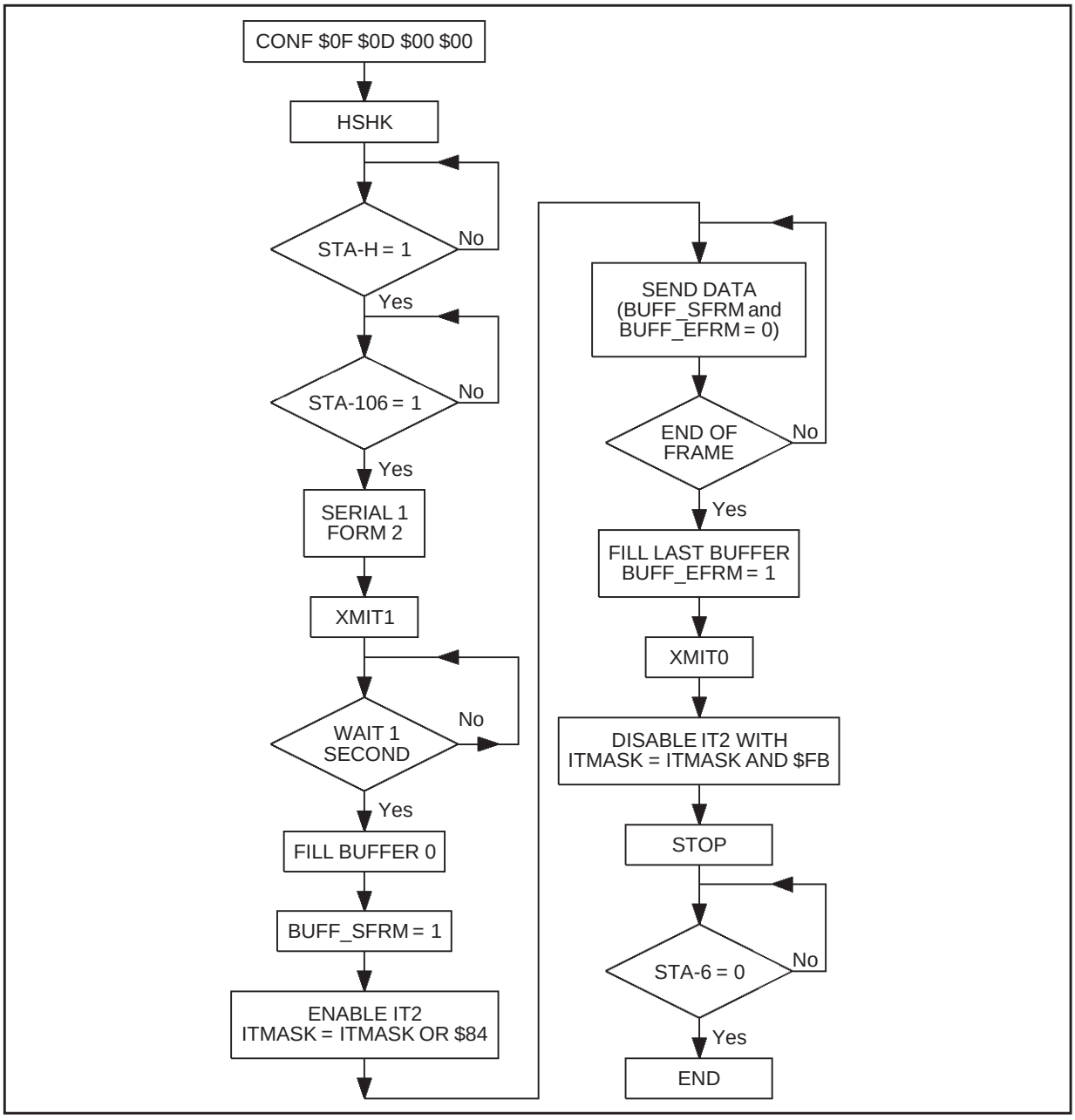
STEP_8 : Stop the data transmission :
Fill the last Tx buffer with data.
Setup **BUFF_EFRM** (bit 5 of **DTTSBX** with x = 0 or 1 respectively for buffer 0 and 1) to 1 to indicate End of Frame.
Send **XMIT 0** to stop data transmission. Desable **IT2** with Interrupt Mask Register **ITMASK** doing ITMASM = ITMASK and $FB.

STEP_9 : Stop sending carrier with **STOP** command.

STEP_10 : Wait end of **STOP** sequence (**STA_106** equal to 0).

The following flow chart summarizes the above sequence.

Figure 9



The typical sequence to set up the ST75C52/520 in serial mode could be :

STEP_1 : Select V.21 ch2 with **CONF $0F $0D $00 $00** command (in this example we do not select the transmit equalizer, the **RTS** signal is not used).

STEP_2 : Select serial mode with **SERIAL $00** command.

STEP_3 : Start to send the carrier with **HSHK** command.

STEP_4 : Check that **STA_H** (bit 0 in **STATUS[1]** of Modem General Status) equal 1 (this step is optional).

STEP_5 : Wait until **STA_106** (bi 2 in **STATUS[0]** of Modem General Status) equal 1.

STEP_6 : Send preamble (HDLC flag during one second) with **TxD** Pin.

STEP_7 : Start to transmit data on **TxD** Pin.

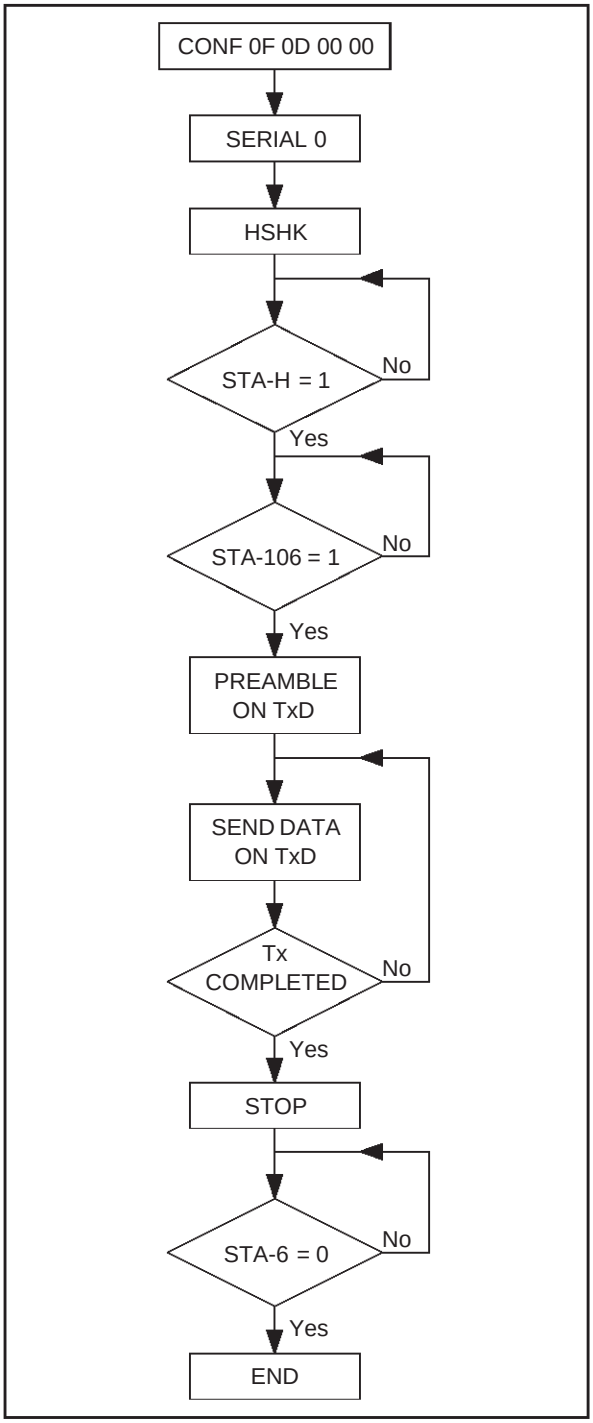
STEP_8 : Stop the data transmission on **TxD** Pin.

STEP_9 : Stop to send carrier with **STOP** command.

STEP_10 : Wait end of **STOP** sequence (**STA_106** equal to 0).

The following flow chart summarizes the above sequence.

Figure 10



III.3 - G3 Reception (Setup and Synchronization)

III.3.1 - Reception in Phase A

Two cases are possible : the ST75C52/520 is in the calling unit or in the called unit (answering unit).

In the first case (calling unit) the ST75C52/520 is used to detect busy tone, answer tone and preamble.

In the second case (called unit) the ST75C52/520 detects the calling tone (CNG tone at 1100Hz) to recognize an automatic fax call.

The following sequence is an example to set up and to use the ST75C52/520 in the calling unit.

The ST75C52/520 send CNG tone, detect busy tone, answer tone and V.21 channel 2 flag.

STEP_1 : Start a time out (e.g 30s to 60s).

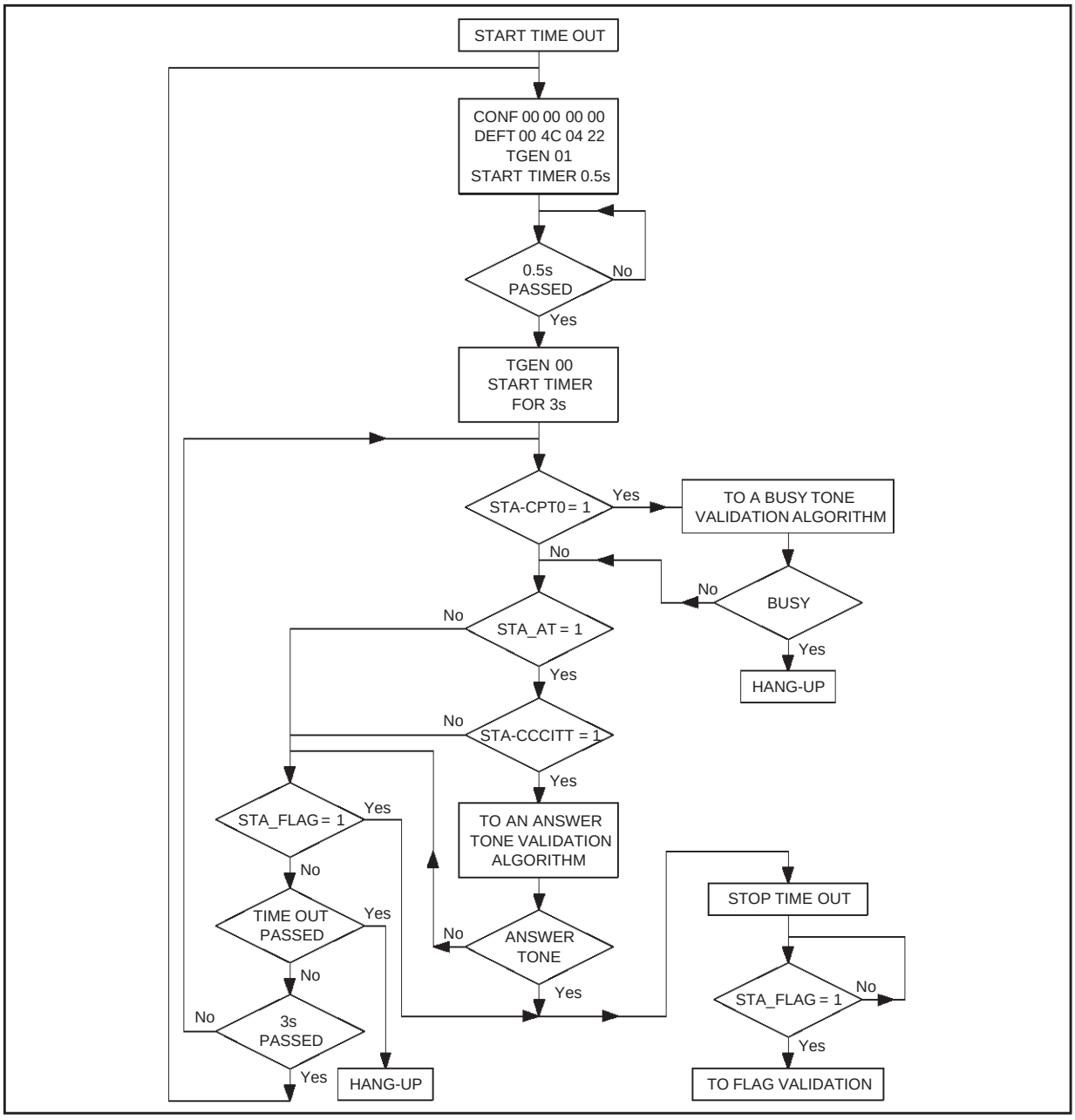
STEP_2 : Setup the ST75C52/520 to send 1100Hz (CNG tone), detect busy tone, answer tone and V.21 flag with the following commands :
CONF $00 $00 $00 $00
DEFT $00 $4C $04 $ZZ (ZZ depend of the wanted level, ZZ = $30 for nominal value).
TGEN $01
wait 0.5s.

STEP_3 : Stop sending CNG tone with **TGEN $00** command and start a timer for 3 seconds.

STEP_4 : If **STA_CPT0** (bit 4 in **STATUS[0]** of Modem General Status) equal 1 begin a Busy tone validation algorithm.
If **STA_AT** and **STA_CCITT** (bits 3 and 2 in **STATUS[1]** of Modem General Status) equal 1 begin an Answer tone validation algorithm.
If **STA_FLAG** (bit 6 in **STATUS[1]** of Modem General Status) equal 1 begin flag detection (preamble).
If no detection and timer 3s is not elapsed go to the beginning of STEP_4.
If timer 3s is elapsed go to STEP_2 and repeat until Time out.

The following flow chart summarizes the above sequence.

Figure 11



The following sequence is an example to setup and to use the ST75C52/520 in the called unit.

The ST75C52/520 detects the CNG tone and after detection sends the answer tone.

STEP_1 : Start a timer for 4 second.

STEP_2 : Setup the ST75C52/520 to detect tone with the **CONF $0 $00 $00 $00** command.
After that the ST75C52/520 will indicate with **TDT8** (bit 0 in **STAOP1** of Optional Status) equal 1 the 1100Hz detection.

STEP_3 : Validation of the 1100Hz

STEP_4 : Send answer tone (2100Hz) with **TONE $10** command.
Wait 3.3 second and stop sending 2100Hz with **TGEN $00** command.

Note : Detection of the CNG tone could be optional, since the calling unit can be manual.

The flow chart (Figure 12) summarizes the above sequence.

III.3.2 - Reception in Phase B

As in phase A two cases are possible. In the first case the ST75C52/520 detects and receives preamble, HDLC frame over V.21 ch2 modulation. In the second case the ST75C52/520 detects and receives training over High speed standards (V.17 or V.29 or V.27 ter).

Hereafter is an example to setup the ST75C52/520 to detect and receive preamble, HDLC frame over V.21 ch2 (use parallel mode).

STEP_1 : Setup V.21 ch2 with **CONF $0F $0D $00 $00** command.
Arm the receiver with **SYNC $01** command.
Wait until a V.21 ch2 signal is received by testing **STA_109** (bit 0 in **STATUS[0]** of Modem General Status) equal 1.

STEP_2 : Wait until HDLC flag is received (preamble) with **STA_FLAG** (bit 6 in **STATUS[1]** of Modem General Status) equal 1.

STEP_3 : Enable Parallel reception (**IT3** interrupt) with the following sequence :
write $00 into **DTRBF0**
write $00 into **DTRBF1**
enable **IT3** doing ITMASK = ITMASK or $88
select HDLC and parallel format with **FORM $02** and **SERIAL $02** commands.

The flow chart (Figure 13) summarizes the above sequence.

Figure 12

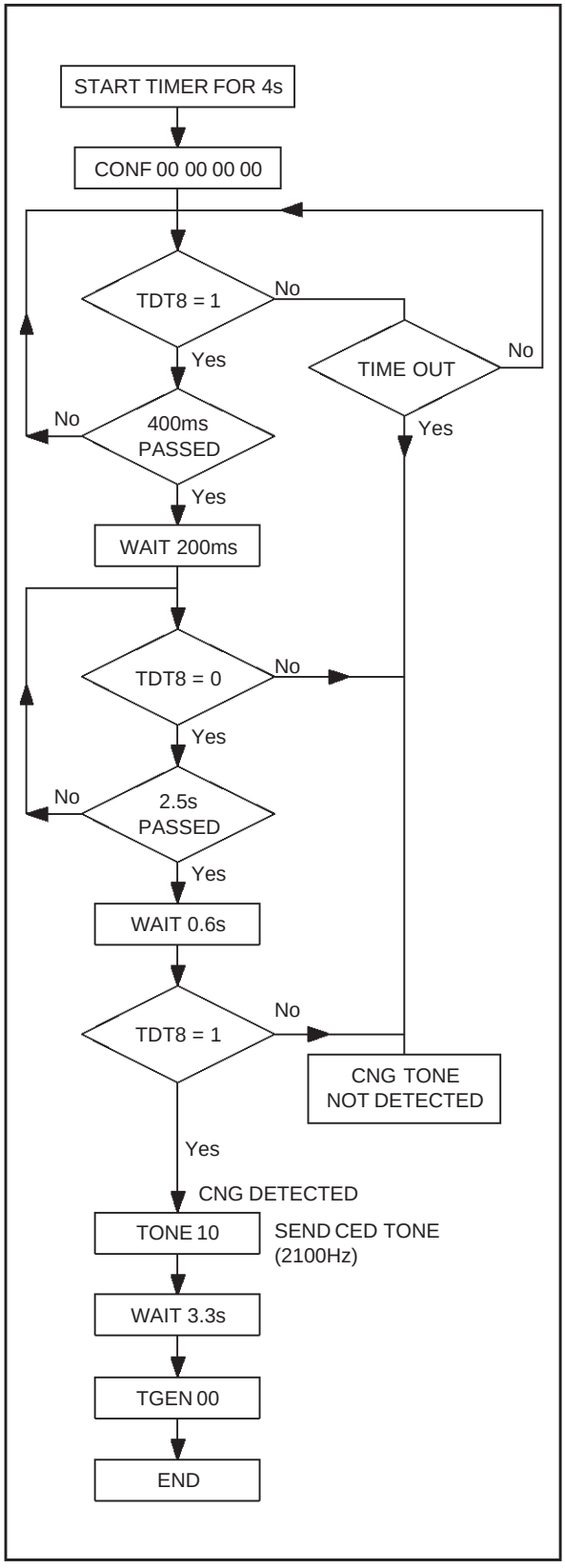
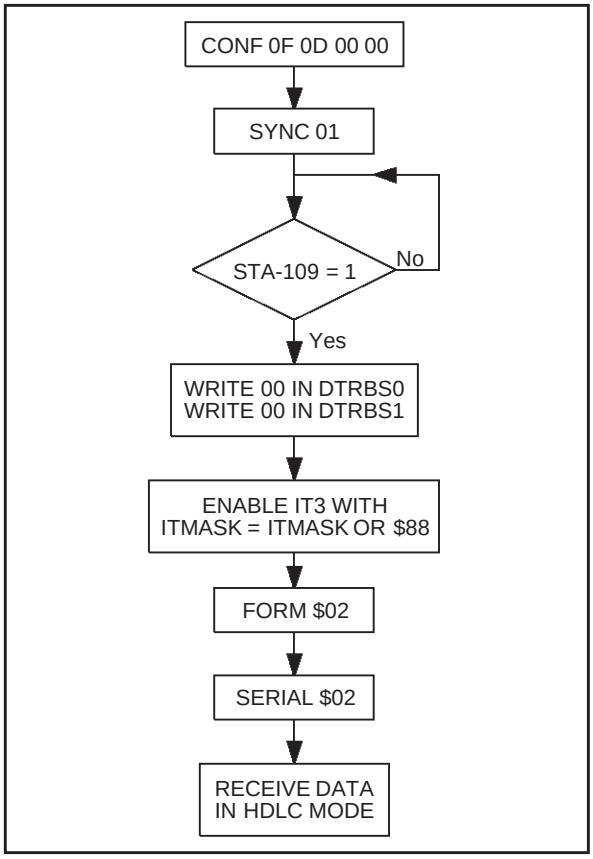


Figure 13



Hereafter is an example to setup the ST75C52/520 to detect V.21 ch2 carrier and after that to be used in serial mode.

STEP_1 : Setup V.21 ch2 with **CONF $0F $0D $00 $00** command.
Send **SERIAL $00** to use serial interface.
Arm the receiver with **SYNC 1** to detect V.21 ch2 carrier.

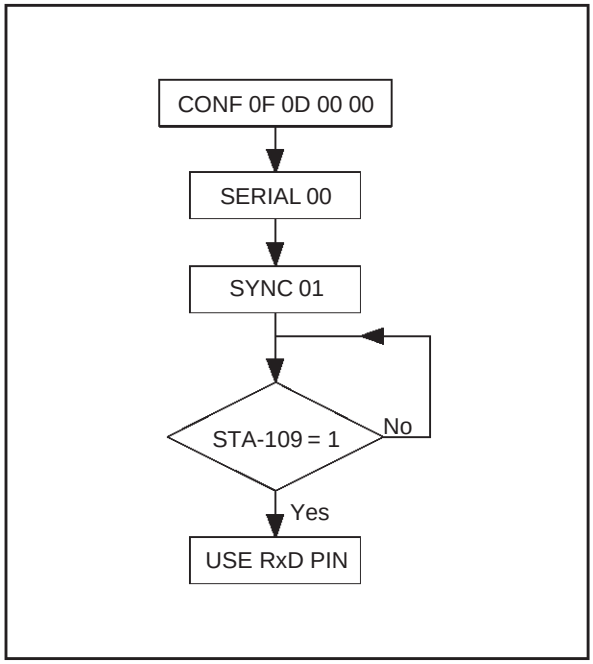
STEP_2 : Wait **STA_109** (bit 0 in **STATUS[0]** of Modem General Status) equal 1 or **CD** Pin equal 0.

STEP_3 : Receive Preamble and Data Frame on **RxD** Pin.

The flow schart (Figure 14) summarizes the above sequence.

In phase B the two units select a high speed among the different possibilities (V.17, V.29 or V.27 ter). At this point the transmitting unit must send a training check (TCF) with the selected speed. The receiving unit must be set up to receive it.
Please see the Table given at chapter III.1.2 for CONF's parameters for all the high speed possibilities.

Figure 14



For parallel reception the typical sequence to setup the ST75C52/520 could be :

STEP_1 : Select modulation, data rate with **CONF** command.

STEP_2 : Arm the receiver with **SYNC $01** command.

STEP_3 : Wait for the beginning of the receive synchronization by testing **STA_HR** (bit 4 in **STATUS[1]** of Modem General Status) equal 1 (this step is optional).

STEP_4 : Wait for the end of the receive synchronization and the beginning of the data mode by testing **ST_109** (bit 0 in **STATUS[0]** of modem General Status) equal 1.

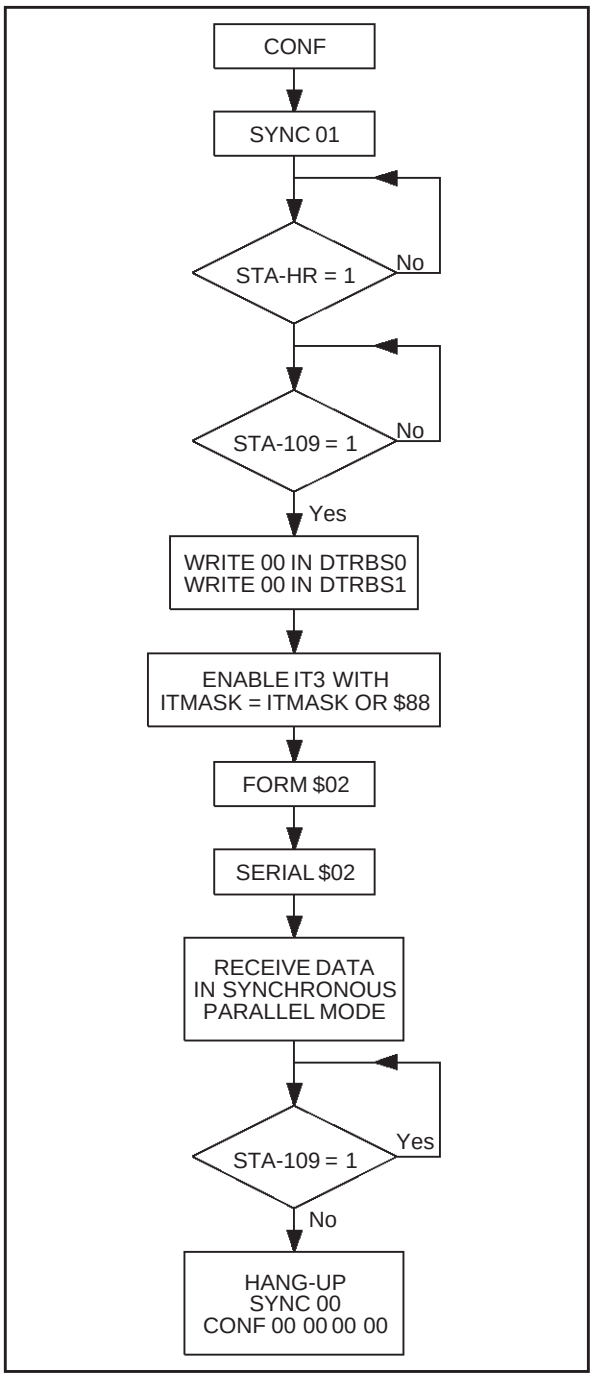
STEP_5 : Enable parallel reception (IT3 interrupt) with the following sequence.
write $00 into **DTRBF0**
write $00 into **DTRBF1**
enable **IT3** doing ITMASK = ITMASK or $88
select synchronous parallel format with **FORM $00** and **SERIAL $02** commands.

STEP_6 : Receive data. If **STAT_109** equal 0 go to STEP_7.

STEP_7 : Hang_up.

The flow chart (Figure 15) summarizes the above sequence.

Figure 15



For serial reception the typical sequence to set up the ST75C52/520 could be :

STEP_1 : Select modulation, data rate with **CONF** command.

STEP_2 : Arm the receiver with **SYNC $01** command.

STEP_3 : Wait for the beginning of the receive synchronization by testing **STA_HR** (bit 4 in **STATUS[1]** of Modem General Status) equal 1 (this step is optional).

STEP_4 : Wait until the end of the receive synchronization and the beginning of the data mode by testing **ST_109** (bit 0 in **STATUS[0]** of modem General Status) equal 1.

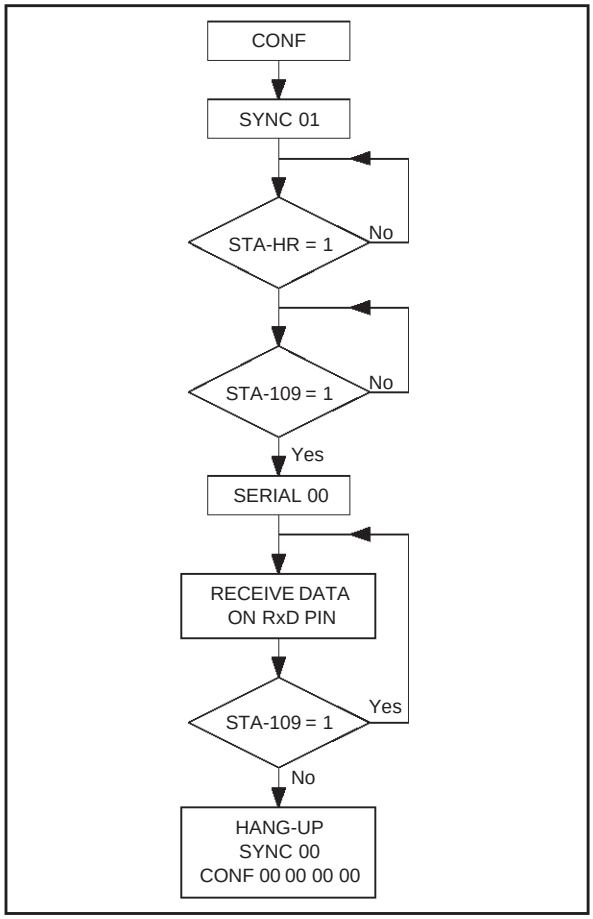
STEP_5 : Select serial mode with **SERIAL $00** command.

STEP_6 : Receive data on **RxD** Pin. If **STAT_109** equal 0 go to STEP_7.

STEP_7 : Hang_up.

The flow chart (Figure 16) summarizes the above sequence.

Figure 16



III.3.3 - Reception in Phase C

As explained in Chapter III.1.3 the receiving unit must be able to detect reception in both modes (high speed and low speed).

Please see the Table given at Chapter III.1.2 for CONF's parameters for all the high speed possibilities.

Be careful that in V.17 the long train sequence is only allowed for the TCF in phase B, that is why the V.17 will always use the short train sequence in phase C. The **MODC** command with its first parameter equals $40 will select the short train sequence (the same parameter equal to $00 selects the long train sequence).

For parallel reception in phase C the following sequence could be :

STEP_1 : Select modulation data rate with **CONF** command.

STEP_2 : If V.17 short train requested send **MODC $40 $00** command.

STEP_3 : Arm the receiver with **SYNC $01** command.

STEP_4 : If **STA_FLAG** (bit 6 in **STATUS[1]** of Modem General Status) equals 1 go to STEP_9.
If **P2s** (bit 1 in **STAOP2** of the Optional Status) equal 1 go to STEP_5.

STEP_5 : If **STA_FLAG** equal 1 go to STEP_9.
If **PNDETs** (bit 5 in **STAOP2** of the Optional Status) equals 1 go to STEP_6.

STEP_6 : Wait until **STA_109** (bit 0 in **STATUS[0]** of the Modem General Status) equal 1.

STEP_7 : STEP_7 : Enable parallel reception (**IT3** interrupt) with the following sequence :
write $00 into **DTRBF0**
write $00 into **DTRBF1**
enable **IT3** doing ITMASK = ITMASK or $88
select synchronous parallel format with **FORM $00** and **SERIAL $02** commands.

STEP_8 : Receive data. If **STA_109** equal 0 go to STEP_13.

STEP_9 : Stop synchronization with **SYNC 0** command.
Setup V.21 ch2 with **CONF $0F $0D $00 $00** command.
Arm the receiver with **SYNC $01** command.

STEP_10 : wait until **STA_109** equal 1.

STEP_11 : Enable HDLC, parallel reception and **IT3** interrupt with the following sequence :
write $00 into **DTRBF0**
write $00 into **DTRBF1**
enable **IT3** doing ITMASK = ITMASK or $88
select HDLC, parallel format with **FORM $02** and **SERIAL $02** commands.

STEP_12 : Receive data. If **STA_109** equal 0 go to STEP_13.

STEP_13 : Hang_up.

The flow chart (Figure 17) summarizes the above sequence.

For serial reception in phase C the following sequence could be :

STEP_1 : Select modulation data rate with **CONF** command.
Select serial mode with **SERIAL $00** command.

STEP_2 : If V.17 short train requested send **MODC $40 $00** command.

STEP_3 : Arm the receiver with **SYNC $01** command.

STEP_4 : If **STA_FLAG** (bit 6 in **STATUS[1]** of Modem General Status) equal 1 go to STEP_7.
If **P2s** (bit 1 in **STAOP2** of the Optional Status) equal 1 go to STEP_5.

STEP_5 : If **STA_FLAG** equal 1 go to STEP_7.
If **PNDETs** (bit 5 in **STAOP2** of the Optional Status) equal 1 go to STEP_6.

STEP_6 : Wait until **STA_109** (bit 0 in **STATUS[0]** of the Modem General Status) equal 1 and than go to STEP_9.

STEP_7 : Stop synchronization with **SYNCH $00** command.
SetupV.21 ch2 with **CONF $0F $0D $00 $00** command.
Arm the receiver with **SYNCH $01** command.

STEP_8 : Wait until **STA_109** equal 1 and go to STEP_9.

STEP_9 : Receive data on **RxD** Pin.
If **STAT_109** equal 0 go to STEP_10.

STEP_10 : Hang_up.

The flow chart (Figure 18) summarizes the above sequence.

Figure 17

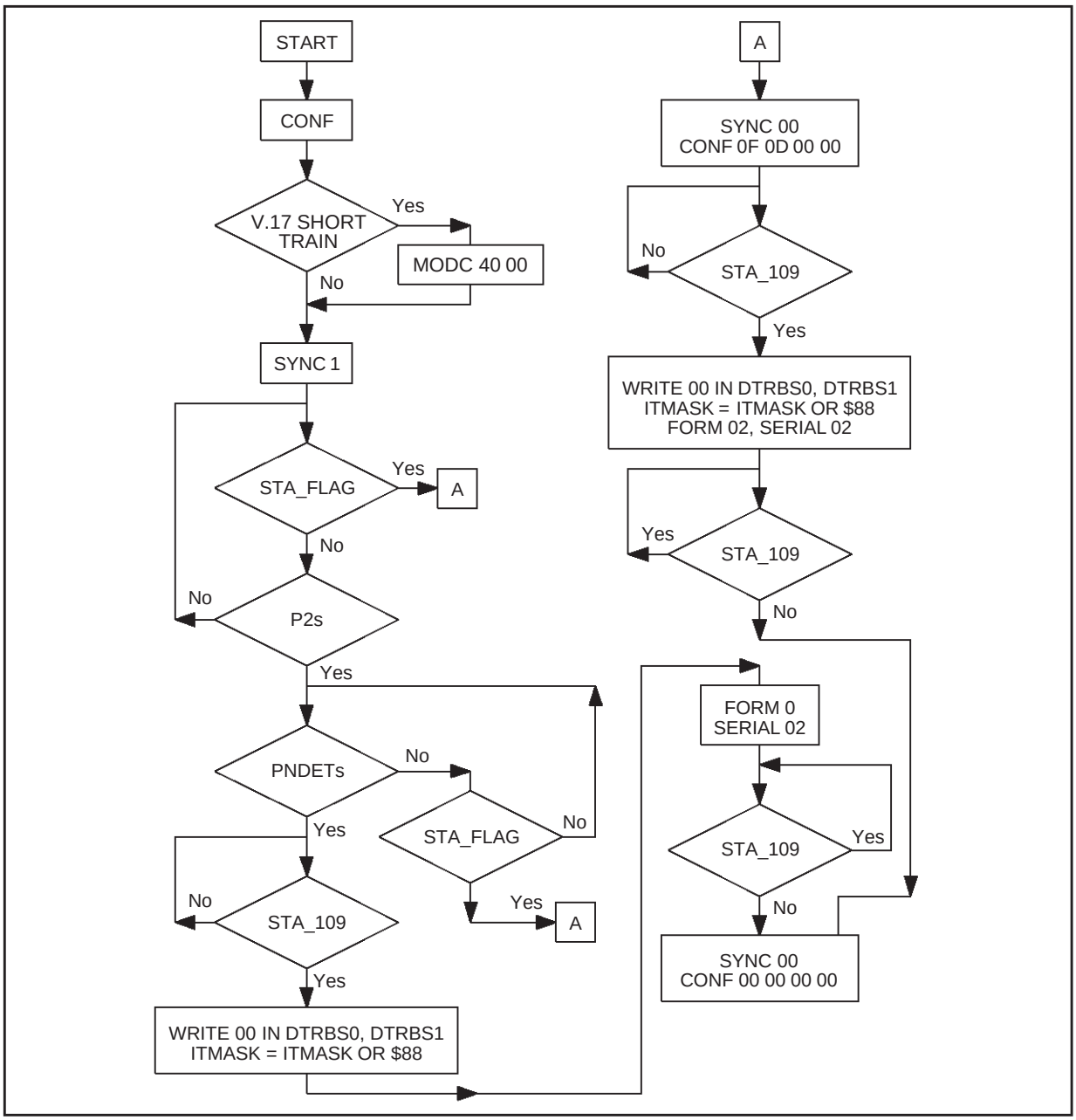
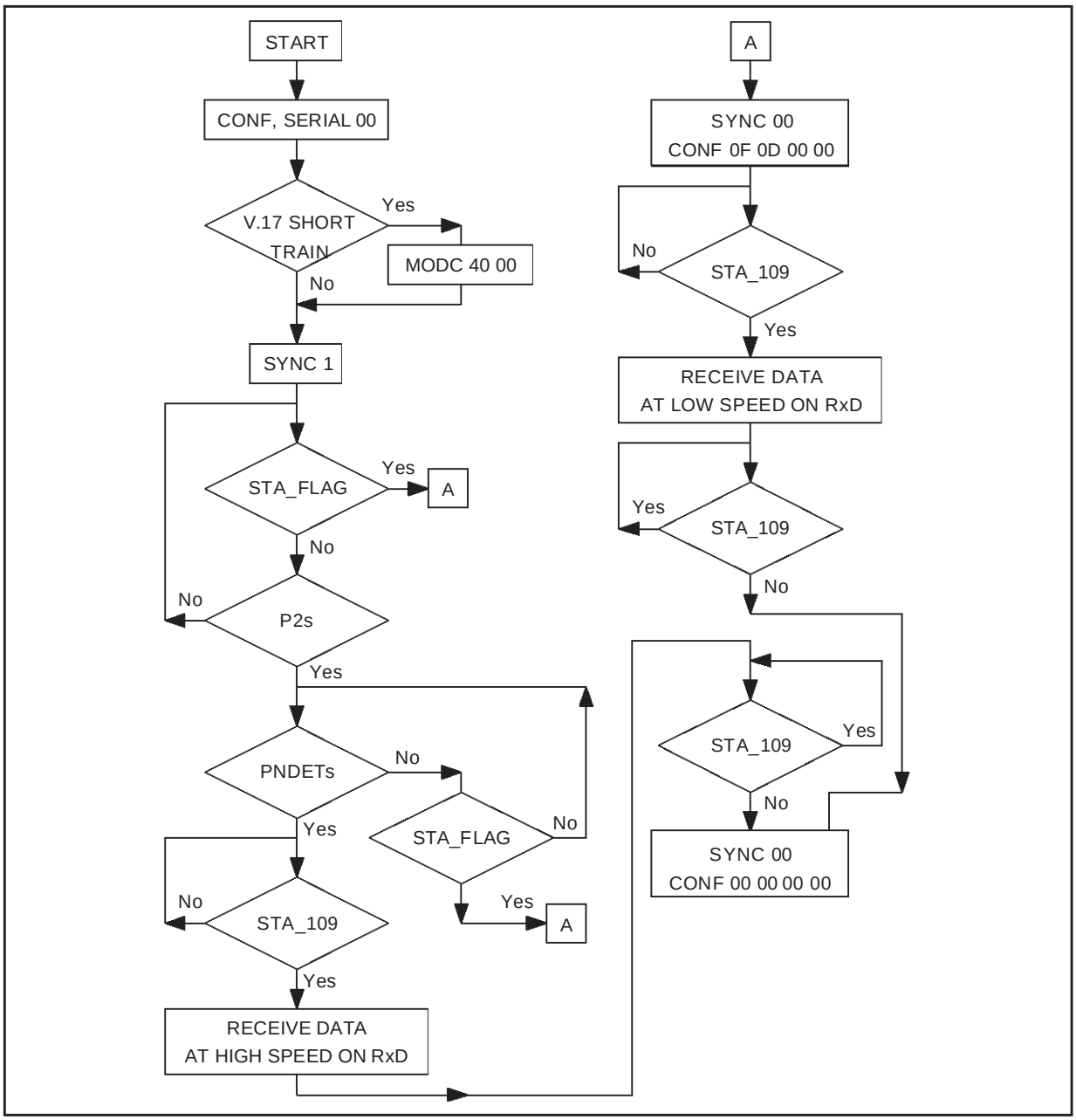

START
CONF
V.17 SHORT TRAIN
Yes
MODC 40 00
No
SYNC 1
STA_FLAG
Yes
A
No
P2s
No
Yes
PNDETs
No
Yes
STA_FLAG
No
Yes
A
No
STA_109
Yes
WRITE 00 IN DTRBS0, DTRBS1
ITMASK = ITMASK OR $88
A
SYNC 00
CONF 0F 0D 00 00
No
STA_109
Yes
WRITE 00 IN DTRBS0, DTRBS1
ITMASK = ITMASK OR $88
FORM 02, SERIAL 02
Yes
STA_109
No
FORM 0
SERIAL 02
STA_109
Yes
No
SYNC 00
CONF 00 00 00 00
75C52-42.EPS

Figure 18



III.3.4 - Reception in Phase D

As in phase B the FAX system will receive data in V.21 ch2 with the HDLC format.

See the example detailed in Chapter III.3.2 for setup the ST75C52/520 to detect and receive preamble, HDLC frame over V.21 ch2.

III.3.5 - Reception in phase E

The FAX system must receive DCN signal (deconnection) in low speed mode.

After that no reception will be done by the FAX system in phase E, so after deconnection we suggest to setup the ST75C52/520 with **CONF $00 $00 $00 $00** command to be able to send and detect tones.

If power management is important we suggest to put the ST75C52/520 in low power mode with the following sequence :
Enable **IT5** interrupt doning ITMASK = ITMASK or $A0.
Send SLEEP command.

IV - DATA EXHANGES

This chapter describes the way to use the ST75C52/520 Data Buffers.

These Data Buffers are implemented into the DUAL RAM of the ST75C52/520. They are shared between the Host processor and the ST75C52/520. A mechanism of Flags and Interrupts is associated with them to allow an easy management of the Data.

The mechanism described below is only valid while in regular Data Transmission, not in Handshaking neither in Call progress (or DTMF) tone detection modes.

"Host" refers to the Micro-controller connected to the ST75C52/520 Data Pump.

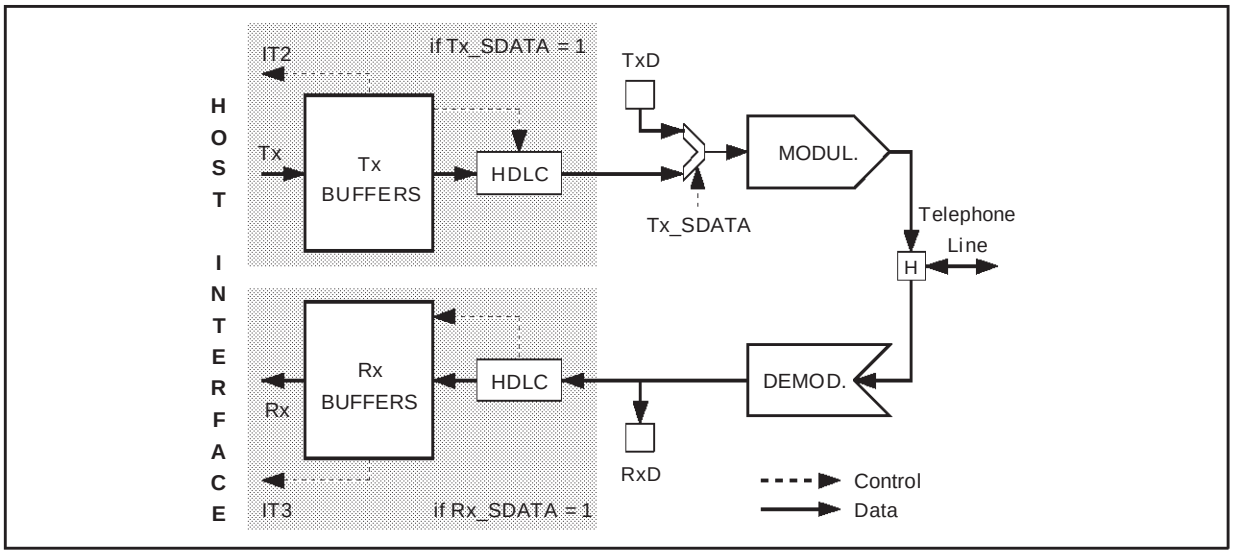
"Transmit Data" (or Tx) means Data transfered by the ST75C52/520, via the modulator, to the telephone line, and "Receive Data" (or Rx) means Data comming from the telephone line and Demodulated by the ST75C52/520.

IV.1 - Overview

While in Parallel mode, the Transmitted (respectively Received) Data to (from) the telephone line are exchanged between the Host and the ST75C52/520.
Two totally independent channels are provived for Transmit and Receive Data. Even while using Half Duplex modes of operation, the transmitted data comes from the Transmit buffers and the receive data arrives in the Receive buffers.

Two independent Interrupts, **IT2** (for Transmit) and **IT3** (for Receive) are available for synchronizing the ST75C52/520 and the Host. An additional **IT0** interrupt will signal the errors in the synchronization mechanism.
The equivalent Data Flow is as follows (see Figure 19).
The ST75C52/520 has a buit-in HDLC capability. This feature automatically performs HDLC framing/deframing, CRC Generation/detection and "0" Insertion/deletion. This Format of Data is selected by the **FORM** Command described bellow.

Figure 19



IV.2 - Select Parallel Mode

IV.2.1 - SERIAL Command

The **SERIAL** command allows the independent selection of the parallel mode for the Transmit and/or Receive Data path. The parameter syntax is as follows (see Table 3).

Table 3

Field	Byte	Pos.	Value	Definition
TX_SDATA	1	0	0 * 1	Use Serial Link for Tx Data Use both Serial and Parallel Link for Tx Data
RX_SDATA	1	1	0 * 1	Use only Serial Link for Rx Data Use both Serial and Parallel Link for Rx Data

Note : Even if the parallel mode is selected for the Receiver, the Received Bit Stream is available on the RxD Pin of the ST75C52/520. This command must be sent in Data Mode, when the Transmit or Receive data links are established. This corresponds with the presence of the signals STA_106 (for Tx) and/or **STA_109** (for Rx).

IV.3 - Transmit Buffers

Two identical buffers are provided to exchange the data between the Host interface and the ST75C52/520. When the host is writing data into a buffer, the ST75C52/520 is transmitting the other one. After that, both the Host and the ST75C52/520 switch to use the other buffer. This mechanism, called "Double-Buffering", ensures that the host has the maximum time to fill one buffer.

The DUAL Ram area associated with the transmit buffers is as follows :

Table 4

Name	Address	Description
DTTBS0	$2E	Buffer 0 Status Byte
DTTBS0 [0]	$2F	Buffer 0 Status Byte 0
DTTBS0 [1]	$30	Buffer 0 Status Byte 1
DTTBS0 [2]	$31	Buffer 0 Status Byte 2
DTTBS0 [3]	$32	Buffer 0 Status Byte 3
DTTBS0 [4]	$33	Buffer 0 Status Byte 4
DTTBS0 [5]	$34	Buffer 0 Status Byte 5
DTTBS0 [6]	$35	Buffer 0 Status Byte 6
DTTBS0 [7]	$36	Buffer 0 Status Byte 7
DTTBS1	$37	Buffer 1 Status Byte
DTTBS1 [0]	$38	Buffer 1 Status Byte 0
DTTBS1 [1]	$39	Buffer 1 Status Byte 1
DTTBS1 [2]	$3A	Buffer 1 Status Byte 2
DTTBS1 [3]	$3B	Buffer 1 Status Byte 3
DTTBS1 [4]	$3C	Buffer 1 Status Byte 4
DTTBS1 [5]	$3D	Buffer 1 Status Byte 5
DTTBS1 [6]	$3E	Buffer 1 Status Byte 6
DTTBS1 [7]	$3F	Buffer 1 Status Byte 7

The Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first in time to be transmited.

According to the Data Format, the Status byte of a buffer has different meanings. However a value of 0 signals to the host that a buffer is empty. This value is set by the ST75C52/520 each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The host must start with the Buffer 0 as soon as the **ST_106** signal is on and the **SERIAL Tx** is selected and BEFORE the **XMIT 1** command is sent.

A mechanism of interruption (IT2 for Transmit) is associated with the Data Buffer management. Each time a Buffer is emptied by the ST75C52/520 it generates an interrupt.

IV.4 - Receive Buffers

Symetrically two identical buffers are provided to exchange receive data between the ST75C52/520 and the Host processor. While the ST75C52/520 is filling one of the buffers with the receive bits, the Host processor is reading the other buffer. As soon as the host has emptied a buffer it frees it by writing 0 in the buffer status byte.

The DUAL Ram area associated with the receive buffers is as follows :

Table 5

Name	Address	Description
DTRBS0	$1C	Buffer 0 Status Byte
DTRBS0 [0]	$1D	Buffer 0 Status Byte 0
DTRBS0 [1]	$1E	Buffer 0 Status Byte 1
DTRBS0 [2]	$1F	Buffer 0 Status Byte 2
DTRBS0 [3]	$20	Buffer 0 Status Byte 3
DTRBS0 [4]	$21	Buffer 0 Status Byte 4
DTRBS0 [5]	$22	Buffer 0 Status Byte 5
DTRBS0 [6]	$23	Buffer 0 Status Byte 6
DTRBS0 [7]	$24	Buffer 0 Status Byte 7
DTRBS1	$25	Buffer 1 Status Byte
DTRBS1 [0]	$26	Buffer 1 Status Byte 0
DTRBS1 [1]	$27	Buffer 1 Status Byte 1
DTRBS1 [2]	$28	Buffer 1 Status Byte 2
DTRBS1 [3]	$29	Buffer 1 Status Byte 3
DTRBS1 [4]	$2A	Buffer 1 Status Byte 4
DTRBS1 [5]	$2B	Buffer 1 Status Byte 5
DTRBS1 [6]	$2C	Buffer 1 Status Byte 6
DTRBS1 [7]	$2D	Buffer 1 Status Byte 7

The Bit 0 (LSB) of the Buffer 0 Data Byte 0 is the first received bit in time (the oldest).

According to the Data Format, the Status byte of a buffer has different meaning. However a value of 0 signals to the ST75C52/520 that a buffer is empty. This value is set by the Host each time it has emptied the buffer. After having used one buffer, the host must select the other buffer for the next operation. The Host must start with the Buffer 0 as soon as the **STA_109** signal is on and the **SERIAL Rx** is selected.

A mechanism of interruption (**IT3** for Receive) is associated with the Data Buffer management. Each time a buffer is filled by the ST75C52/520 it generates an interrupt.

IV.5 - Interruption

Two Interrupt signals are provided in order to synchronize the Data Buffer Exchanges. **IT2** is associated with the Transmit Buffer mechanism and **IT3** with the Receive Buffer mechanism.

In order to enable these interrupts, the Host processor must set the bit 2 (for **IT2**) and the bit 3 (for **IT3**) of the **ITMASK** Register to 1. It must also set the Bit 7 of the **ITMASK** register to 1 in order to globally enable all the selected sources of interruption.

When an Interrupt occurs (low level on **SINTR** Pin) the user must read the **ITSRCR** Register to determine the source of the interrupt, either **IT2** for Tx (if the bit 2 is 1) or **IT3** for Rx (if the bit 3 is 1).

Once the Interrupt has been serviced, the host must acknowledge it by writing a $00 value into the register **ITRES2** for **IT2**, or **ITRES3** for **IT3**.

These registers have the following address (see Table 6).

Table 6

Name	Address	Type	Description
ITRES2	$42	Write only	Clear IT2
ITRES3	$43	Write only	Clear IT3
ITMASK	$4F	Read/Write	Interrupt Mask
ITSRCR	$50	Read Only	Interrupt Source

Notes : 1. The ST75C52/520 does not check that the interrupt has been acknowledged.

2. Even if the Host does not use the interruption, the ST75C52/520 will set the bit 2 (for **IT2**) and/or bit 3 (for **IT3**) of the **ITSRCR**.

3. The ST75C52/520 uses only the Data Buffer Status Bytes to detect Overrun or Underrun Error. These errors are reported into the **SYSERR** byte, and could generate an interrupt **IT0**.

The equivalent schematic is : see Figure 20.

The interrupt mechanism assumes that the Host processor uses a Level sensitive interrupt (active low). The flow chart of the Host interrupt service routine looks generaly like this (see Figure 21).

Figure 20

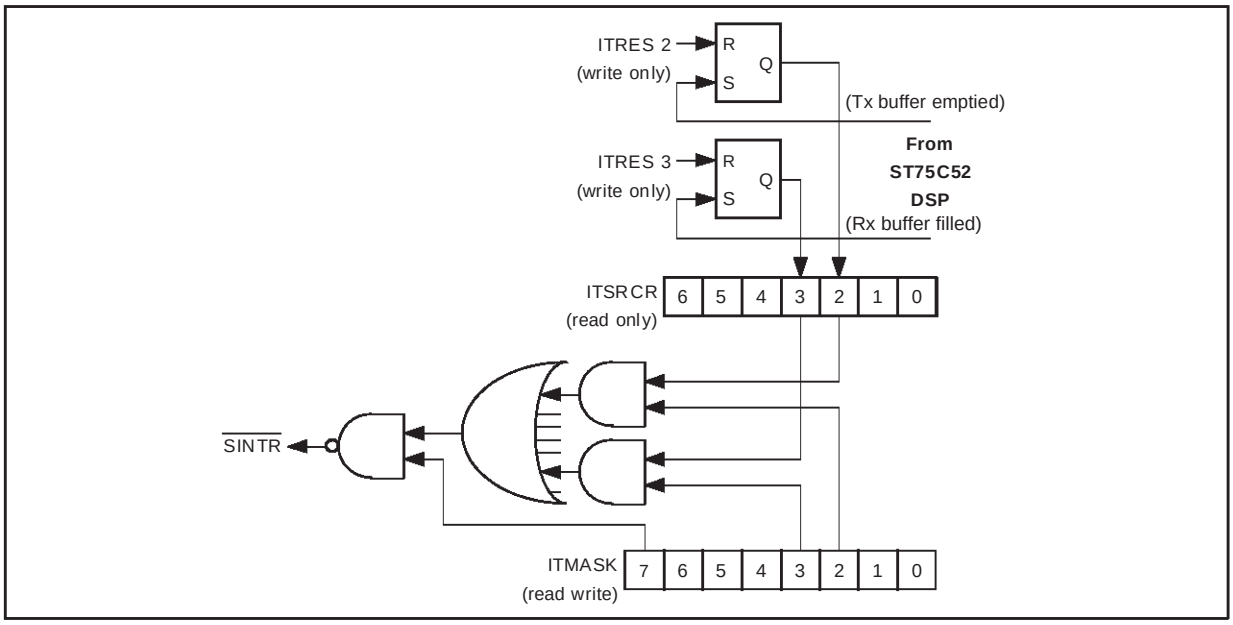
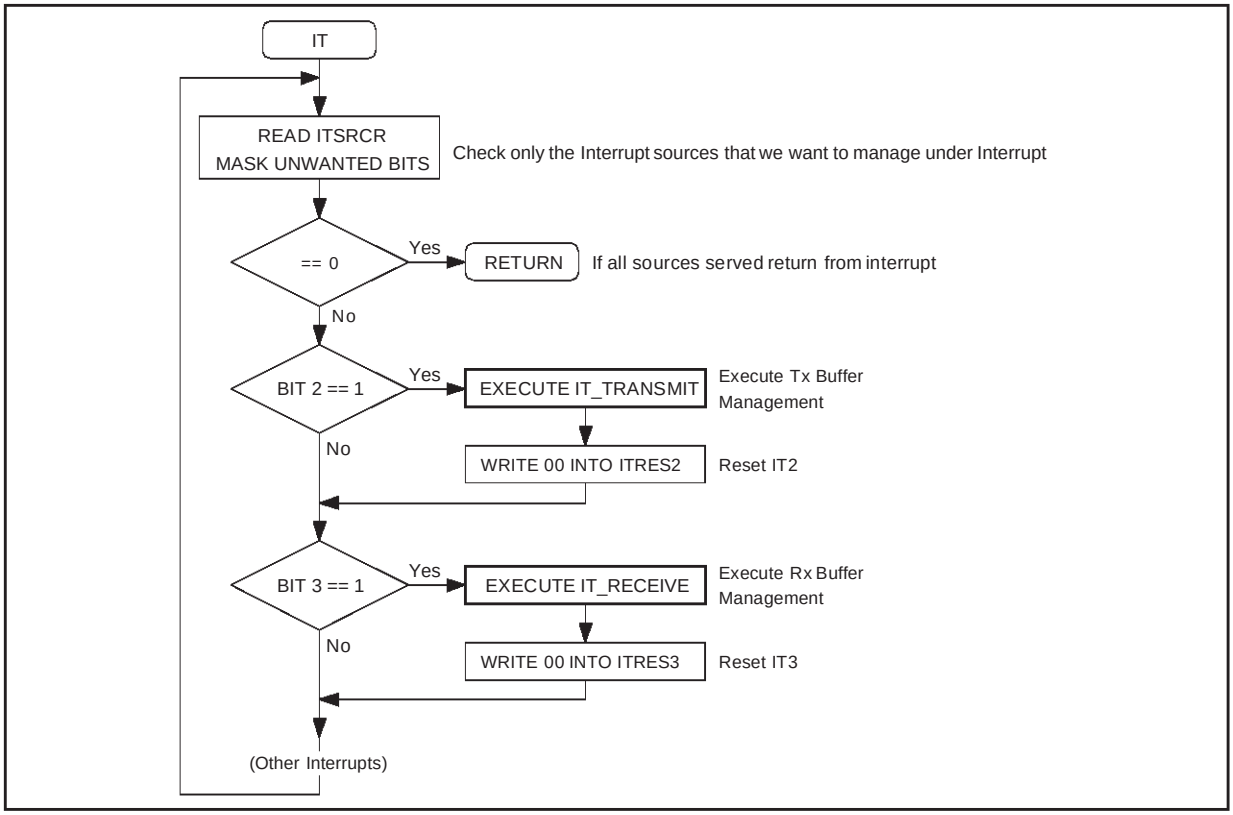


Figure 21



IV.6 - Data Format

Different Formats of Data can be Transmitted/Received to/from the Telephone Line. These Formats can be selected when entering the Data Mode by using the **FORM** command.
The Format of the Data can be changed, on the fly in the Data Mode during the same communication, by sending a different **FORM** command at any time. Note that for Full Duplex operation the Data Format is the same for the transmitter and the receiver.

IV.6.1 - FORM Command

The **FORM** command allows the selection of the Data Format. The Parameter syntax is as follows :

Table 7

Field	Byte	Pos.	Value	Tx	Rx	Definition
X_SYNC	1	1..0	00*	X	X	Synchronous format
			01	X		Continuous "1" (Tx only)
			10	X	X	HDLC framing /deframing
			11	X		Continuous "0" (Tx only)

IV.6.2 - Synchronous Mode

The synchronous mode is the default mode, if no **FORM** command is used.

The transmitter reads the bits in the DUAL Ram Buffer **DTTBFx** (starting with the Bit 0 of Byte 0 of Buffer 0) and send them over the Telephone line. The Buffer Status Byte **DTTBSx** contains the number of Data Bytes to transmit.

The Receiver write the received bits comming from the Telephone line and write them into the DUAL Ram Buffer **DTRBFx** (starting with the Bit 0 of the Byte 0 of the Buffer 0). The Buffer Status Byte **DTRBSx** contains the number of Data Bytes received (generaly 8).

The time between each **IT2** interrupts (or **IT3**) is equal to 64-bit if the number of Data Bytes is set to 8. The Host has the full 64 bits time to serve the interrupt.

Table 8

Bit Rate (bps)	Interrupt Time (ms)
14400	4.4
12000	5.3
9600	6.6
7200	8.8
4800	13.3
2400	26.6
1200	53.3
300	213.3
75	853.3

IV.6.3 - HDLC Mode

The HDLC Format can be used for T.30 or ECM implementations

IV.6.3.1 - HDLC Transmit

The HDLC Transmitter performs the following tasks :
- flag generation (7E) while in inter-frame,
- flag generation (7E) at the beginning of a frame,
- zero insertion (after 5 consecutive "1"),
- CRC16 computation,
- CRC16 transmission at the end of a frame,
- flag generation (7E) at the end of a frame,
- abort frame.

The Buffer Status Byte **DTTBSx** defines the frame type, and the number of Data Bytes to transmit.

IV.6.3.2 - HDLC Receive

The HDLC Receiver performs the following tasks :
- flag recognition,
- opening flag recognition,
- zero deletion,
- CRC16 computation,
- CRC16 check; error CRC16 detection,
- closing flag recognition,
- abort frame detection.

The Buffer Status Byte **DTRBSx** contains the frame type, the number of Data Bytes and the error report if any.

The errors detected are :
- CRC16 Error : Wrong CRC received,
- non byte-alligned frame : The number of Data bits between the beginning of the frame and the end of the frame (after "zero" deletion) is not a byte-multiple,
- aborted frame : More that 6 consecutive "1" received.

IV.7 - Transmitting in Parallel Mode

IV.7.1 - Description

When the **STA_106** (CTS) signal is on, the user must select the parallel mode by enabling the parallel link with **TX_SDATA** bit set in **SERIAL** command. After that the ST75C52/520 will start transmitting continuous "1". Note that for a proper operation each time the **STA_106** signal goes on, the **SERIAL** command must be sent.

IV.7.1.1 - XMIT Command

The **XMIT** Command works like a CTS signal for the Parallel process.

When **XMIT** is off, the ST75C52/520 transmits continuous "1". When on the ST75C52/520 transmits Data in accordance with the **FORM** command and starts to manage the Data Buffer.

This command can be sent at any time, while in Data Mode (see Table 9).

IV.7.1.2 - FORM Command

The **FORM** Command can be sent at any time to redefine the current format. The effect will take place only when **XMIT** is on.

Here is a formal example showing the relationship between **SERIAL**, **XMIT**, and **FORM** Commands : see Figure 22.

IV.7.1.3 - STOP Command

The **STOP** command is used, at the end of the transmission, to stop sending the carrier on the telephone line. According to the Parallel/Serial mode (defined with the **SERIAL** command) and the Format (defined with the **FORM** command) the effect of this command is as in Table 10.

Prior to the **STOP** command the user must have stop the parallel transmission with a **XMIT off** command.

Table 9

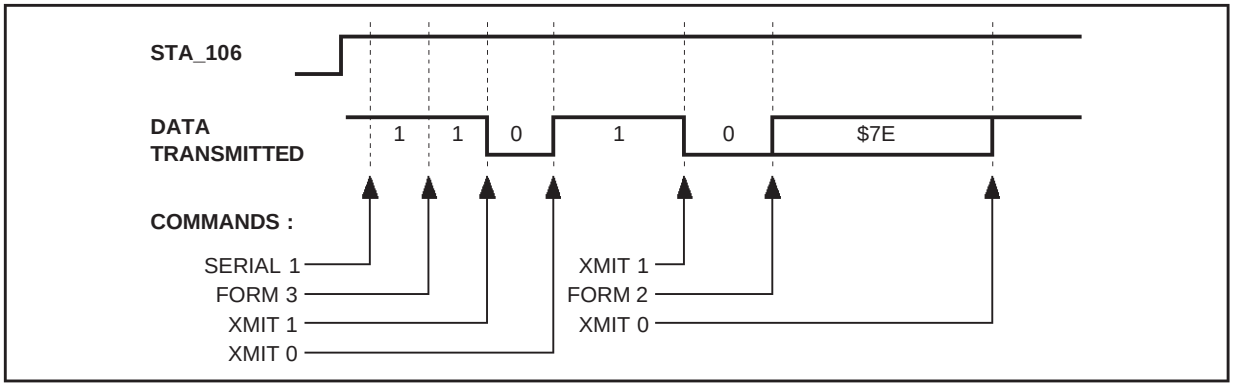
Field	Byte	Pos.	Value	Definition
TX_START	1	0	0 * 1	(Off) Send continuous "1" (1). (On) Send Data according with the Format defined in the **FORM** command.

Note 1 : The XMIT Off command takes effect only when the two Transmit buffers are empty : **DTTBF0** and **DTTBF1** equal to $00.

Table 10

Mode	TX-SDATA	Observed actions
Serial	0	Immediate
Parallel	1	When the current data buffer will be totaly transmitted, and that no more buffers will be available, that is to said both **DTTBF0** and **DTTBF1** will be $00 (equivalent to an Underrun condition).

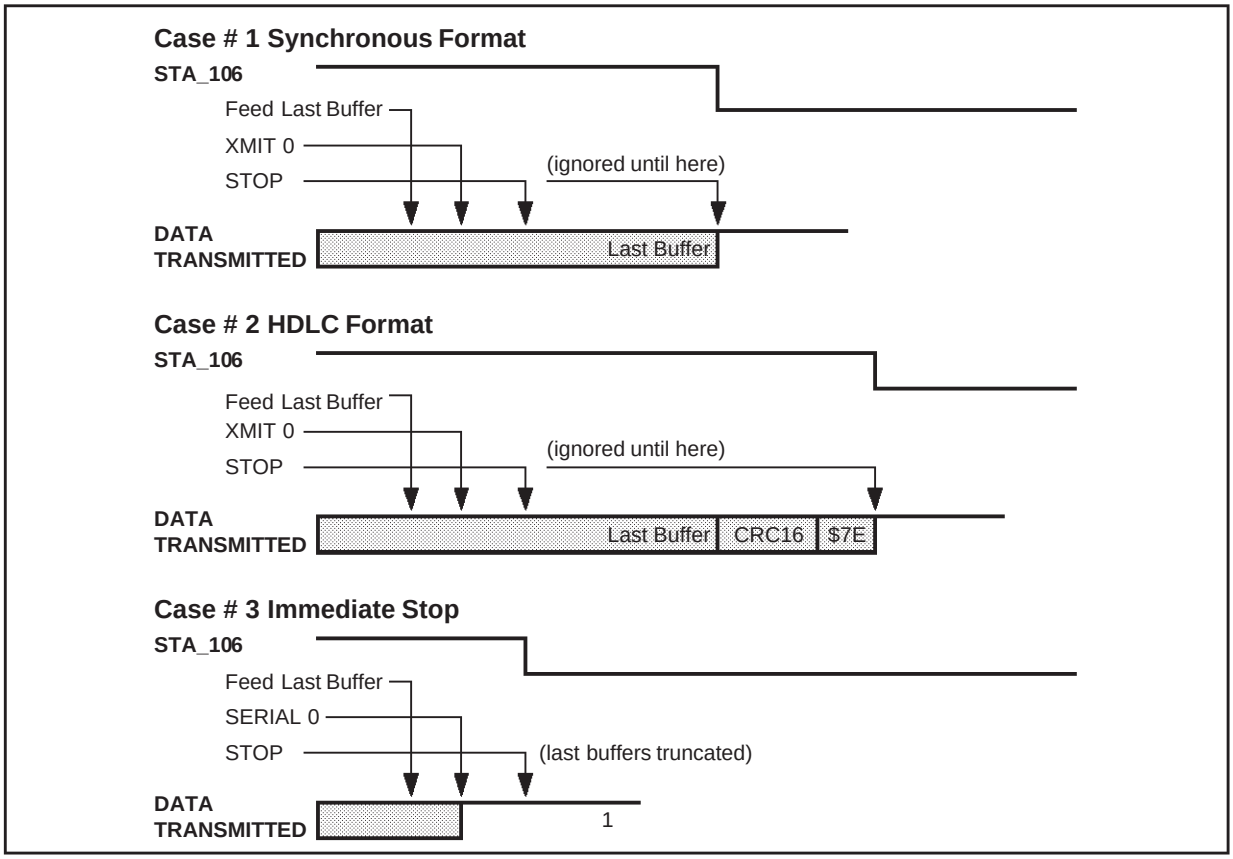
Figure 22



IV.7.1.4 - Timing

Here are regular sequences to stop properly the transmission : see Figure 23.

Figure 23



IV.7.1.5 - FSK Full Duplex Mode

In FSK Full duplex Mode the parallel mode assumes that the Bit time duration is the nominal Bit rate. Each bit element from the Transmit buffer is maintained during the full bit time. The Nominal bit clock is defined as follows :

Table 11

FSK Standard	Nominal Transmit Bit Rate (Hz) (1)	Bit Clock on CLK Pin (Hz)
V.21	300	9600
Bell 103	300	9600
V.23 Originate	75	9600
V.23 Answer	1200	9600

Note 1 : The accuracy of the Bit clock is given by the ST75C52/520 oscillator, and must better than 50ppm.

IV.7.2 - Modem Flow Chart

When in the Parrallel Data Mode, each time the ST75C52/520 need a bit to transmit it executes the following routine (see Figure 24).

Where **x** starts with the value 0 and toggle thereafter between 1 and 0.

IV.7.3 - Host Flow Chart

Here after are Flowcharts to :

- establish a V.29 transmission
- send Synchronous continuous "$AA, $55, $AA, $55..." sequence.
  The management of the Buffers are done under Interrupt.
- stop properly the transmission.

Establish a V.29 transmission and send the very first Buffer (see Figure 25).

Figure 24

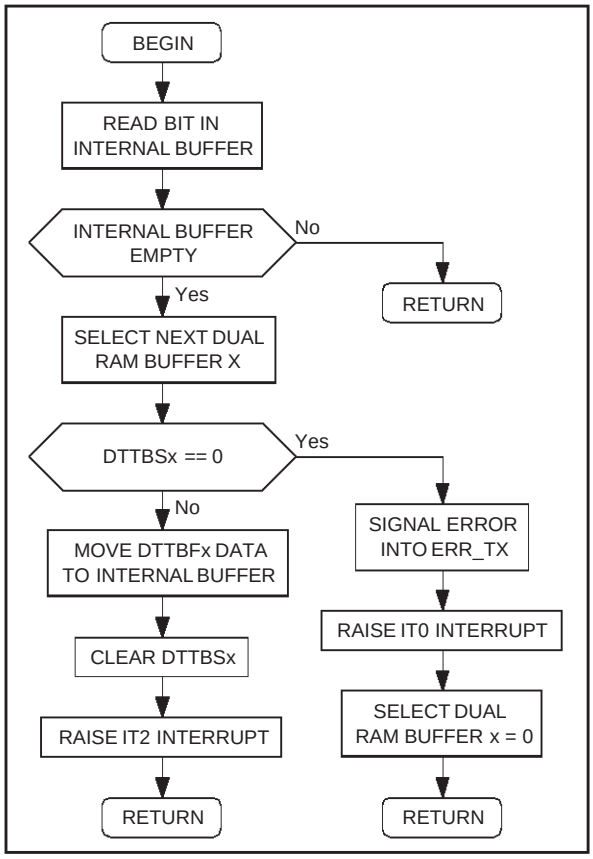
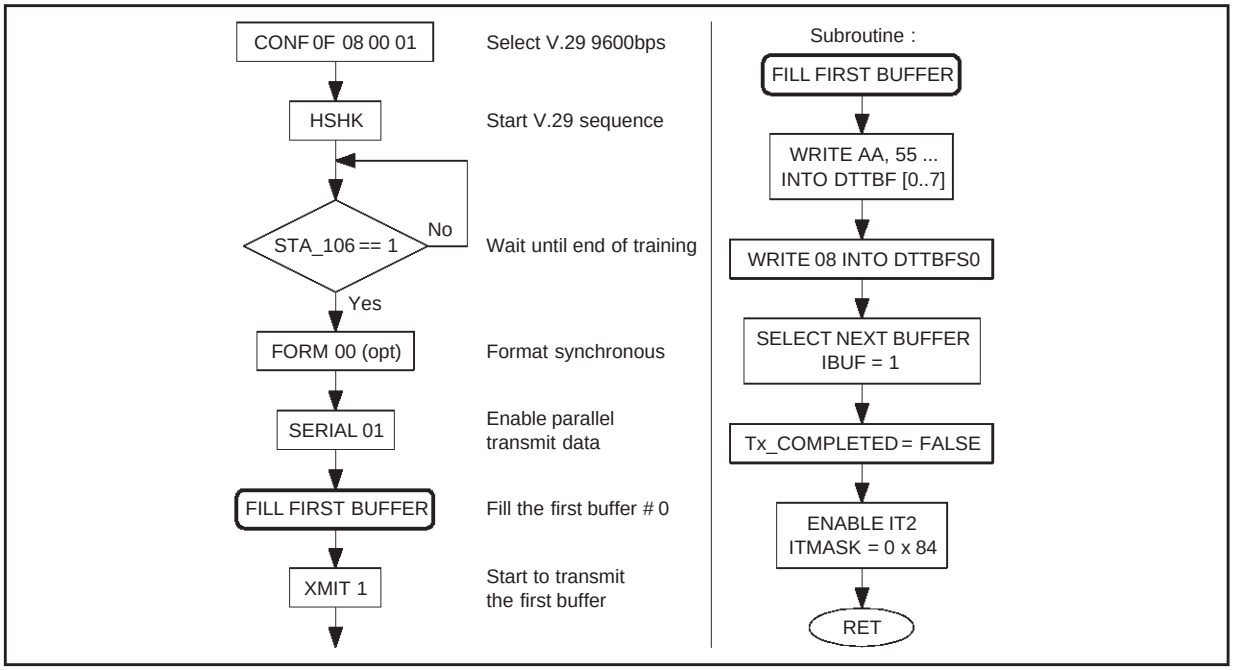


Figure 25

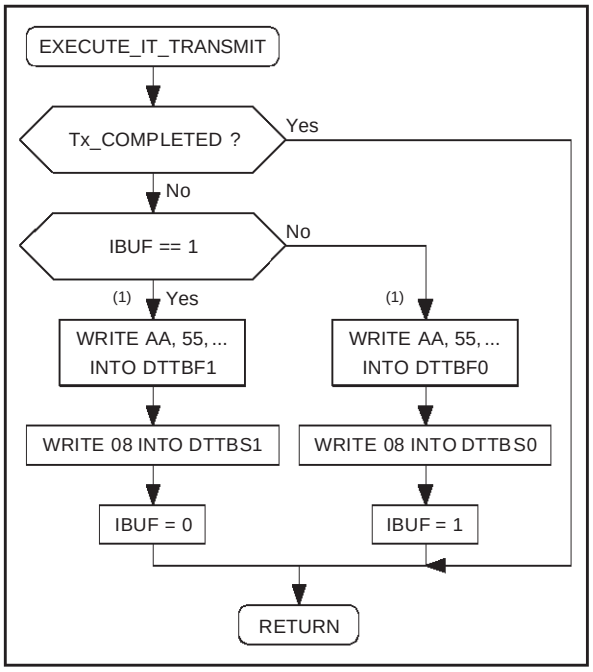


These flowcharts show two CPU variables labeled IBUF and Tx_Completed, they are necessary for the understanding of the mechanism, but there is different manners to implement it. These two variables have the following meanning :

- IBUF: This is the number of the DUAL Ram Buffer currently in use by the Host processor. It starts with 0 and then alternate 1, 0, 1, 0...
- Tx_Completed: This is a Flag to dialog with the interrupt process in order to stop properly the transmission.

The other Buffers are sent under interrupt control (refer to the interrupt flow chart, Figure 26).

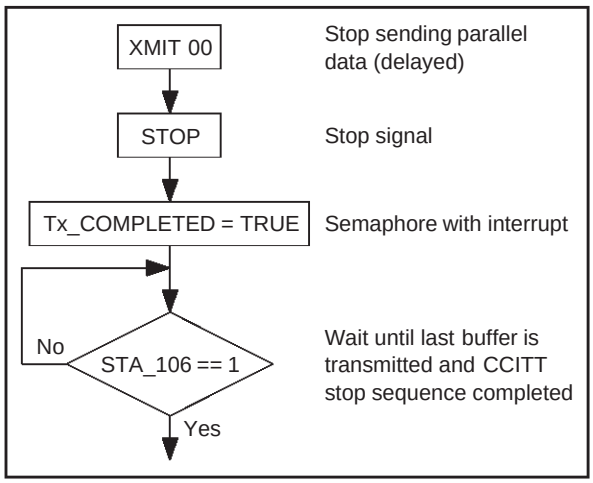
Figure 26



Note : (1) At this step the host can check that the corresponding **DTTBSx** buffer is empty (equal to $00), otherwise it is an error.

To stop properly the transmission, without loss of Data (see Figure 27).

Figure 27



IV.7.4 - Error Detection

Error occurs when the ST75C52/520 need some bits from the transmit buffer DTTBSx and this buffer is empty. This condition is called "Underflow".
This error is signaled in the bit **ERR_TX** of the **SYSERR** byte, and generates an interrupt IT0. To clear the error a **CSE 01** command must be issued.

An Underflow condition occurs when :

- in synchronous mode : the host processor "forgets" to feed the current **DTTBSx** buffer,
- in HDLC mode : when, while inside a frame, the host processor "forgets" to feed the current **DTTBSx** buffer. An abort frame is transmitted in place of the regular Buffer.

When an underflow condition occur the host must restart the whole parallel initialization, as explained above.

IV.7.5 - Synchronous Mode

IV.7.5.1 - Description

In synchronous mode the ST75C52/520 transmits the bits contained in the DUAL Ram Buffer without any modification. It starts with the Bit 0 of the **DTTBF0[0]** byte.

IV.7.5.2 - Status Word Format

The Transmit Status Bytes **DTTBS0** or **DTTBS1** have the same following meaning :

Table 12

DTTBSx in Synchronous Mode			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 Other	Buffer empty. 1 Byte to transmit (**DTTBFx[0]**). 2 Bytes to transmit (**DTTBFx[0]** and **DTTBFx[1]**). .. 8 Bytes to transmit (**DTTBFx[0 .. 7]**). Not allowed.
Other	7 .. 4	0	Reserved, must be 0.

This status byte must be written by the Host, after filling the corresponding data buffer **DTTBFx[0..7]** with the right number of data bytes to transmit.
This status byte is cleared by the ST75C52/520, just before generating the **IT2** interrupt.

IV.7.6 - HDLC Mode

IV.7.6.1 - Description

In HDLC mode the ST75C52/520 transmits the data bytes contained into the DUAL Ram buffer packed inside an HDLC frame. The mechanism is as follows :

- while the Host has no frame to transmit, that is: as long as **DTTBSx** equals $00, the ST75C52/520 transmits the HDLC Flag $7E.
- when the Host wants to send some data, it feeds the buffer with some data bytes to transmit (between 1 and 8) and set the **BUFF_SFRM** bit in the **DTTBSx** status buffer. At that time the ST75C52/520 start sending data contained in the Buffer, computing the CRC and performing "zero insertion" if needed.
- when the host wants to send additional data (within the same frame) it feeds the buffers just like in synchronous mode. If an Underflow condition occurs, the ST75C52/520 will abort the frame by sending 8 consecutive "1", and the Host must restart the whole parallel initialization.
- when the host wants to close a frame, it set the **BUFF_EFRM** bit in the **DTTBSx** status buffer. At that time the ST75C52/520 will send the contents of the buffer, then send the CRC and an HDLC closing flag $7E.
- if the Host, wants to abort a frame (while sending a frame) it set the **BUFF_FRAB** bit in the **DTTBSx** status buffer. At that time, as soon as the last buffer will be transmitted, the ST75C52/520 will send 8 consecutive "1" and wait for the next buffer.

IV.7.6.2 - Status Word Format

Table 13

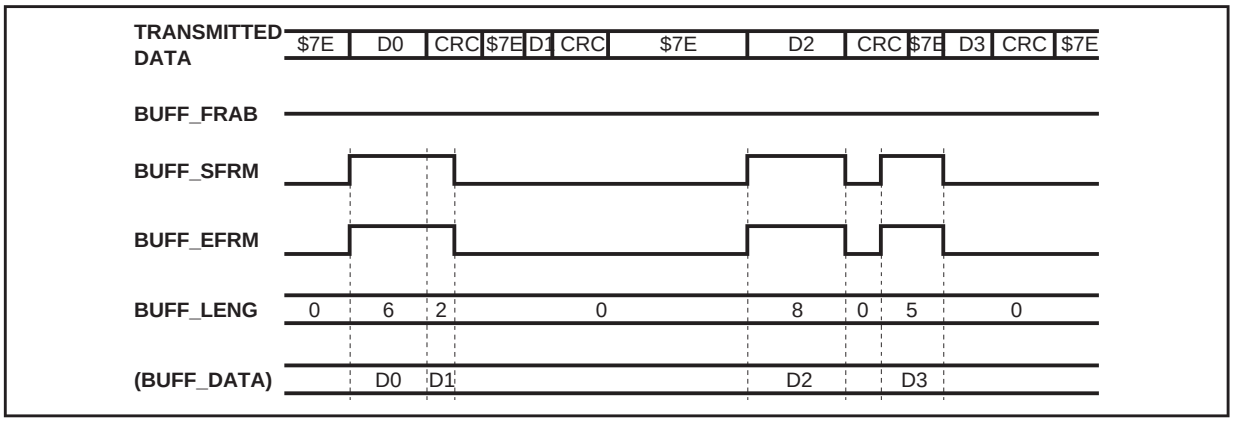
DTTBSx **in HDLC Mode**			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 other	Buffer emty. 1 Byte to transmit (**DTTBFx[0]**). 2 Bytes to transmit (**DTTBFx[0]** and **DTTBFx[1]**). .. 8 Bytes to transmit (**DTTBFx[0 .. 7]**). Not allowed.
BUFF_SFRM	4	0 1	Data stream. Start of frame : the buffer is a beginning of frame.
BUFF_EFRM	5	0 1	Data stream. End of frame : the buffer will be followed by the transmission of the CRC and closing flag.
BUFF_FRAB	6	0 1	Data stream. Abort frame : 8 consecutive "1" will be transmitted (whatever **BUFF_LENG** is).
Other	7	0	Reserved, must be 0.

Notes : 1. A buffer can have **BUFF_SFRM** and **BUFF_EFRM** set in the same **DTTBSx** byte, this means that the frame transmitted is short (between 1 and 8 Bytes long).

2. An ending frame (with **BUFF_EFRM** set) must have at least ONE byte of data to transmit.

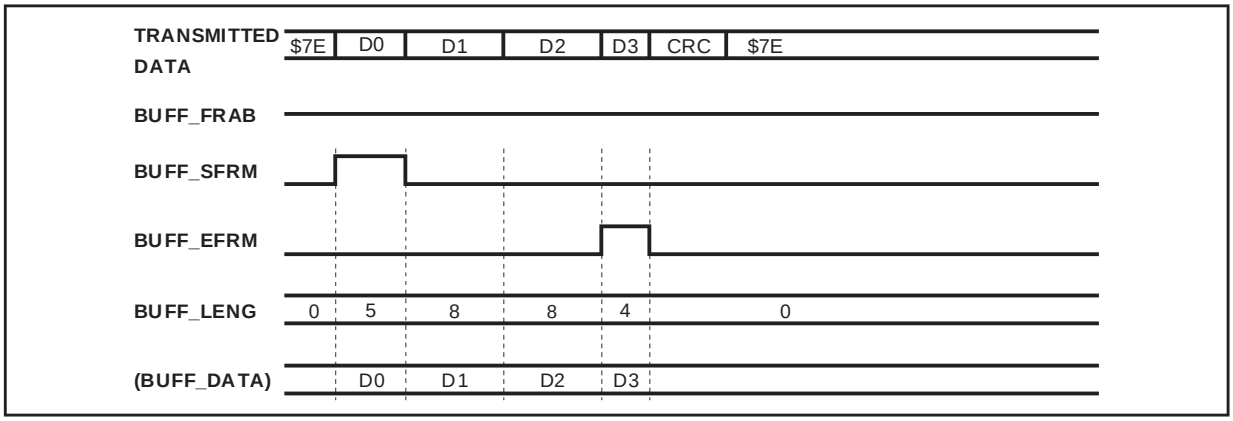
IV.7.6.3 - Single Short Frame

Figure 28



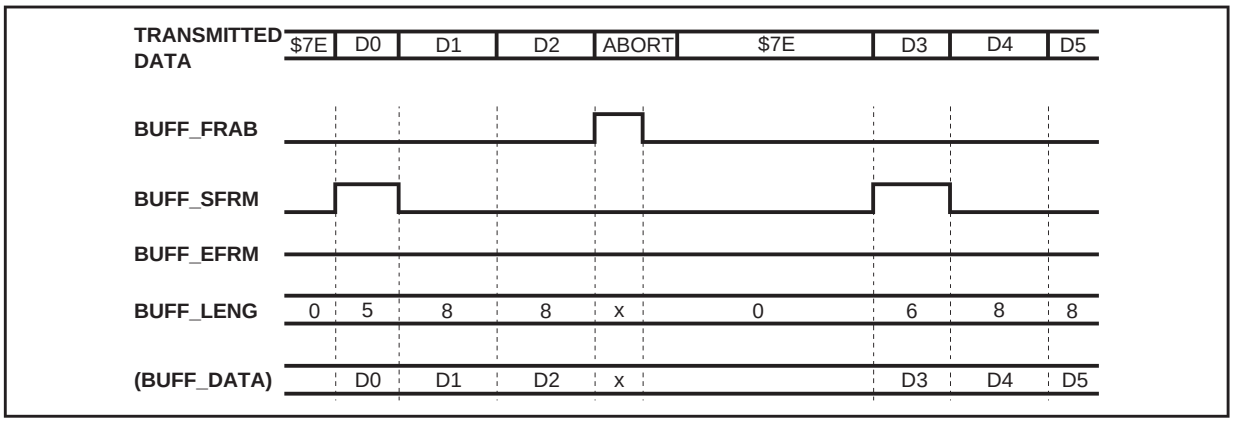
IV.7.6.4 - Long Frame

Figure 29



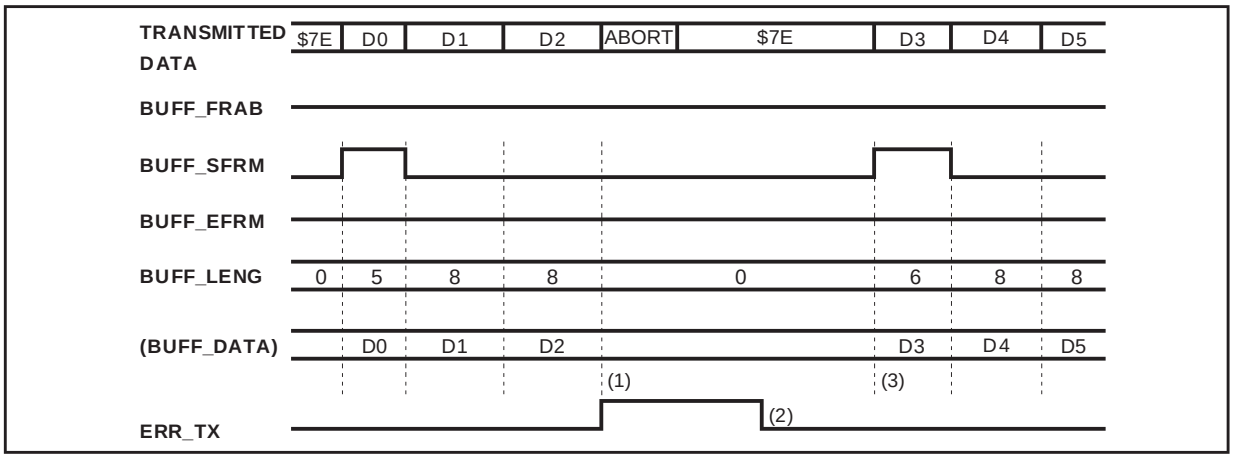
IV.7.6.5 - Abort Frame

Figure 30



IV.7.6.6 - Abort due to Underflow

Figure 31



Where : 1. The Underflow condition appears when the ST75C52/520 needs, inside a frame, some bytes to transmit and that the corresponding buffer is empty.

2. The **ERR_TX** bit is cleared with a **CSE 01** Command.

3. After an Underflow condition restart the initialization of the parallel mode and use the buffer number 0.

IV.8 - Receiving In Parallel Mode

IV.8.1 - Description

When the **STA_109** (CD) signal goes on, the user must select the parallel mode by enabling the parallel link with **RX_SDATA** set in the **SERIAL RX** command. After that the ST75C52/520 will write received data into the DUAL Ram Buffer **DTRBS0**. Note that for a proper operation, each time the **STA_109** goes on the **SERIAL** command must be send.

IV.8.1.1 - Initialization

The host processor must enable the **IT3** receive interrupt first.
Then it must empty the two **DTRBS0** and **DTRBS1** registers by writting $00 at these locations.
Then it must send the **SERIAL RX** command.

As soon as the first **IT3** interrupt appears, the host must proceed with the **DTRBS0** buffer.

IV.8.1.2 - Loss of Carrier

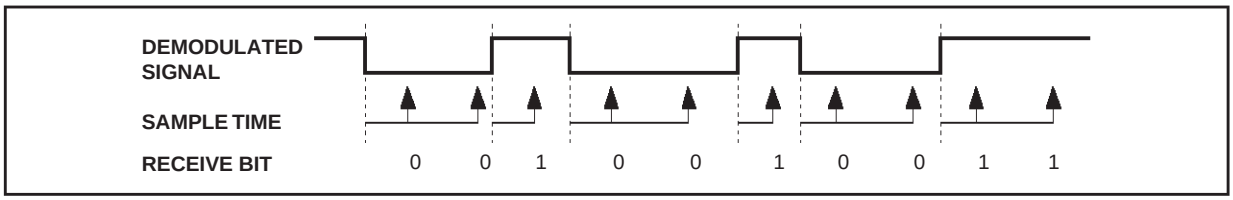
Each time a loss of carrier appears the ST75C52/520 stops updating the Data buffer.

If the carrier reappers the host must proceed again with the initialisation sequence.

IV.8.1.3 - FSK Synchronization

The FSK Full Duplex demodulator uses an algorithm based on the transitions of the received signal. The synchronization mechanism is adjusted with each signal transition in order to sample the demodulated signal at the midle of the bit (see Figure 32).

Figure 32



IV.8.2 - Modem Flow Chart

When in parallel data mode, each time the ST75C52/520 has received some bit of data it executes the following routine (see Figure 33).

Where **X** start with the value 0 and toggle between 1 and 0.

IV.8.3 - Host Flow Chart

Hereafter are flowcharts to :
- establish a V.29 reception,
- receive synchronous data. This task is performed under interrupt,
- handle properly some temporary loss of carrier.

Establish the reception (see Figure 34).

These flowcharts show one CPU variable labeled IBUF which is necessary for the understanding of the mechanism, but there are different manners to implement it.

- IBUF : this is the number of the DUAL Ram Buffer currently in use by the Host processor. It starts with 0 an then alternates 1, 0, 1, 0 ...

The received bits are read by an interrupt routine (see Figure 35).

Figure 33

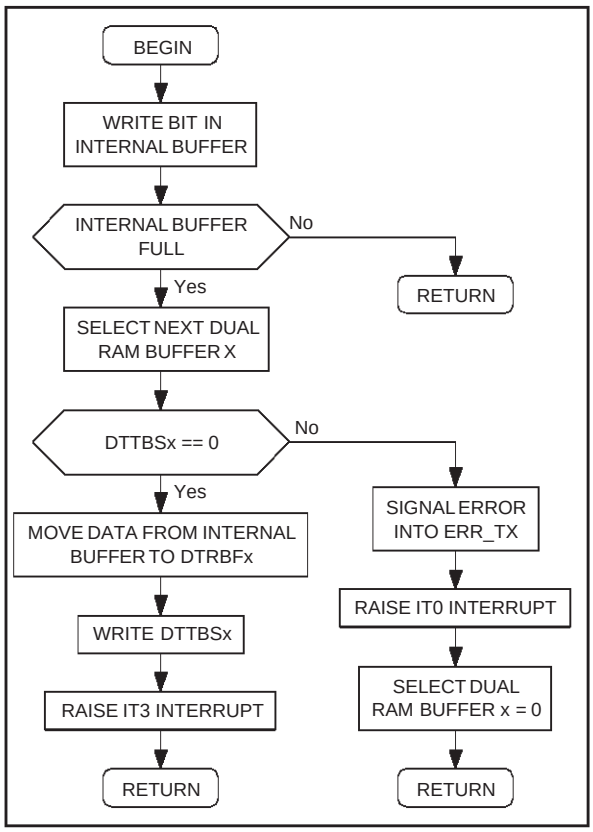


Figure 34

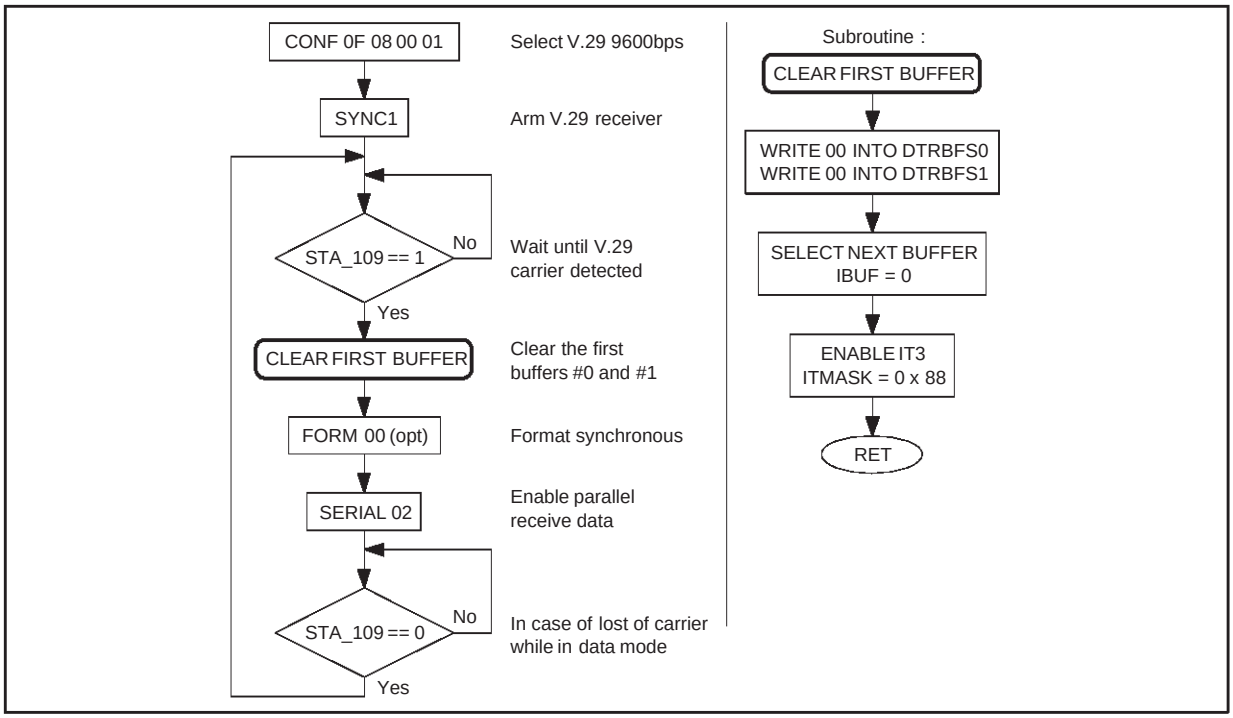
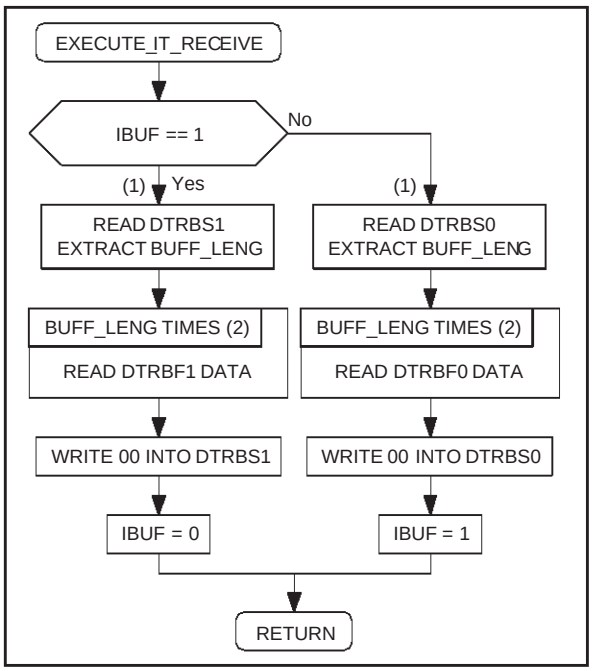


Figure 35



Notes : 1. At that step the host can check that the corresponding **DTRBSx** buffer is full (different from $00), otherwise it is an error.

2. This means read **BUFF_LENG** bytes, inside the Receive buffer **DTRBFx** starting from location **DTRBFx[0]** to **DTRBFx[BUFF_LENG - 1]**. In synchronous mode, the **BUFF_LENG** is always 8 bytes, except when a **STA_109** lost appears in the middle of the buffer.

IV.8.4 - Error Detection

Error occurs when the ST75C52/520 has received some bits and that the buffer **DTRBSx** is not empty, this condition is called "Overflow".

This error is signaled in the bit **ERR_RX** of the **SYSERR** byte, and generates an interrupt IT0. To clear the error a **CSE 02** command must be issued.

An Overflow condition occurs when :

- in synchronous mode: the host processor "forgets" to empty the current **DTRBSx** buffer,
- in HDLC mode: when, while inside a frame, the host processors "forgets" to empty the current **DTRBSx** buffer.

When an Overflow condition occurs the host must restart the whole parallel initialisation.

IV.8.5 - Synchronous Mode
IV.8.5.1 - Description

In synchronous mode the ST75C52/520 writes the received bit into the DUAL Ram Buffer without any modification. It starts with the Bit 0 of the **DTRBF0[0]** byte.

IV.8.5.2 - Status Word Format

The receive Status Byte **DTRBS0** or **DTRBS1** have the same following meaning (see Table 14).

Table 14

DTRBSx **in Synchronous Mode**			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 Other	Buffer emty. 1 Byte received (**DTRBFx[0]**). 2 Bytes received (**DTRBFx[0]** and **DTRBFx[1]**). .. 8 Bytes received (**DTRBFx[0 .. 7]**). Not used.
Other	7 .. 4	0	Not used.

The BUFF_LENG is always 8 except when a lost of carrier (**STA_109** going to 0) happens.
This status byte is set by the ST75C52/520, just before generating the **IT3** interrupt.

IV.8.6 - HDLC Mode

IV.8.6.1 - Description

In HDLC mode the ST75C52/520 extracts from the received HDLC frame the Data information only. It reports, trough the DUAL Ram Buffer, only data information and frame validity. The mechanism is as follows :

- as long as the ST75C52/520 receives continuous HDLC Flag $7E, nothing happens. Note that the ST75C52/520 allows zero sharing between adjacent flags.
- when the ST75C52/520 receives some data, it removes inserted "zero" if needed, and starts to compute the CRC. As soon as its internal buffer is full, the ST75C52/520 writes the received data into the **DTRBFx** buffer and sets the **BUFF_SFRM** inside the **DTRBSx** status byte.
- when receiving additional data, the ST75C52/520 feeds the buffer just like in synchronous mode.
- when the ST75C52/520 receives a closing flag (which can be shared with the following opening flag) it compares the received CRC with its internal computation. It writes the contents of the received last data into the **DTRBFx** buffer, sets the **BUFF_EFRM** bit and reports any frame error in the **DTRBSx** register via the **BUFF_ERRS** bits. Reported errors are :
  CRC error (lowest priority) : the received CRC is not equal to the computed CRC. Some bits, inside the frame, are erroneous.
  Non Byte-Aligned frame (middle priority) : the received data bit count (after deletion of the "zero inserted"), between the opening and the closing flag, is not a multiple of 8.
  Aborted frame (highest priority) : the frame was aborted with at least 7 consecutive "1"
- an abort frame can be also detected, while in the inter frame mode, if instead of receiving $7E flag, the ST75C52/520 receive more than 7 consecutive "1". In this case only one Aborted frame is signaled, event if the "1" condition is maintained.

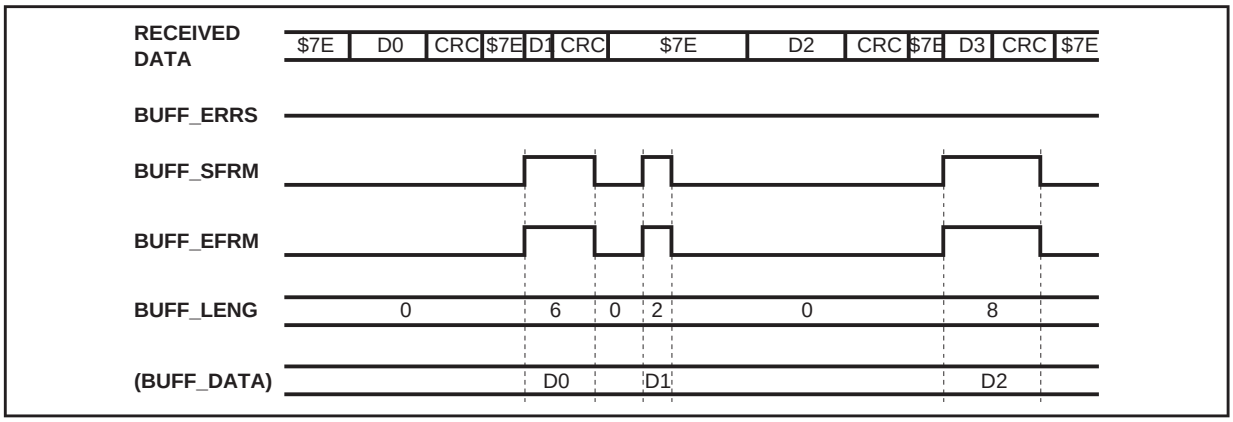
IV.8.6.2 - Status Word Format

Table 15

DTRBSx **in HDLC Mode**			
Field	**Pos.**	**Value**	**Definition**
BUFF_LENG	3 .. 0	0 1 2 .. 8 other	Buffer emty. 1 Byte received (**DTRBFx[0]**). 2 Bytes received (**DTRBFx[0]** and **DTRBFx[1]**). .. 8 Bytes received (**DTRBFx[0 .. 7]**). Not allowed.
BUFF_ERRS	5 .. 4	0 0 0 1 1 0 1 1	No error. CRC error. Non Byte-Aligned frame. Aborted frame.
BUFF_SFRM	6	0 1	Data stream. Start of frame : the buffer is a beginning of frame.
BUFF_EFRM	7	0 1	Data stream. End of frame : the buffer is a closing frame.

IV.8.6.3 - Single Short Frame

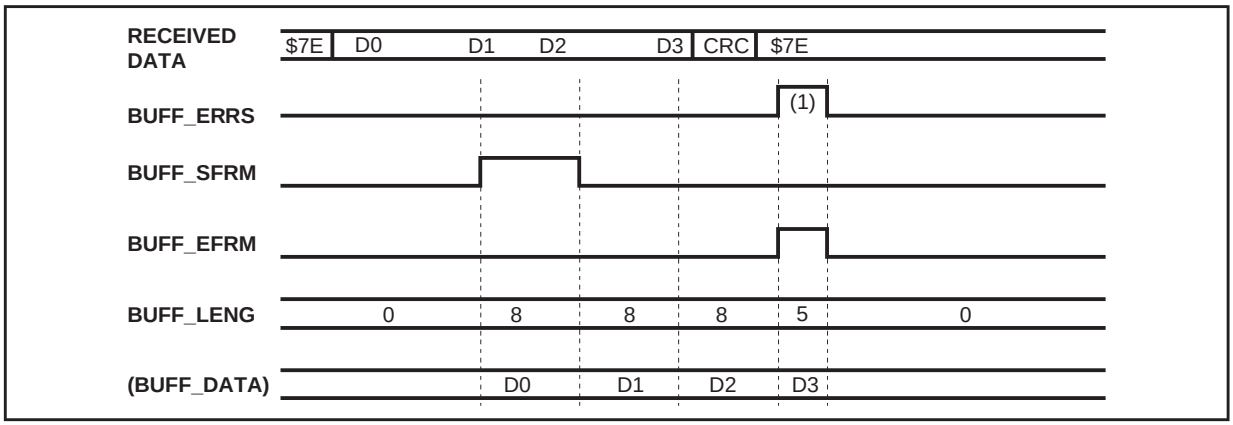
Figure 36



75C52-61.EPS

IV.8.6.4 - Long Frame

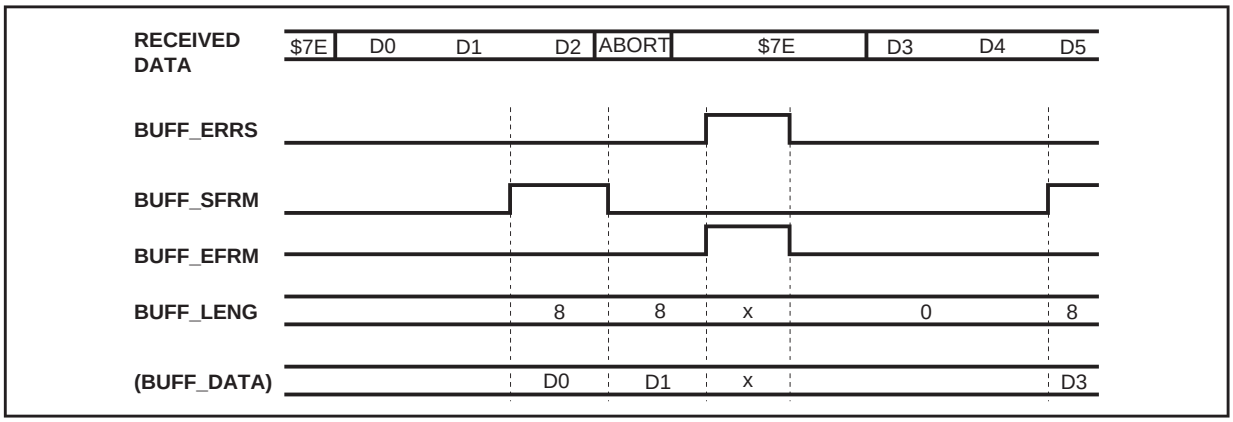
Figure 37



Note 1 : If error occurs during the reception, it is signaled in this last buffer.

IV.8.6.5 - Aborted Frame

Figure 38



V - TONE DETECTORS

For additional information about the TONE DETECTORS please refer to Chapter VIII of the ST75C52/520 Data Sheet.

V.1 - Computation of Tone Detector Coefficient and How to Change Them

1) Elementary Properties of IIR Filter

The filters included in the modem are biquad filter (see above) that is IIR filter. The most general form of the z transform of IIR can be written as :

$$H(z) = \frac{\sum_{i=0}^{M} b_i \cdot z^{-i}}{1 + \sum_{i=0}^{N} a_j \cdot z^{-j}}$$

The magnitude-squared response of a filter is defined as :

$$\left(\left| H\left[\exp\left(2 \cdot \pi \cdot j \cdot \frac{f}{Fe} \right) \right] \right| \right)^2$$

The poles and zeros of a magnitude-squared function are distributed with mirror-image symmetry with respect to the unit circle in the Z plane. The filter is stable if all poles of the transfer function are situated inside the unit circle in the z-plane. The group delay of a filter is a measure of the average delay of the filter as a function of frequency. A desirable group delay characteristic is approximately constant over the passband of the filter.

Choosing a filter type :
The well-known analog filter classes are the Butterworth, Chebyshev and Cauer or elliptic filter. If the characteristic of the filter is not severe, a Butterworth filter can be used because of the flat response in the passband and the small group delay . The drawback is a relatively wide transition band. If the characteristics of the filter are severe with a narrow transition band for instance, an elliptic filter should be chosen in order to minimize filter order. The drawback is a very non uniform group delay , especially a large value when approaching the passband edge.

2) Computation of Tone Detector Coefficients

We will take a Butterworth filter for a simplicity of tuning :

We have

$$B1(C,z) = \left(C_0 \cdot \frac{C_5 + 2 \cdot C_3 \cdot z^{-1} + 2 \cdot C_4 \cdot z^{-2}}{1 - 2 \cdot C_1 \cdot z^{-1} - 2 \cdot C_2 \cdot z^{-2}} \right) \cdot C_6 \cdot \frac{C_{11} + 2 \cdot C_9 \cdot z^{-1} + 2 \cdot C_{10} \cdot z^{-2}}{1 - 2 \cdot C_7 \cdot z^{-1} - 2 \cdot C_8 \cdot z^{-2}}$$

Let $C_3 = C_9 = 0$, $C_5 = C_{11} = 1$, $C_4 = C_{10} = -0.5$

This :

$$B1(C,z) = C_0 \cdot \frac{1 - z^{-2}}{1 - 2 \cdot R \cdot \cos(\theta) + R^2} \cdot C_6 \cdot \frac{1 - z^{-2}}{1 - 2 \cdot R_a \cdot \cos(\theta 1) + (R_a)^2}$$

with R = Ra

$C_1 = R \cdot \cos(\theta)$, $C_7 = R \cdot \cos(\theta 1)$,

$C_2 = -\frac{R^2}{2}$, $C_8 = -\frac{R^2}{2}$

This method is available for any frequency in the 400Hz -3kHz band. The radius of the tone detector pole was chosen so that each filter has a high Q factor without being unstable.
We choose R in the Table 16.

$$\theta = 2 \cdot \pi \cdot \frac{Fo}{Fe}$$

Were Fo is the desired center frequency and Fe is the sample frequency (Fe = 7200Hz).

We take two different filters, first one is centered on (Fo - Fa), second one on (Fo + Fa), were Fa is the frequency offset. The value of Fa is approximately 72% of the band width divided by 2.

$$\theta = 2 \cdot \pi \cdot \frac{Fo - Fa}{Fe} \qquad \theta 1 = 2 \cdot \pi \cdot \frac{Fo + Fa1}{Fe}$$

The value of Fa should be equal to Fa1. However, Fa may be choosen 1% smaller than Fa1 to compensate for the fact that the overall cascade response is not perfectly symmetrical.

The values for the coefficients C0 and C6 that give unity gain were measured and plotted versus center frequency Fo. Three equations corresponding to three linear approximations result :

$$400 \le f \le 1400 \quad C_0 = \frac{\frac{5}{16} \cdot f + 100}{32768} \quad (C0_f)$$

$$1400 \le f \le 2400 \quad C_0 = \frac{\frac{3}{32} \cdot f + 400}{32768} \quad (C01_f)$$

$$2400 \le f \le 3000 \quad C_0 = \frac{\frac{1}{8} \cdot f + 325}{32768} \quad (C02_f)$$

Figure 39

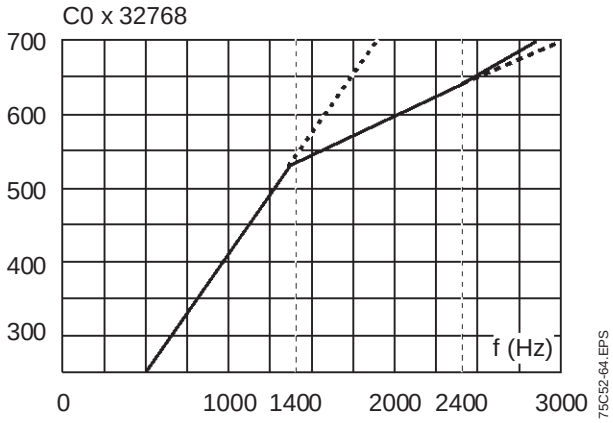


Table 16

Frequency Range	400-800Hz	800-1200Hz	1200-200Hz	2000-3000Hz
-((R x R) / 2) x 32767	$C084	$C0C4	$C0E6	$C147
R	0.996	0.994	0.993	0.990

V.1.1 - Computation of Tone Detector Coefficients using Mathcad Software

Mathcad software is a popular software from mathsoft Inc. We simply give an example of computation using this software to illustrated the above theory.

Tuning of coefficient for a band pass 1850Hz filter

*** Enter filter characteristic ***

Sampling Frequency Fe = 7200
Central Frequency Fo = 1850
Frequency offset Fa = 18

*** Define some Mathcad constant and formula ***

Default sampling Frequency Fe = 7200
Complex constant $j = \sqrt{-1}$
Complex Frequency Function $Z(f) = \exp\left(2 \cdot \pi \cdot j \frac{f}{Fe}\right)$
dB Function $dB(x) = 20 \cdot \log(x + 10^{-5})$
Hexadecimal Function H(x) = if (x < 32768, X, X - 65536)
Hexa to Fractional Function $D(x) = \frac{H(x)}{32768}$
Hexadecimal Display Function X(x) = if (x < 0, 65536 + x, x)
The transfer function is

$$B1(C,z) = C_0 \frac{C_5 + 2 \cdot C_3 \cdot z^{-1} + 2 \cdot C_4 \cdot z^{-2}}{1 - 2 \cdot C_1 \cdot z^{-1} - 2 \cdot C_2 \cdot z^{-2}} \cdot C_6 \frac{C_{11} + 2 \cdot C_9 \cdot z^{-2} + 2 \cdot C_{10} \cdot z^{-2}}{1 - 2 \cdot C_7 \cdot z^{-1} - 2 \cdot C_8 \cdot z^{-2}}$$

*** Extract Pole Location ***

Band pass center Frequency $\theta = 2\pi \cdot \frac{Fo - Fa}{Fe}$, $\theta 1 = 2\pi \cdot \frac{Fo + Fa}{Fe}$

Take care to have the good value of radius

$300 \le Fo \le 800$ R : = 0.996 $1200 \le Fo \le 2000$ R : = 0.993
$800 \le Fo \le 1200$ R : = 0.994 $2000 \le Fo \le 3000$ R : = 0.990
Fo = 1.85 · 103 then **Pole radius** : R = 0.993

*** Compute coefficients ***

Coefficients Formula k = 0 .. 11

$C_0 = \frac{\frac{3}{32} \cdot Fo + 400}{32768}$ $C_1 = R \cdot \cos(\theta)$ $C_2 = \frac{-R \cdot R}{2}$ $C_3 = 0$ $C_4 = -0.5$ $C_5 = 1 - \frac{1}{32768}$

$C_6 = \frac{\frac{3}{32} \cdot Fo + 400}{32768}$ $C_7 = R \cdot \cos(\theta 1)$ $C_8 = \frac{-R \cdot R}{2}$ $C_9 = 0$ $C_{10} = -0.5$ $C_{11} = 1 - \frac{1}{32768}$

Coefficients in Hexadecimal form : C_k =

H(023DH)
H(0FC74H)
H(0C0E6H)
H(0)
H(0C000H)
H(07FFFH)
H(023DH)
H(0F877H)
H(0C0E6H)
H(0)
H(0C000H)
H(07FFFH)

Coefficients to be downloaded into the Modem with TDWC commands

*** Compute Transfer Function ***

$C_k = \frac{C_k}{32768}$

Frequency Range : f = 0,1 .. 3000
$F1_f$ = dB (|B1(C,Z(f))|) $F1_{1850}$ = 0.387dB

*** Display Transfer Functions ***

Figure 40

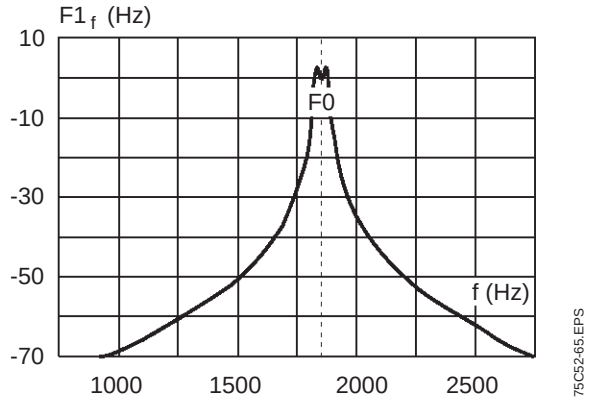
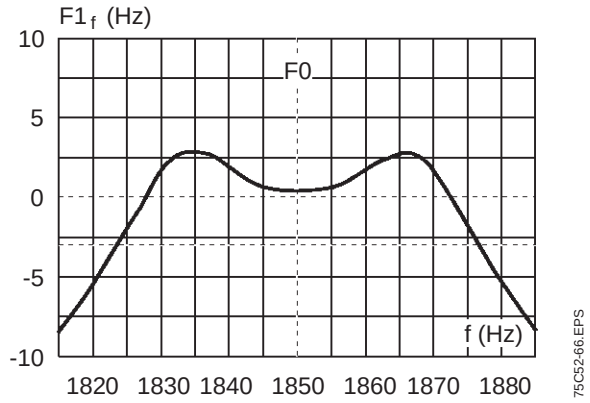


Figure 41



V.1.2 - Computation of Tone Detector Coefficients using TD Software

Tone Detector Description

Refer to the ST75C52/520 Data Sheet for detailed description of the tone detectors, Figure 2 (ST75C52/520 Data Sheet) for the Biquadratic IIR filter, Figure 3 for the Power estimator, Figure 4 for the tone detector wiring address (first half) and Figure 5 for the tone detector wiring address (second half). There are 16 programmable tone detector cells available. Each cell contains a 4th order IIR(biquadratic) filter, energy estimator consisting of an absolute value measurement and a 1st order low pass filter, 2-input comparator, and a static level. Detect information is sent to status word **TONEDET**. The user has the possibility of sending commands to the data pump to program the tone detectors for almost any desired transfer function. For each cell, the command **TDWC** can be used to program the 12 coefficients of the 4th order IIR filter (C0 to CB), the 1st order low pass filter coefficient, and the static level. The command **TDWW** can be used to program the wiring between cells for cascading and signal routing. One is free to program the IIR input, energy estimator input, and comparator + and - inputs.

Program TD Description

The user has the possibility of calculating his proper coefficients and determining the corresponding **TDWC** and **TDWW** commands manually but, the program TD was written to facilitate this task. The purpose of this chapter is to give the operating instructions for using program TD for quick development of the code needed to program the detectors.

Compatability and Input/Output

Program TD is written in FORTRAN and is executable on almost any PC with hard disk using MS-DOS. Input is from the keyboard and output is on the screen. Also, several useful files are generated by the program :

a) TD.SPC - contains trace of filter specifications given by user
b) TD.RES - shows floating-point frequency response of specified filter
c) TD.CCI - CCI commands needed for the data pump for specified filter

Starting the Program

To start the program, the user should first create a directory and load program TD.EXE into the directory. The command TD is now sent while in the created directory to start program execution. The program will then display ENTER TYPE. The following paragraph will describe the filter types.

Choosing a Filter Type

Four possible filter types are available to the user with the following characteristics :

BUTTERWORTH : This type of filter has a maximally flat pass-band with no ripple. It has multiple zeroes at half the sampling frequency (3600Hz) or D.C. or at the center of the band for band-stop configurations.

CHEBYCHEV : Equiripple in the pass band and flat response in the stop band which is particularly useful for band rejection filtering.

INVERSE CHEBYCHEV : Ripple-free pass band and more efficient than the Butterworth. For the same target design template, a lower order filter is necessary. Equiripple stop-band characteristics render this type useful for band-pass, low-pass or high-pass filtering.

ELLIPTIC : This type of filter is the most efficient and can have narrow transition bands. However, it is characterized by ripple in the pass and stop bands. Once the type is chosen, the program will ask for LOPASS, HIPASS, BANDPASS, or BAND REJECT filters.

Choosing a Filter Order

For all but Elliptic types, the program TD will ask the desired order. The user must specify the number of cascaded biquads (2nd order sections) desired.

Defining and Optimizing a Target Template

The corner frequencies for pass band and/or stop band are required by the program, and attenuation in the pass band and/or stop band for all types except Butterworth. These attenuations are in dB referenced from the input to the output. The program now calculates the transfer function in the Z domain displaying locations of poles and zeroes, and the required number of 4th order tone detector cells needed. This information is displayed on the screen and output to file TD.SPC. For the case of an Elliptic type, the order required is calculated from the transition band specified by the user, rather than specified directly by the user as for the other types. The order may be too high for the number of cells available or desired. The user may re-specify the filter. In general, one or more of the following steps may be performed, if the application enables it, to decrease the required order of an Elliptic type filter.

- change from band pass or band reject to lowpass or high pass,
- increase difference between pass band and stop band frequencies,
- increase the pass band ripple and/or decrease the stop band atten.

Using an iterative process, one can optimize the target specification of the filter before continuing to the next step.

Displaying the Ideal Frequency Response

The program TD will now calculate the frequency response of the specified filter and normalize coefficients to avoid overflow in the DSP ALU. The program now proceeds with the display of the frequency response on the screen. The user is asked by the program TD to specify start, stop, and step frequencies to facilitate interest in a particular portion of the frequency response. Once displayed, the program asks if the response is to be re-displayed allowing the user to change the frequency ranges. The desired frequency response is calculated in floating-point while the actual program implemented in the data pump uses a fixed-point DSP. In most cases, there should not be too much difference between the two calculation methods if the transition bands are not too narrow in the case of Elliptic types or the order is not too high for all types. At this point, the user has a better idea of the transition bands for Butterworth and Chebychev designs and also the unity gain loss. The normalization process may, in some cases to avoid overflow, result in an attenuation in the pass band or unity gain loss. Increasing the order of the Butterworth or Chebychev filters may be necessary for a narrower transition band. Widening of the transition band may be necessary for diminuing the unity gain loss of an Elliptic filter. In any case, the frequency response is written to file CP.RES for reference after the end of program execution. This can be especially useful for reference if several optimization attempts are desired.

Choosing the Used Cells

The program TD will now ask for the starting cell number (a number from 0 to F). The program will write CCI instructions for programming n (n= order/4) cells starting from the given address. The program cascades the biquadratic filters. However, only the last comparator and static level are used for the detection decision. This means that, eventually, the comparators or static levels for intermediate cells could be programmed for other functions. If the user, for example chooses 1 for the starting address, and there are 3 cells used, then the detection bit for this configuration will be available in **TONEDET(0)** position 3 (refer to ST75c5x data sheet). The user should choose a relatively low starting address beginning with the first unused position, if possible. This is because the execution time of the detectors in the non-idle mode may necessitate the utilizaton of less than 16 cells (NTDCELL .lt. 16 refer to ram mapping application note). In this case the higher cell numbers are not executed.

Selecting the Detection Thresholds

The detection threshold is now asked for by the program to define the minimum detectable input signal level at a pass band frequency with 0dB unity gain loss. The program will remind the user of the actual unity gain loss due to normalization and, in general, the desired threshold must be lowered by the number of dB in the unity gain loss. However, threshold levels lower than -50dBm are not reliable as the minimum dynamic range of the detectors will be surpassed.

Selecting the Energy Estimator Time Constant

The energy estimator time constant is now asked for by the program and the user will specify the value in milliseconds. A typical value of 8 is used for the default tone detectors but, if the user designs a filter with a particularly large group delay, he should also increase this value to avoid undesirable transients in the detection decision. Please note that group delay calculation is beyond the scope of this program and must be calculated by other techniques from the coefficients in TD.SPC.

Example Listings

The following listings give an example printout of the files TD.SPC, TD.RES, TD.CCI for a Butterworth 8th order low pass filter with cut-off frequency of 1000Hz.

```
EXAMPLE FOR 8th ORDER BUTTERWORTH
LPF FC=1000HZ, TH=-40dBM

        TD.SPC
        ------

 ENTER TYPE: 1 BUTTERW, 2 CHEBY, 3 ICHEBY, 4 ELLIP
   1
 ENTER 1 LOPASS, 2 HIPASS, 3 BPASS, 4 BREJ
   1
 ENTER NUMBER OF CASCADED BIQUADS DESIRED
   4
 ENTER BAND EDGE IN UN-NORMALIZED HZ
  1000.000
 Z PLANE
 #,   ZEROS  (REAL,  IMAG),     POLES (REAL, IMAG)
 1     -1.000000      0.000000     0.367029      0.085334
 2     -1.000000      0.000000     0.392676      0.259992
 3     -1.000000      0.000000     0.450892      0.446792
 4     -1.000000      0.000000     0.559214      0.653640
 5      1.000000      0.000000     1.000000      0.000000

        2 4TH ORDER TONE DETECTOR CELLS NEEDED !

 F(Z) = (Z*Z + B1Z + B2)/(Z*Z + A1Z + A2)
      1    2.000000    1.000000     -0.734059    0.141992
      2    2.000000    1.000000     -0.785351    0.221790
      3    2.000000    1.000000     -0.901784    0.402926
      4    2.000000    1.000000     -1.118428    0.739966

            TD.RES
            ------

 Freq(Hz):                                  Gain(dB):
 ---------                                  ---------
    0.**************************************************     0.0
  100.**************************************************     0.0
  200.**************************************************     0.0
  300.**************************************************     0.0
  400.**************************************************     0.0
  500.**************************************************     0.0
  600.**************************************************     0.0
  700.**************************************************     0.0
  800.**************************************************    -0.1
  900.*************************************************     -0.6
 1000.************************************************      -3.0
 1100.*********************************************          -8.3
 1200.*************************************                 -15.0
 1300.****************************                        -21.7
 1400.**********************                              -28.3
 1500.***************                                     -34.6
 1600.*********                                           -40.8
 1700.***                                                 -46.9
 1800.                                                    -53.0
 1900.                                                    -59.1
 2000.                                                    -65.2
 2100.                                                    -71.4
 2200.                                                    -77.8
 2300.                                                    -84.3
 2400.                                                    -91.2
 2500.                                                    -98.4
 2600.                                                   -100.0
 2700.                                                   -100.0
 2800.                                                   -100.0
 2900.                                                   -100.0
 3000.                                                   -100.0
 3100.                                                   -100.0
```

```
                TD.CCI
                ------

; 4TH ORDER BIQUAD CELL 9 COEFS
CCI TDWC 9 0 1B 1A
CCI TDWC 9 1 FA 2E
CCI TDWC 9 2 EA F6
CCI TDWC 9 3 00 40
CCI TDWC 9 4 00 20
CCI TDWC 9 5 00 40
CCI TDWC 9 6 EE 1B
CCI TDWC 9 7 43 32
CCI TDWC 9 8 CF F1
CCI TDWC 9 9 00 40
CCI TDWC 9 A 00 20
CCI TDWC 9 B 00 40
; 4TH ORDER BIQUAD CELL A COEFS
CCI TDWC A 0 12 20
CCI TDWC A 1 B6 39
CCI TDWC A 2 37 E6
CCI TDWC A 3 00 40
CCI TDWC A 4 00 20
CCI TDWC A 5 00 40
CCI TDWC A 6 9E 23
CCI TDWC A 7 94 47
CCI TDWC A 8 A5 D0
CCI TDWC A 9 78 47
CCI TDWC A A BC 23
CCI TDWC A B 78 47
; POWER ESTIMATOR AND BIQUAD INPUTS
CCI TDWW 9 0 19 02
CCI TDWW A 0 1A 19
; COMPARATOR - AND + INPUTS
CCI TDWW A 1 3A 2A
; DETECTION THRESHOLD AT  -40.00 DB
CCI TDWC A 20 70 00
; ENERGY TIME CONSTANT IS     8.00 MS
CCI TDWC A 10 E3 08
; CLEAR INTERNAL VARIABLES OF ALL USED CELLS
CCI TDZ 9
CCI TDZ A
```

V.2 - DTMF Detection

The way the DTMF detector is implemented is differential. First we split the 300Hz - 3kHz band signal in upper band and lower band. These two signals feed the input of 2 times 4 band filters (tuned on the 8 DTMF frequencies). To detect a valid DTMF signal, we check that the ratio between the upper band and the lower band is within plus or minus 8dB. Then we check if only one band pass detector is higher than the half band signal (either upper or lower band).

STAOPT0 and **STAOPT1** (in the optional status) indicate the tone detectors **TDT0** to **TDT15**. In this receive mode the 12 last tone detectors are set to detect the DTMF frequencies (the first 3 Tone detectors are unchanged).

Table 17

TDT0 : 440Hz (unchanged)
TDT1 : Wide Band (unchanged)
TDT2 : Call Progress low pass 650Hz (unchanged).
TDT3 : Not used
TDT4 : Low Pass 960Hz filter (Chebishev order 8)
TDT5 : High Pass 1190Hz filter (Chebishev order 8)
TDT6 : Not available
TDT7 : Not available
TDT8 : Band Pass 697Hz Filter ± 12Hz
TDT9 : Band Pass 770Hz Filter ± 13Hz
TDT10 : Band Pass 852Hz Filter ± 15Hz
TDT11 : Band Pass 941Hz Filter ± 16Hz
TDT12 : Band Pass 1209Hz Filter ± 20Hz
TDT13 : Band Pass 1336Hz Filter ± 22Hz
TDT14 : Band Pass 1477Hz Filter ± 24Hz
TDT15 : Band Pass 1633Hz Filter ± 26Hz

Figure 42

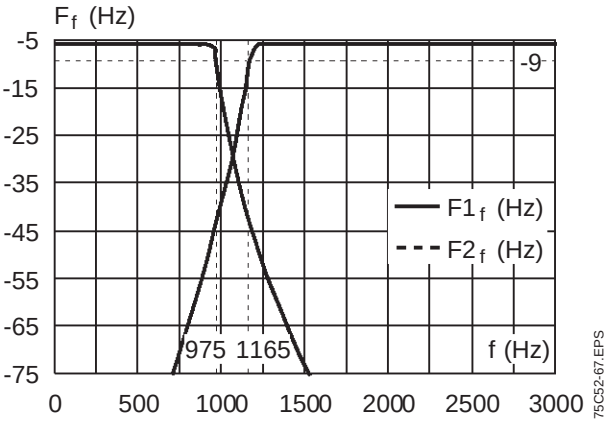


Figure 43

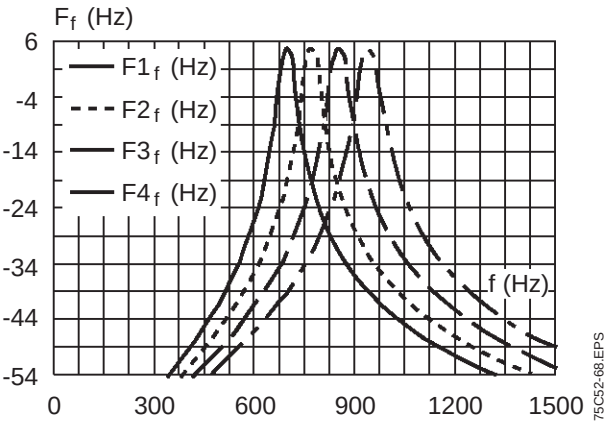
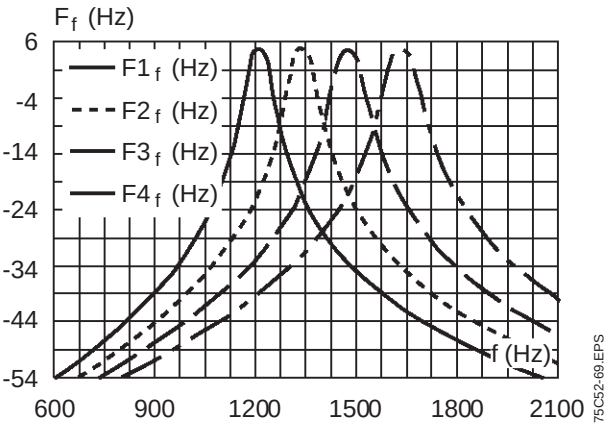


Figure 44



Hereafter are given the coefficients for the different filters used in DTMF detection.

Coefficients for Low Pass Filter from C0 to C23 are :
300h, 6BE2h, D117h, 401Ch, 200Eh, 401Ch, DB9h, 638Ch, CE22h, 20BFh, 105Fh, 20BFh, 1C6Eh, 592Ch, C934h, 4065h, 2032h, 4065h, 212Eh, 53EAh, C33Eh, 4C16h, 260Bh, 4C16h

Coefficients for High Pass Filter from C0 to C23 are :
1C8Eh, C933h, EB14h, BB3Fh, 2260h, 44C1h, 5975h, 249h, DA0Dh, B9FDh, 2301h, 4603h, 6E54h, 2BC0h, CC87h, A6E1h, 2C8Fh, 591Fh, 2DE8h, 3EE4h, C3C4h, 8000h, 4000h, 7FFFh

Coefficients for Band Pass 697Hz Filter from C0 to C11 are :
26Ah, 671Dh, C164h, 0, C000h, 7FFFh, 2A8h, 68B6h, C15Ah, 0, C000h, 7FFFh

Coefficients for Band Pass 770Hz Filter from C0 to C11 are :
2E8h, 6213h, C180h, 0, C000h, 7FFFh, 2CBh, 63F2h, C175h, 0, C549h, 756Dh

Coefficients for Band Pass 852Hz Filter from C0 to C11 are :
378h, 5BE9h, C1A4h, 0, C000h, 7FFFh, 30Eh, 5E22h, C199h, 0, C9FDh, 6C04h

Coefficients for Band Pass 941Hz Filter from C0 to C11 are :
35Bh, 574Fh, 408h, 54B4h, C1C8h, 0, C000h, 7FFFh, C1BDh, 0, CDFFh, 6401h

Coefficients for Band Pass 1209Hz Filter from C0 to C11 are :
5D6h, 3C1Eh, C237h, 0, C000h, 7FFFh, 44Bh, 3FF4h, C22Ch, 0, D60Eh, 53E3h

Coefficients for Band Pass 1336Hz Filter from C0 to C11 are :
6BAh, 2F45h, C269h, 0, C000h, 7FFFh, 4ABh, 33ADh, C25Fh, 0, D846h, 4F72h

Coefficients for Band Pass 1477Hz Filter from C0 to C11 are :
7A1h, 2058h, C2A3h, 0, C000h, 7FFFh, 52Bh, 2563h, C29Bh, 0, D9EFh, 4C1Fh

Coefficients for Band Pass 1633Hz Filter from C0 to C11 are :
891h, F53h, C2E1h, 0, C000h, 7FFFh, 5B2h, 1501h, C2DCh, 0, DB27h, 49B0h

V.3 - Default Tone Detectors ST75C52/520

Cell Description

The first cell (# 0) is programmed as a 440Hz tone detector (Call Waiting Detection) and is never changed whatever the DSP is doing. After a RESET (or INIT command) or any conf command, its parameters are set to detect the 440Hz single tone.
The Template of this filter is :

Table 18

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
Callwait	0	Band Pass	430,450Hz	360,530Hz	0.1	25

The second and third cell (#1 and #2) are used for Call progress detection. It is a Low pass filter with a cutt of frequency of 650Hz. This filter like the previous one is never changed.
The Template of this filter is :

Table 19

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
Cplow	1,2	Low Pass	0,650Hz	1000Hz	0.2	45

The cells number 3 and 4 are used for Call progress tone detection. It is a High pass filter with a cutoff frequency of 600Hz.
The Template of this filter is :

Table 20

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
Cphigh	3,4	High Pass	600,3600Hz	400Hz	0.2	45

While using the DTMF Mode (with a conf command) the cell 4 to 15 are overwritted with the DTMF detector parameters.

Cells number 5 and 6 are not used

The cell number 7 is used to detect the 462Hz single tone. It is a band pass filter.
The Template of this filter is :

Table 21

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN462	7	Band Pass	448,476Hz	340,540Hz	0.3	45

Cell number 8 is used to detect the 1100Hz single Tone.
The Template of this filter is :

Table 22

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN1100	8	Band Pass	1070,1130Hz	1000,1275Hz	0.3	45

Cell number 9 is used to detect the 1300Hz single Tone.
The Template of this filter is :

Table 23

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN1300	9	Band Pass	1275,1325Hz	1000,1600Hz	0.5	45

Cells number 10 and 11 are used to detect the V21.1650Hz Mark Tone.
The Template of this filter is :

Table 24

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
AN1650	10,11	Band Pass	1625,1675Hz	1500,1800Hz	0.1	45

Cells number 12 and 13 are used to detect ITU2100Hz Answer Tone.
The Template of this filter is :

Table 25

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
ANS2100	12,13	Band Pass	2080,2120Hz	2030,2170Hz	0.3	45

Cells number 14 and 15 are used to detect 2225Hz Answer Tone.
The Template of this filter is :

Table 26

Name	Cell Number	Type	Pass Band	Stop Band	Ripple (dB)	Reject (dB)
ANS2225	14,15	Band Pass	2205,2270Hz	2140,2360Hz	0.5	45

Bit Description

Refer to the figure hereunder for the default wiring of the cells.
The 16 bits output of the tone detectors have the following meaning :

Table 27

Tonedet Word	Tonedet Bit	Filter Function	Biquad	Power	Level
0	0	Band pass 440Hz	Cell 0	Cell 0	Cell 0
0	1	Flat (signal > -21dBm)	-	Cell 1	Cell 1
0	2	Call progress low pass 650Hz	Cell 1,2	Cell 2	Cell 2
0	3	Call progress high pass 600Hz	Cell 3,4	Cell 3	Cell 3
0	4	CP High < CP Low	-	-	-
0	5	Not used	-	-	-
0	6	Not used	-	-	-
0	7	Band pass 462Hz	Cell 7	Cell 7	Cell 7
1	0	Band pass 1100Hz	Cell 8	Cell 8	Cell 8
1	1	Band pass 1300Hz	Cell 9	Cell 9	Cell 9
1	2	Band pass 1650Hz	Cell A,B	Cell B	Cell A
1	3	Not used	-	-	-
1	4	Band pass 2100Hz	Cell C,D	Cell D	Cell C
1	5	Not used	-	-	-
1	6	Band pass 2225Hz	Cell E,F	Cell F	Cell E
1	7	Not used	-	-	-

Note : Biquad of cells 5 and 6 are not used. Power of cells 4, 5, 6, A, C and E are not used. Level of cells 4, 5, 6, B, D and F are not used.

Figure 45 : Tone Detector Wiring Address (first half)

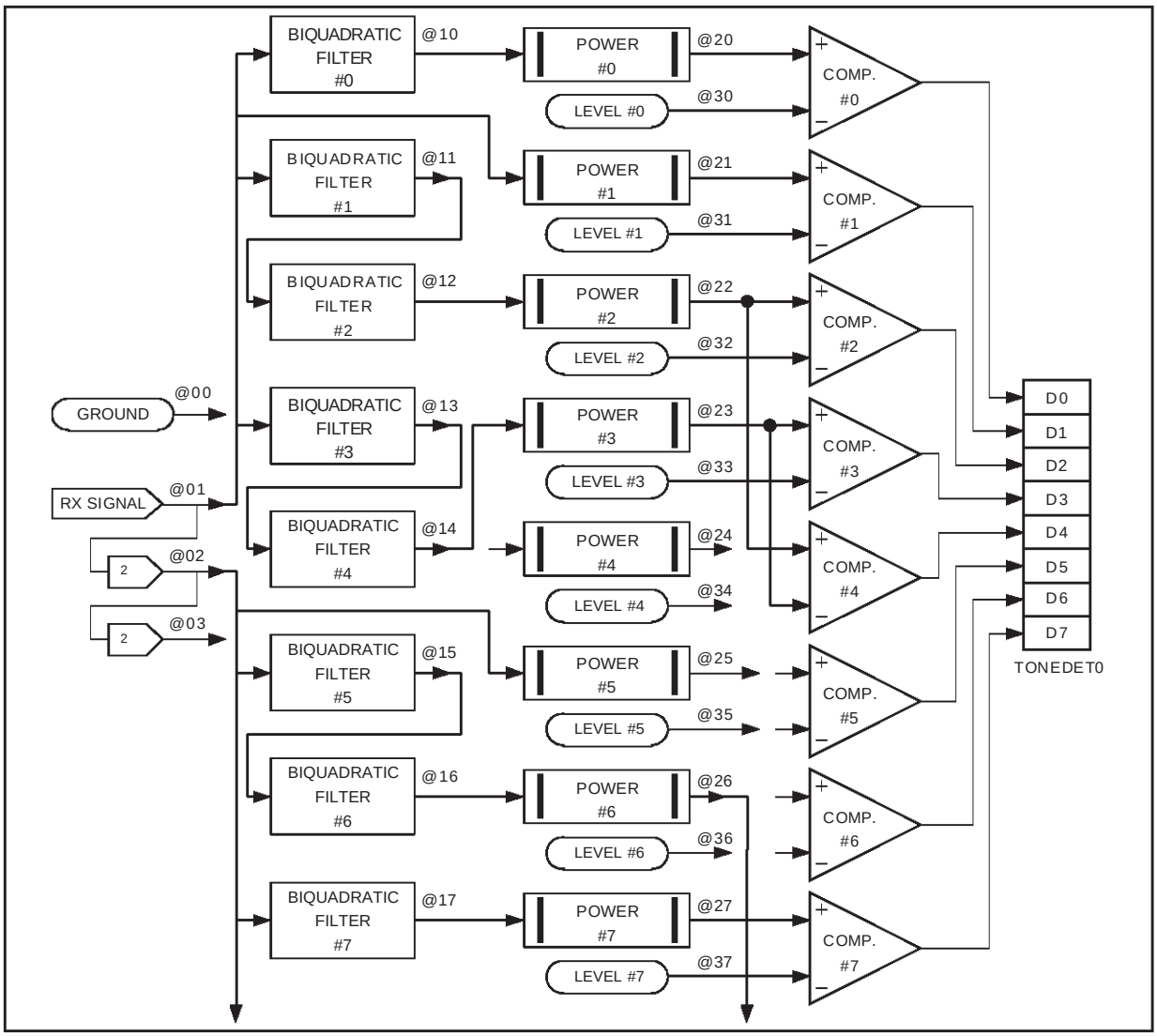
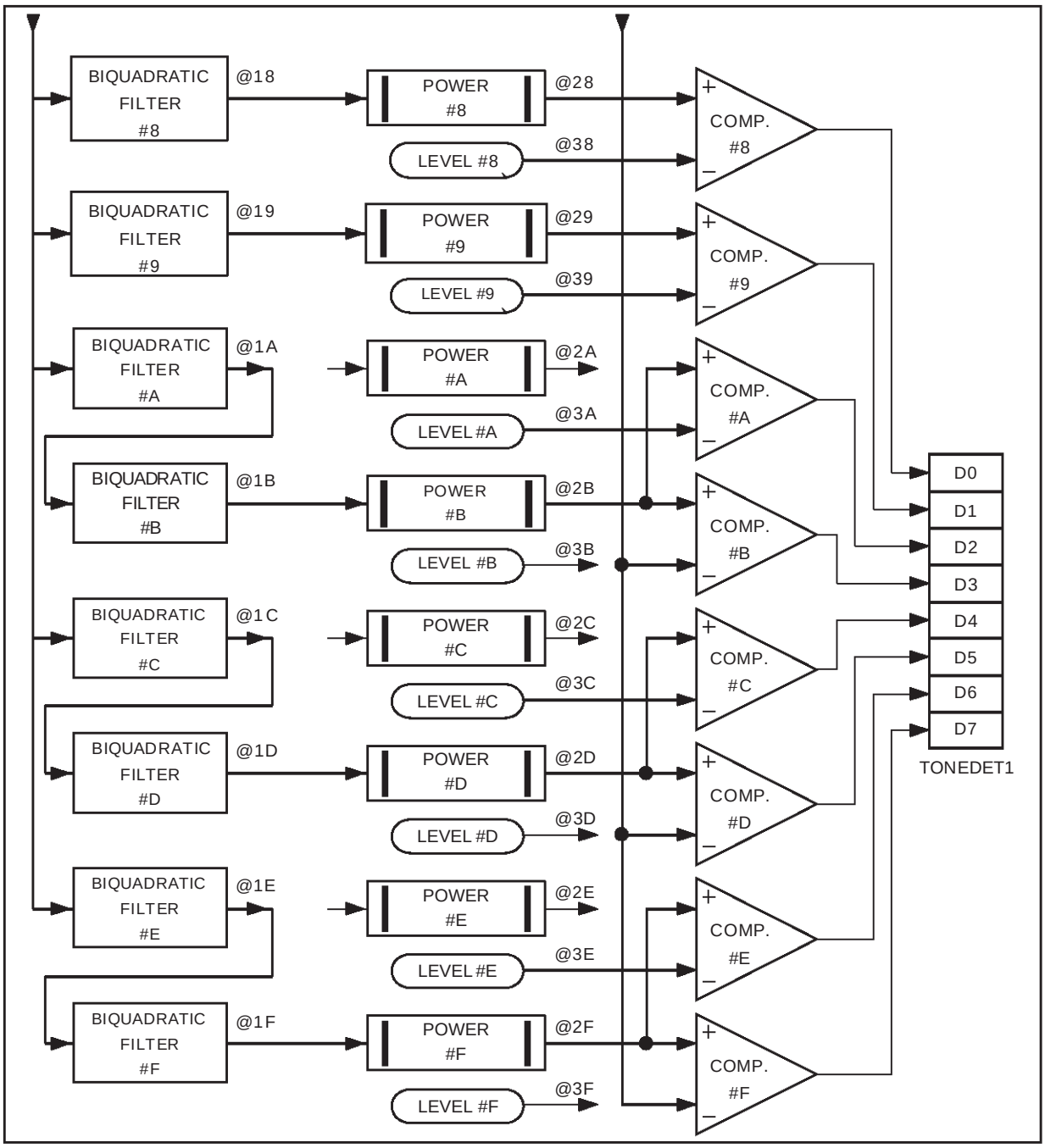
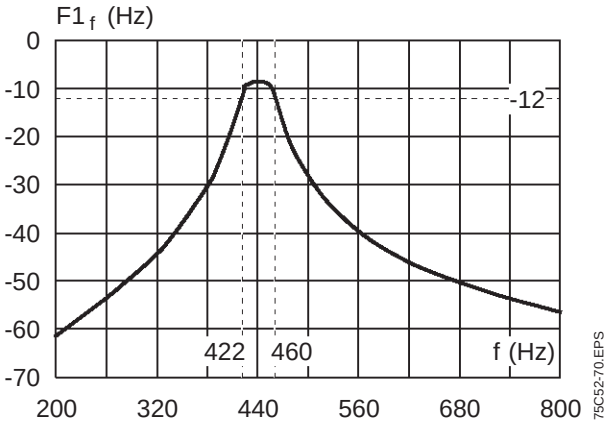


Figure 46 : Tone Detector Wiring Address (second half)



V.3.1 - Band Pass 440Hz Filter

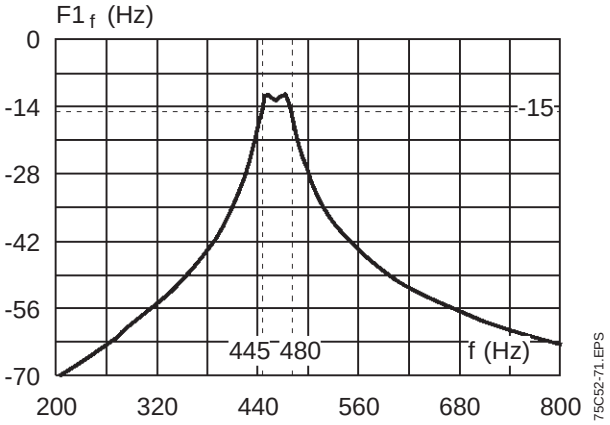
Figure 47



Coefficients for band pass 440Hz filter from Co to C11 are :
085h, 74D7h, C15Ah, 0,C000h, 7FFFh, 02D4h, 760F, C146h, 0, C000h, 7FFFh

V.3.2 - Band Pass 462Hz Filter

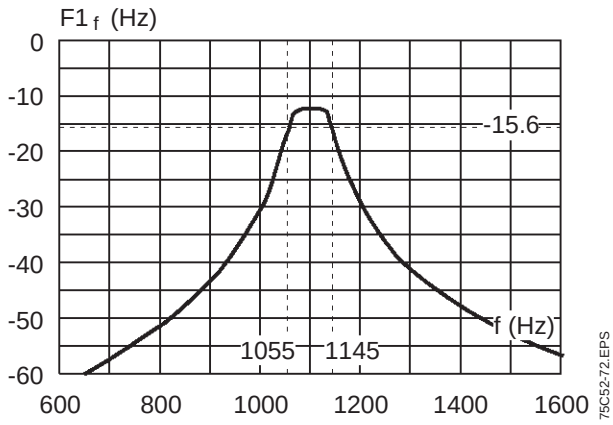
Figure 48



Coefficients for band pass 462Hz filter from C0 to C11 are :
066H, 7461H, C0E0H, 0 , C000H , 7FFFH, 0251H, 7583H, C0D5H, 0 , D555H, 5554H

V.3.3 - Band Pass 1100Hz Filter

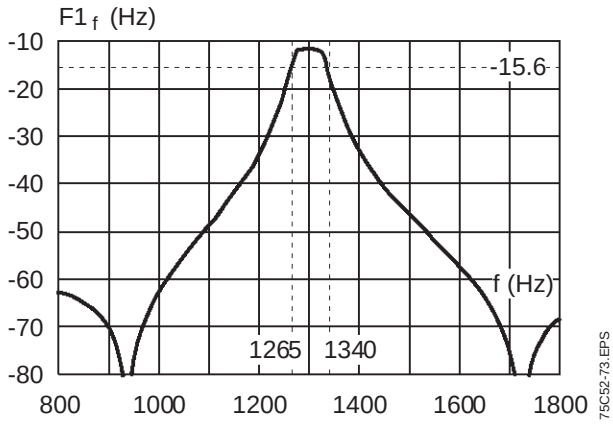
Figure 49



Coefficients for band pass 1100Hz filter from C0 to C11 are :
1FDh, 4551h, C263h, 0, C000h, 7FFFh, 64Dh, 4AC7h, C24Eh, 0, EC8Ah, 26EBh

V.3.4 - Band Pass 1300Hz Filter

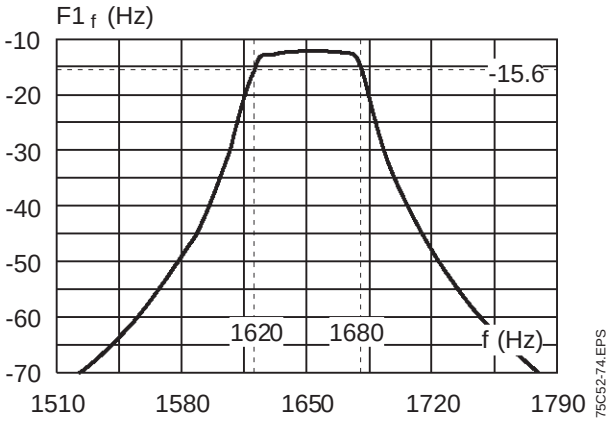
Figure 50



Coefficients for band pass 1300Hz filter from C0 to C11 are :
1DFh, 32BDh, C1FAh, F788h, 4000h, 7FFFh, C95H, 37C6h, C1F0h, A882h, 4000h, 7FFFh

V.3.5 - Band Pass 1650Hz Filter

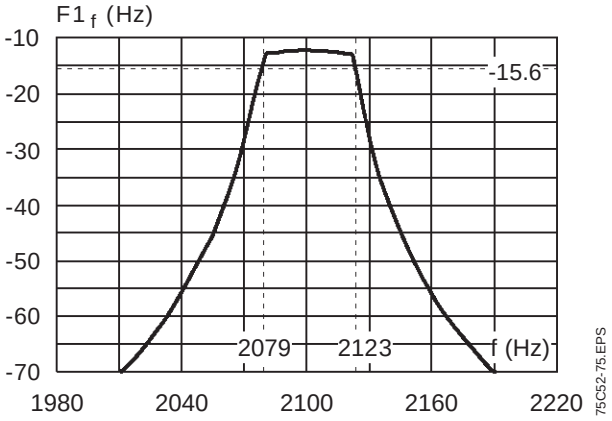
Figure 51



Coefficients for band pass 1650Hz filter from C0 to C23 are :
1C1h, F35h, C1C3h, 0, C000H, 7FFFh, 2ABh, 11C0h, C1C2h, 0, C000h, 7FFFh, 1E7h, D83h, C0BDh, 0, C000H, 7FFFh, 54Fh, 13B2h, C0BCh, 0, F0B6h, 1E91h

V.3.6 - Band Pass 2100Hz Filter

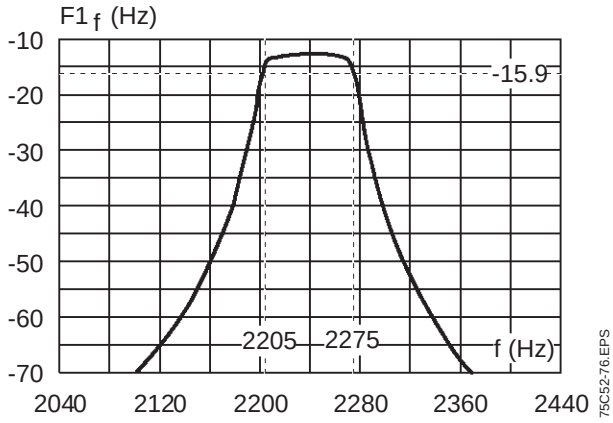
Figure 52



Coefficients for band pass 2100Hz filter from C0 to C23 are :
10Fh, E014h, C116h, 0, C000h, 7FFFh, 1E7h, DE39h, C115h, 0, C000h, 7FFFh, 13Dh, E13Eh, C074h, 0, C000h, 7FFFh, 468h, DCBFh, C073h, 0, F017h, 1FD1h

V.3.7 - Band Pass 2225Hz Filter

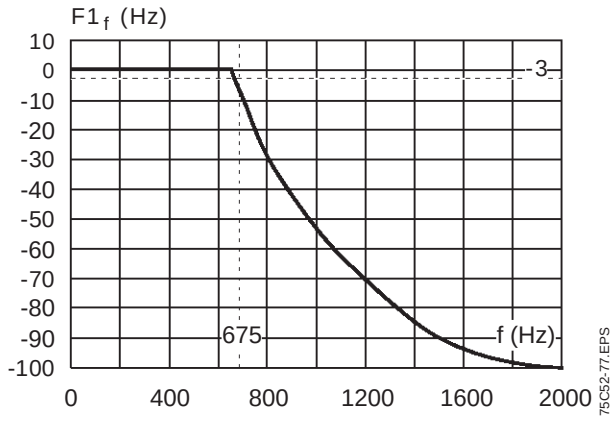
Figure 53



Coefficients for band pass 2225Hz from C0 to C23 are :
17Bh, D245h, C187h, 0, C000h, 7FFFh, 2DEh, CF76h, C183h, 0, C000h, 7FFFh, 206h, D3FAh, C0A4h, 0, C000h, 7FFFh, 672h, CD29h, C0A1h, 0, EFDFh, 203Fh

V.3.8 - Low Pass 650Hz Filter

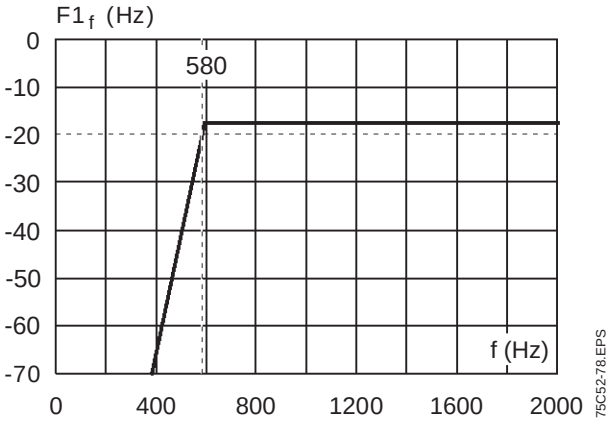
Figure 54



Coefficients for low pass 650Hz filter from C0 to C23 are :
230h, 6C2Ch, D1A8h, 3FFFh, 1FFFh, 3FFFh, 738h, 69CAh, CEFDh, 4000h, 2000h, 4000h, E73h, 6760h, CA21h, 400Eh, 2007h, 400Eh, 124Dh, 681Bh, C3ACh, 453Ch, 229Eh, 453Ch

V.3.9 - High Pass 600Hz Filter

Figure 55



Coefficients for high pass 600Hz filter from C0 to C23 are :
33C0h, 116Dh, F836h, 91ACh, 372Ah, 6E54h, 44C4h, 4527h, DB80h, 8000h, 4000h, 7FFFh, 3ED0h, 608Fh, CB9Fh, 8000h, 4000h, 7FFFh, 20ACh, 6C9Dh, C350h, 8001h, 4000h, 7FFFh

VI - CONTROL IN TRANSMIT MODE

VI.1 - Analog Hybrid Implementation

The following schematic shows the hybrid used on the ST9 SGS-THOMSON application board. This hybrid is designed to use the ST75C52/520'smaximum performances (differential Input and Output). The operational amplifier U1 is only used for transmit purpose and powered between +12V and -12V. The reference signal (Pin 3 and 5 of U1) is tied to V_{CM} which is the reference for the ST75C52/520 sigma delta digital to analog convertor.

The user could connect Pin 3 and 5 of U1 to the analog ground. In such a case TXA1 and TXA2 must be connected to the 13.2kΩ resistors through capacitors (minimum 100nF).

The Transmit Gain is given by the ratio 22kΩ/13.2kΩ. It gives a default level of -9dBm on the telephone line. We have a full differential low-pass filter on transmit side before the DAA (second order) with Fc = 19.6kHz.

The return loss (very important parameter) could be adjusted by changing R3. In fact R3 value depentson the transformer. In our case R3 = 220Ω.

VI.2 - Default Level (Tones, Carriers, DTMF)

The following table gives the default level on the telephone line for all the possible carriers, the tones (predifined), and the DTMF signals.

Table 28

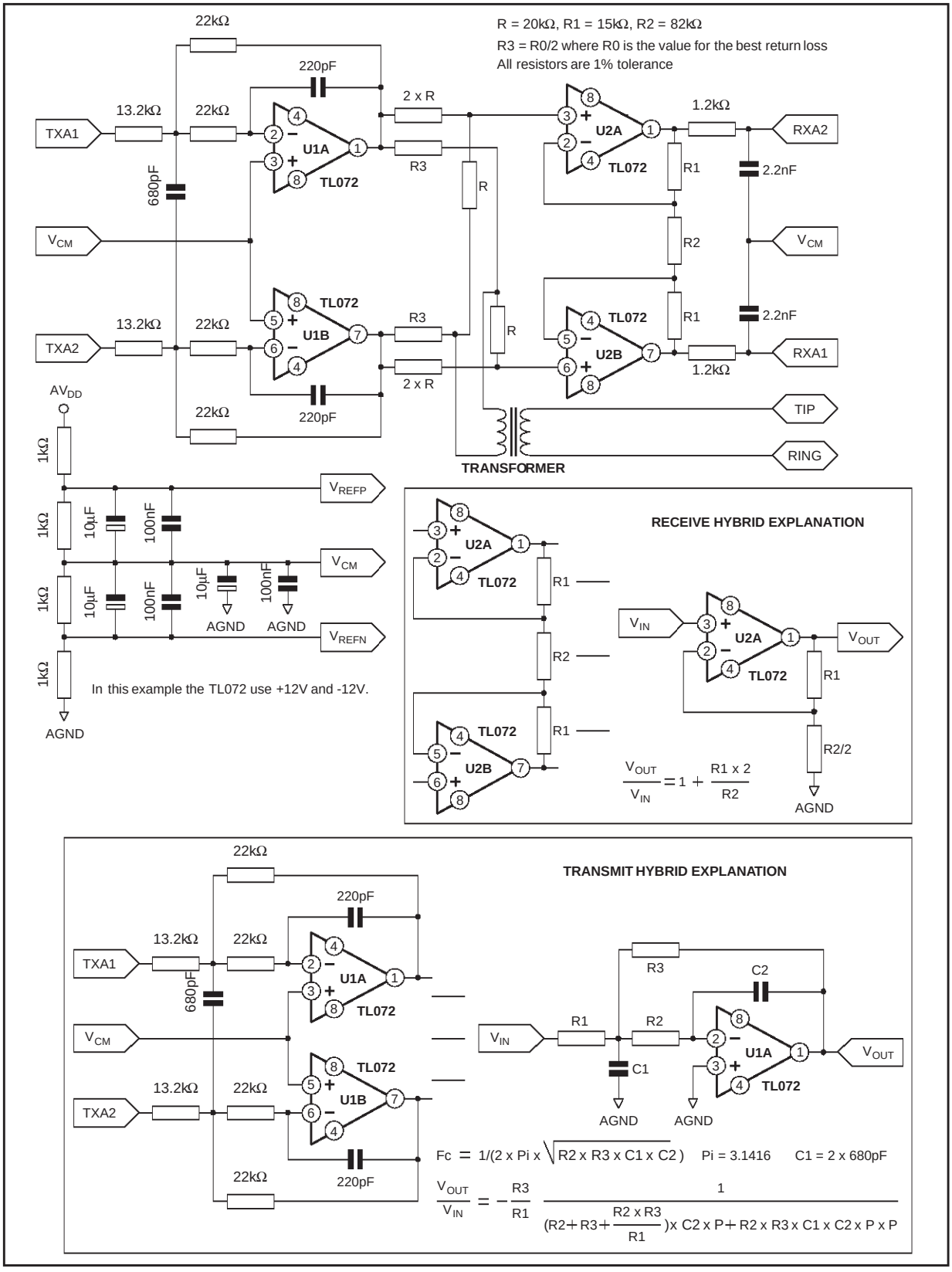
Signal	Default Level (dBm)
Bell 103 Originate	- 8.8
Bell 103 Answer	- 8.6
V.23 Originate	- 9.2
V.23 Answer	- 9.1
V.21 Originate	- 8.7
V.21 Answer	- 8.8
V.21 ch2	- 8.8
V.27 ter	- 8.9
V.29	- 8.8
V.17	- 9
V.33	- 9

Hybrid implementation for differential input and output (all the levels given in the chapter where measured with this schematic) (see Figure 56).

Table 29

Signal	Default Level (dBm)
DTMF0	- 9.32
DTMF1	- 9.31
DTMF2	- 9.33
DTMF3	- 9.37
DTMF4	- 9.3
DTMF5	- 9.32
DTMF6	- 9.36
DTMF7	- 9.29
DTMF8	- 9.32
DTMF9	- 9.35
DTMFA	- 9.4
DTMFB	- 9.39
DTMFC	- 9.39
DTMFD	- 9.39
DTMF*	- 9.29
DTMF#	- 9.35
2100Hz	- 9.38
2225Hz	- 9.46
1300Hz	- 9
1650Hz	- 9.13

Figure 56 : High Performance Differential Hybrid



VI.3 - How to Adjust Level Transmission

The user can adjust the level on the line with the SET OUTPUT GAIN (**SETGN**) command, which is done to set the Scaling Factor of the Transmit samples. **SETGN** is used for setting both the output level or the tone generators level. The gain value is given in the form of a 2's complement 16-bit value. **SETGN** parameters are given in two bytes :

Table 30

Field	Byte	Pos.	Value	Definition
GAIN_L	1	7..0	range FF*	Low byte of the 16-Bit gain value
GAIN_H	2	7..0	range 7F*	High byte of the 16-bit gain value

Table 31 : Examples

Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)	Gain (dB)	Gain (Hex)
0	7FFF	- 5	47FA	- 10	287A
- 1	7214	- 6	4026	- 11	2413
- 2	65AC	- 7	392C	- 12	2026
- 3	5A9D	- 8	32F5	- 13	1CA7
- 4	50C3	- 9	2D6A	- 14	198A

The default level for DTMF is tuned to obtain -9dBm on the telephone line with the default value of SETGN (7FFF or 0dB). To increase the level of the DTMF the user must use the variable **TGNBLK** for the tone generator 0 and the the tone generator 1.

For example to obtain -4.5dBm on the line, the amplitude must be multipled by 1.73. The actual amplitude for tone generator 0 and tone generator 1 are located at address $11EE and $11F1. The default values are read with the **MR** command and the new values are initialized with the **MW** command.

The sequence is :

MR EE 11 : Read the tone generator 0 amplitude
COMREP[0] = 36 : Low byte value
COMREP[1] = 0F : High byte value
MW EE 11 50 1A : Write new tone generator 0 amplitude
MR F1 11 : Read the tone generator 1 amplitude
COMREP[0] = 7A : Low byte value
COMREP[1] = 13 : High byte value
MW F1 11 B1 21 : Write new tone generator 1 amplitude

The value which will be used for **SETGN** will add or substract dB to the new tone generator amplitude.

If we want to decrease the level given in Chapter VI.2 (default level) by 2dB for example we only have to send **STEGN AC 65**. The following tables show the new levels measured on the telephone line after a 2dB theoric attenuation.

Table 32 : Example

Signal	Default Level (dBm)	Attenuated Signal with SETGN (dBm)
Bell 103 Originate	- 8.8	- 10.8
Bell 103 Answer	- 8.6	- 10.6
V.23 Originate	- 9.2	- 11.2
V.23 Answer	- 9.1	- 11.1
V.21 Originate	- 8.7	- 10.7
V.21 Answer	- 8.8	- 10.8
V.21 ch2	- 8.8	- 10.8
V.27 ter	- 8.9	- 10.8
V.29	- 8.8	- 10.8
V.17	- 9	- 11
V.33	- 9	- 11

Table 33 : Example

Signal	Default Level (dBm)	Attenuated Signal with SETGN (dBm)
DTMF0	- 9.32	- 11.32
DTMF1	- 9.31	- 11.31
DTMF2	- 9.33	- 11.33
DTMF3	- 9.37	- 11.37
DTMF4	- 9.3	- 11.3
DTMF5	- 9.32	- 11.32
DTMF6	- 9.36	- 11.36
DTMF7	- 9.29	- 11.29
DTMF8	- 9.32	- 11.32
DTMF9	- 9.35	- 11.35
DTMFA	- 9.4	- 11.4
DTMFB	- 9.39	- 11.39
DTMFC	- 9.39	- 11.39
DTMFD	- 9.39	- 11.39
DTMF*	- 9.29	- 11.29
DTMF#	- 9.35	- 11.35
2100Hz	- 9.38	- 11.38
2225Hz	- 9.46	- 11.46
1300Hz	- 9	- 11.0
1650Hz	- 9.13	- 11.13

VI.4 - Transmit Equalizers

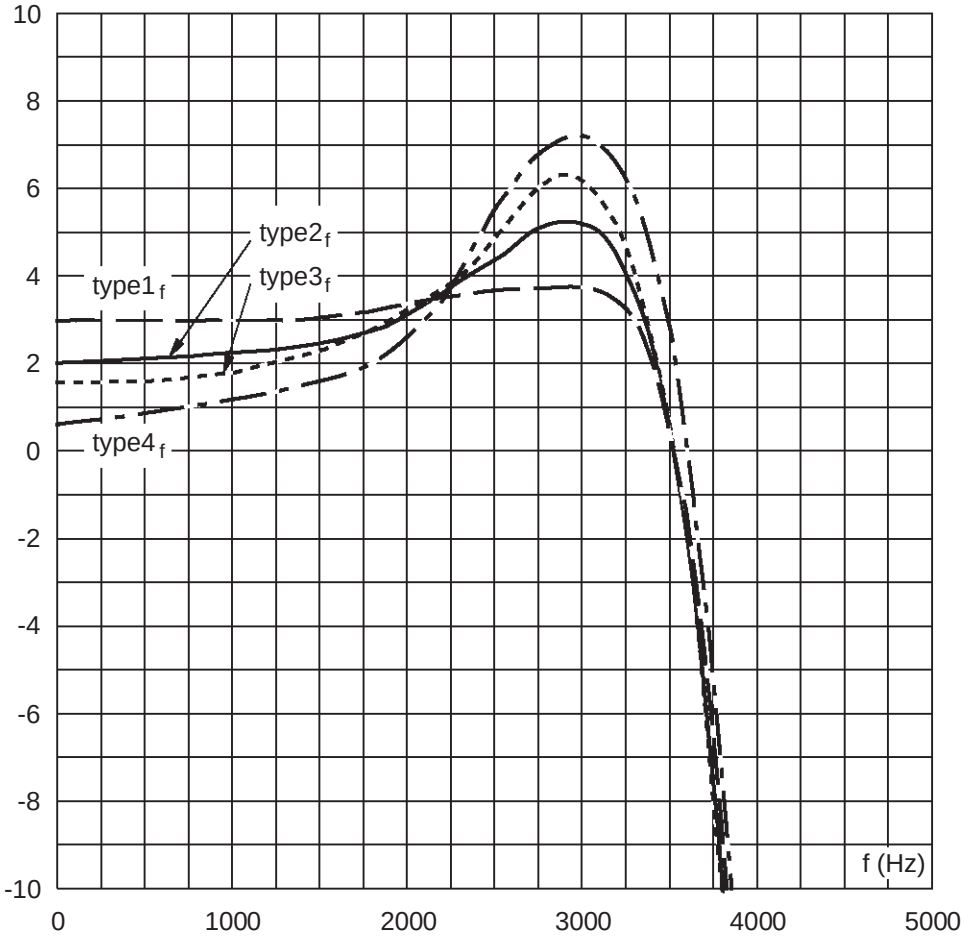
The following types of equalizers are built into the modem to improve the transmission performance when the line conditions are poor. They are also built to compensate the interpolation filter of the analog front end part of the ST75C52/520.

4 equalizers can be selected :

- type 0 built to compensate just the filter of the analog front end part,
- type 1 built to compensate the filter of the analog front end and the amplitude distorsion of the 0.4mm diameter non-loaded cables of 1.8km,
- type 2 built to compensate the filter of the analog front end and the amplitude distorsion of the 0.4mm diameter non-loaded cables of 3.6km,
- type 3 built to compensate the filter of the analog front end and the amplitude distorsion of the 0.4mm diameter non-loaded cables of 7.2km.

The characteristics of amplitude equalizers are ploted on the figure hereunder (see Figure 57).

Figure 57 : Amplitude Equalizer Characteristics



VII - CONTROL IN RECEIVE MODE

VII.1 - Analog Hybrid Implementation

Refer to the schematic showed in Chapter VI.1. As for the transmit hybrid the receive hybrid is designed to use the ST75C52/520's maximum performances (differential Input). The operational amplifier U2 is only used for reception purpose and powered between +12V and -12V. This analog interface allows to receive a signal up to 0dBm.

The receive gain is given by the formula Grec = 1 + (R1x2)/R2, with R1 = 15kΩ and R2 = 82kΩ.

Both RXA1 and RXA2 must be referenced to V_{CM}.

VII.2 - Carrier Detect Signal

The DSP uses the following internal variables for carrier detection :

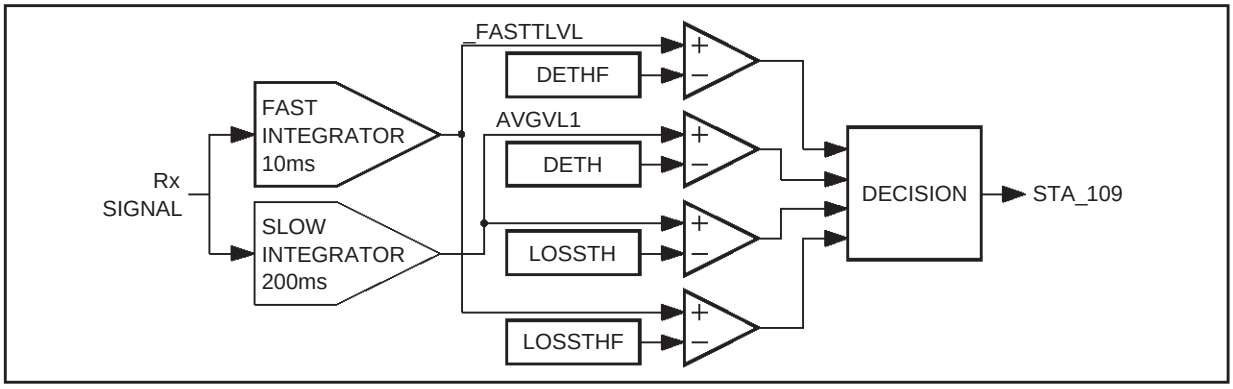
DETHF(R/W)	Fast detection threshold	at address $16C2
DETH (R/W)	Slow detection threshold	at address $16C1
LOSSTH (R/W)	Slow loss threshold	at address $16C4
LOSSTHF (R/W)	Fast loss threshold	at address $16C3

The carrier detect is displayed on status byte 0, bit 0 as well as on the **CD** pin of the ST75C52/520 serial interface and is active at the end of the synchronization sequence for V.17, V.29, V.27, V.21 ch 2 provided the detection threshold has been reached. For FSK modes, it is active provided the threshold has been reached. The carrier detect algorithms use, 2 signal level integrators a fast integrator for quick detection with a limited precision and a slow integrator for enhanced precision. There are four thresholds programmed with default values for each of the modes V.33, V.17, FSK, V.29, and V.27 which can be modified by the user after the conf command. Typical values for V.17 are shown below as an example and doubling the value read will increase the threshold by approximately 6dB :

(-40dBm)	$167	DETHF (fast detection threshold)
(-44dBm)	$140	DETH (slow detection threshold)
(-47dBm)	$D0	LOSSTH (slow loss threshold)
(-51dBm)	$A0	LOSSTHF (fast loss threshold)

note that it is mandatory to have :
DETHF > DETH > LOSSTH > LOSSTHF

Figure 58



AVGLVL1 (R) Carrier detect level.
This level is the ouput of the slow level integrator with a 200ms time constant. The formula for the rx lvl on the line for a V.17 receive signal, for example, is a function of x, the value of the variable at address AVGLVL1 :
RxLevel = 20 * log(x) - 93 in dBm

_FASTLVL (R) Fast carrier detect level.
This level is the output of the fast level integrator calculated with a 10ms time constant and obeying the same formula as above with, of course, more ripple for a given level due to the smaller time constant.

VII.3 - Received Signal Dynamic Range

The received signal dynamic range mainly depents of the hybrid. The ST75C52/520 with the above hybrid using the differential input can receive carrier up to 0dBm. Be careful that the hybrid is powered between +12V and -12V.

Carrier detection threshold is -44dBm, and carrier loss threshold is -47dBm.

DTMF detection is only possible for level higher than -35dBm.

Tone detector detection thresholds are programmable from -45dBm up to -10dBm.

All the results given in this chapter refer to the above hybrid (Chapter VI.1).

The table hereafter summarizes the test results for the carrier detection. You will find detection level, droptout level and hysteresis for fax modes. Tests were done on Automatic Modem Test Equipment AUTOTEST 1AE AEA.

Table 34

Modes	Detection (dBm)	Dropout (dBm)	Hysteresis (dB)
V.17 14400bps	44.06	46.38	2.32
V.17 1200bps	44.06	46.38	2.32
V.17 9600bps	44.06	46.38	2.32
V.17 7200bps	44.36	46.8	2.44
V.29 9600bps	44.5	46.22	1.72
V.29 7200bps	44.5	46.22	1.72
V.29 4800bps	43.62	46.7	3.08
V.27 4800bps	44.02	47	2.98
V.27 2400bps	44.2	47	2.8
V.21 Channel 2	44.2	46.2	2

The table hereafter summarizes the timing of carrier detection and the timing for loss of carrier detect. The time for carrier detection is about 3ms and the time for loss of signal carrier Detect cdt) is about 14ms.

Table 35

Modes	Timings for Loss (ms)	Timing for Detection (ms)
V.17 14400bps	13.1	2.3
V.17 1200bps	11.7	2.3
V.17 9600bps	12	2.3
V.17 7200bps	12.2	2.2
V.29 9600bps	13.3	2.5
V.29 7200bps	12.3	2.1
V.29 4800bps	12.7	2.5
V.27 4800bps	13.7	2.7
V.27 2400bps	13.3	3.6
Bell 103	19.5	5
V.21	19.1	5

VII.4 - PSTN/Leased Line Selection

The ST75C52/520 can be used both over PSTN network and over leased line (2 wire).

The choice is made with bit 5 (CONF_PSTN) of the first parameter of the CONF command.

CONF_PSTN = 0 will select PSTN network
CONF_PSTN =1 will select leased line.

The nominal carrier detect thresholds for such networks are :
- -33/-38dBm for leased line
- -43/-48dBm for PSTN.

VII.5 - Constellation

For all the high speed FAX modulations the user can observe the constellation with an oscilloscope using the EYEX and EYEY signals. This feature is always available (no validation required).

VIII - ELECTRICAL SCHEMATICS

VIII.1 - First Hybrid Example

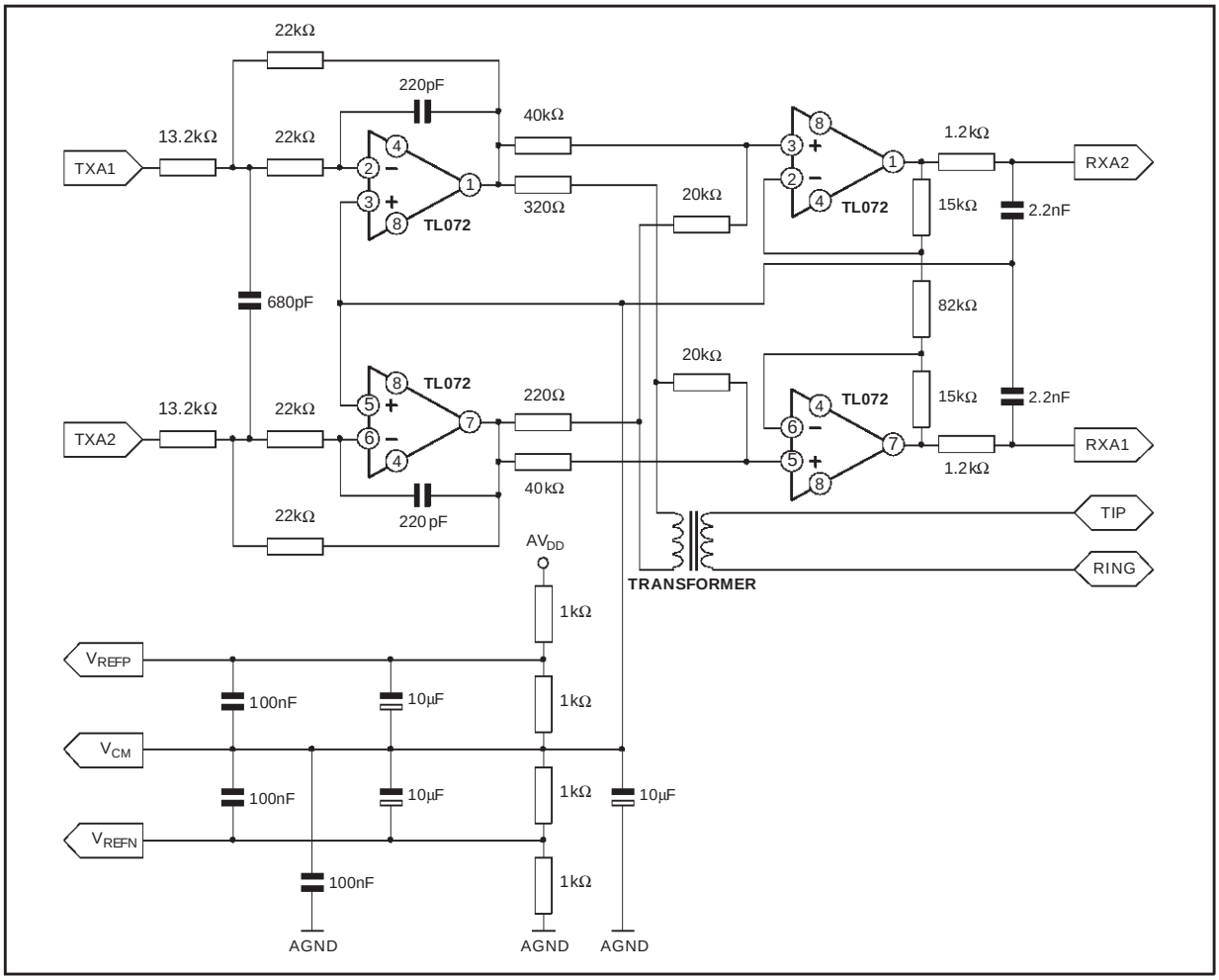
The example is detailed on the following schematic. It is the hybrid used on the application boards of SGS-THOMSON. All the tests were done with this hybrid. With such a solution (differential output and input) and with a double power for the operational amplifier the user can have the ST75C52/520's maximum performances.

The transmit gain is tuned to send carrier at - 9dBm (default value). If the user wants to be able to send carrier signal at 0dBm the transmit gain must be increased. We recommand the following procedure :

- Replace the two 13.2kΩ 1% with two 4.64kΩ 1%.
- Replace the two 220pF with two 47pF.
- use **SETGN** command to decrease the level around -9dBm.

If user wants to use +5V and -5V instead +12V and -12V we recommand to use Rail to Rail operational amplifier to avoid distortion.

Figure 59



VIII.2 - Second Hybrid Example

The following schematic is an example of a cheaper hybrid solution. The main difference is that the reception does not use the differential possibility of the ST75C52/520. The received signal is connected on RXA1 and RXA2 is tied to V_{CM}. The signal at RXA1 must not be higher than 2.5V. The receive gain must be tuned to detect carrier at -43dBm and we suggest to limit the maximum level at -9dBm.

Tuning :
- adjust the return loss,
- ajust the transmit gain,
- adjust the receive gain,
- adjust the duplexor.

Return loss : adjust R0 and C0 to meet the technical requirements in your country which imposes the reference impedance (600Ω or complex impedance), and the different parameters such DC voltage and DC current on the line.

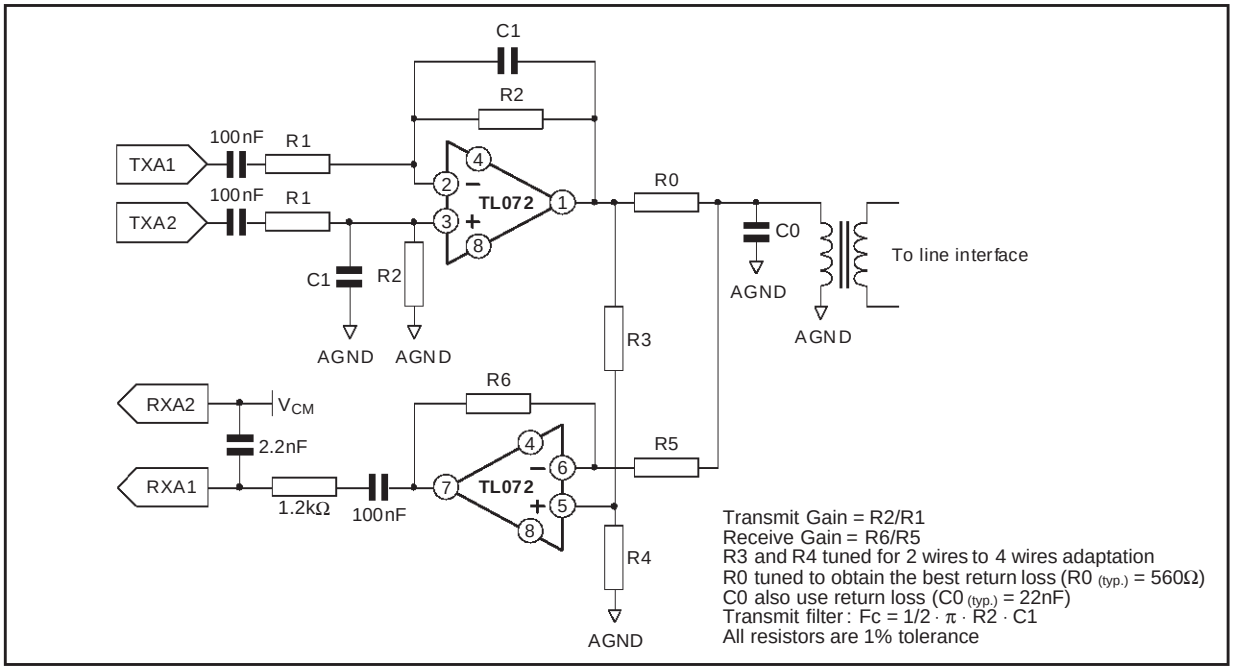
Transmit gain : we recommand the following procedure.
- Keep the **SETGN** default value (7FFF)
- adjust the transmit gain (R2 and R1) and the transmit filter (C1) to have 0dBm and Fc at 19.6kHz.
- adjust **SETGN** to obtain -9dBm (default value for carrier) and -4.5dBm (default value for the DTMF). **STEGN** may be different for carrier and DTMF.

Receive gain : adjust R6 and R5 to detect carrier around -44dBm.

Duplexor : adjust R3 and R4 to remove unwanted carrier when in ful duplex mode.

Hybrid implementation for differential output and single input (operational amplifiers use +12V and -12V) (see Figure 60).

Figure 60



IX - PCB DESIGN GUIDE

IX.1 - DAA

The DAA has both digital and analog portions in which we need to have sufficient dielectrique isolation from the telephone line and to suppress EMI.

Different technical requirements (FCC in USA, EN41003 in Europa...) influence the PCB design. In all cases the PCB layout must keep the insulation given by the components (i.e the distance between input and output for an optocoupler usally used for RING detection, between primary side and secondary side of the line transformer...). We suggest to have a visible dielectric barrier of 4mm (minimum value).

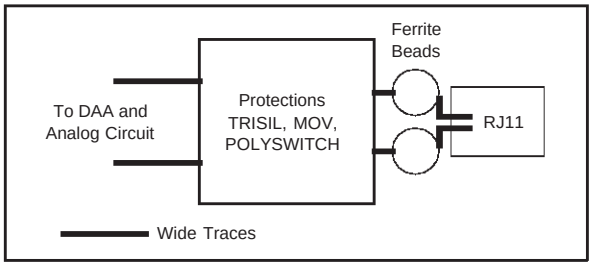
The layout may have wide traces in all the DAA part to avoid problems due to surge tests and to carrie eventualy high DC current.

We suggest to use polyswitch (fuse with auto rearmament) instead of narrow traces to implement fusible mechanism. The polyswitch must be associated with a TRISIL
(such TPA 220 of SGS-THOMSON).

Both transmit carrier (analog signal at - 9dBm) and receive signal (that can be as low as -48dBm) carry all the information through the analog circuit and the DAA. These two parts must be located as close as possible to the RJ-11 telephone jack.

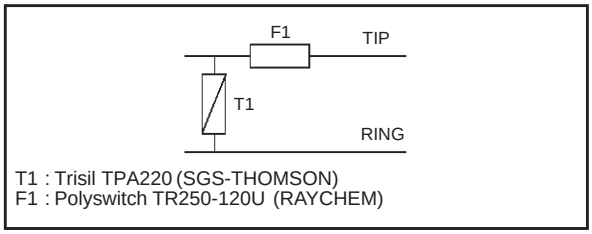
All the protections (surge limiter, MOV or TRISIL) and ferrite beads must be installed just near the RJ-11 telephone jack.

Figure 61



We suggest to use the following protection which meet EN41003 technical requirements :

Figure 62



IX.2 - Digital Circuit

The Hook-control, Pulse-control, Ring-detection, DC current line detection (optional), ST75C52/520 Dual Port Ram Interface, microcontroller, memory and DTE interface are installed in the digital part of the PCB.

The equipment will use frequencies such as 29.412MHz (for the ST75C52/520) and other high frequencies for the microcontroller and different peripherals. For such reasons the digital power (V_{DD}) and the digital ground (DGND) must be separated from the analog power (AV_{DD}) and the analog ground (AGND). We suggest to have a four layers PCB with one layer for the V_{DD} and one layer for the DGND.

It is recommanded to install a bead just at the output of each voltage regulator.

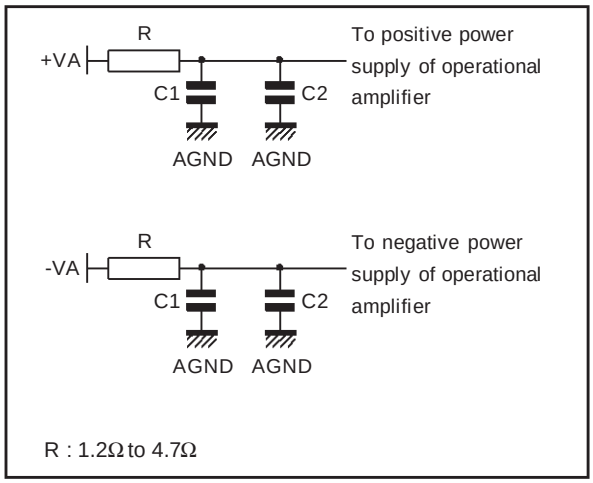
All the components must have a 100nF capacitor between V_{DD} and DGND. Some component (such microcontroller, MODEM/FAX...) required other capacitors usally higher than 1µF. All the capacitors must be connected with the shortest distance from the powers pins.

IX.3 - Analog Circuit

The hybrid, the analog interface of the ST75C52/520 and the transformer line interface only carry analog signals. The power (AV_{DD}) of the ST75C52/520 must be connected to the V_{DD} Pin of the ST75C52/520. The analog ground (AGND) must be connected to the digital point with a very low impedance, at one point and as close as possible to the ST75C52/520.

The Hybrid interface uses one positive power supply and one negative power supply. Simple filters (resistors and capacitors) can be used for each power signal.

Figure 63

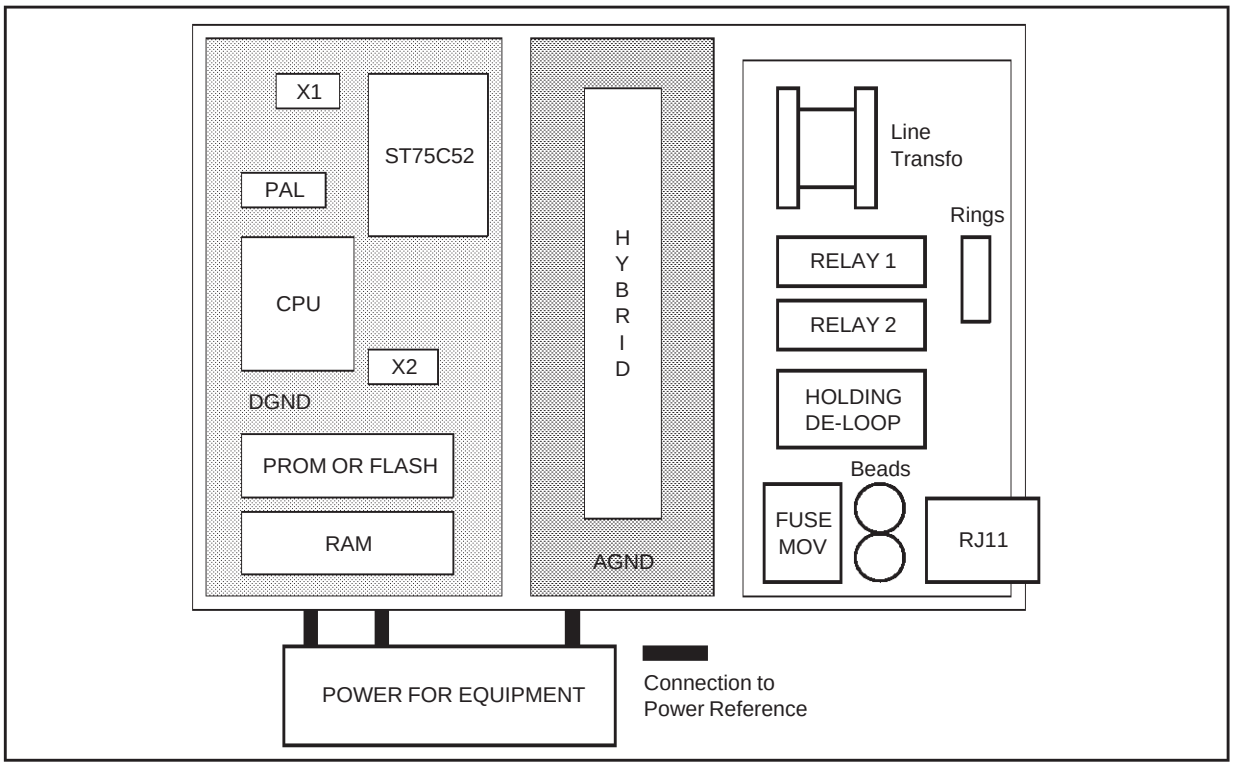


We recommand the following points :

- the V_{CM} reference must be generated as close as possible to the ST75C52/520,
- the two 2.2nF capacitors connected to the RXA1 and RXA2 Pins must be as close as possible to them,
- the two 100nF capacitors connected to the V_{REFP} and V_{REFN} Pins must be as close as possible to them.
- the ground for loudspeaker circuit must be separated from all the other analog modem circuit. In fact due to the audio current during the handshake the receive signal could be affected.
- use wide traces for all the power signals.

The analog ground could be a part of the ground layer, but the connection between the two references must be done only at one point. When possible the analog ground will be connected directly to the reference of the power equipment without going through the digital ground layer as shown on the Figure 64.

Figure 64



X - ST75C52/520 VARIABLES DESCRIPTION

Introduction

This chapter describes the most interesting variables that can be read or modified by the user. In order to read a variable a **MR** command (or **CR** for complex read) must be issued, and the answer is available in the Dual Ram, in the **COMREP** and **COMREP+1** locations. In order to overwrite a variable a **MW** command must be issued.

The address, characteristic (R = read, W = write, R/W = read or write), and function of key data pump variables is listed below by basic modem functional block. All numbers starting with a $ are Hexadecimal numbers, % are binary numbers.

Some of the variables and the explanations were some times introduced in above chapters.

Timing Recovery

FRQOFFT (R) Receive clock frequency offset.

PSITHRSH (R) 0.7 Deg timing phase adjustement threshold for timing signal dpll. The local-to-remote modem timing offset for all modes except V.21 channel 2 can be calculated using the following formula :

$$TOffset = \frac{FRQOFFT}{PSITHRSH} \cdot \frac{0.7}{360}$$

FRQ (R) V.21 ch. 2 receive clock frequency offset. V.21 channel 2 has a wider range of timing offset tracking permitting ±0.3% and it can be calculated using the following formula :

$$TOffset = \frac{FRQ}{32767} \cdot \frac{1.4}{360}$$

PLLcount (R/W) a counter which is decremented every baud in the timing recovery routine and, when > 0 selects wide bandwidth timing recovery DPLL. When = 0 selects narrow bandwidth timing recovery DPLL. For short train applications, it is useful to write PLLcount = 4800 (around 2s) after sending the SYNC 1 command to have a good success rate for many successive short train sequences, especially when there is a large timing offset.

Carrier Recovery

FRQOFF (R) Receive carrier frequency offset :

Offset = FRQOFF x 0.0366

in Hz. Typically, FRQOFF = $1B(27) for 1Hz.

Equalizer, AGC

_RX_STA (R/W) Equalizer and AGC can be frozen independently or simultaneously.

- Bit 0 : Freeze Equalizer (the Equalizer is frosen if this bit is 1).
- Bit 2 : Freeze AGC (the AGC is frosen if this bit is 1).

_RX_STA must be modified in data mode and the other bits must be unchanged. Read the value and change only the corresponding bits in the _RX_STA word.

_AGCSCA (R) Automatic gain control level for receive signal varies from $80 (0dBm) to $7FFF (-48dBm) according to the following table :

Table 36

Value	RXLVL (dBm)
$0080	0
$0100	- 6
$0200	- 12
$0400	- 18
$0800	- 24
$1000	- 30
$2000	- 36
$4000	- 42
$7FFF	- 48

The level calculated above must be corrected by 0 or -12dB to indicate the real receive analog level on the line. (See _GAINSTA below). The exact formula is :

RxLevel = (-20 x log(value)) + 46 - 6 x (_GAINSTA)

_GAINSTA (R) This variable tells whether the 12dB analog gain between input RXA and the analog to digital converter output has been activated. This gain enables a receive dynamic range between 0 and -50dBm. In the case that it has been activated, it has the value 2, otherwise 0.

_GAINCTL (R/W) This variable contains the following information :

- bit 0: FRZGAIN,
- bit 1: FORCE0,
- bit 2: FORCE12,
- all other bits are 0.

The user has the possibility of forcing 12dB, 0dB, or freezing the analog input gain. If desired, this word is programmed before sending the CONF

command and is effective after its execution. The variable _GAINCTL is initialized to 0 after a hardware reset or issuing of the init command, and if not programmed by the user, will allow the analog gain to be automatically enabled or disabled via the DSP software according to the actual input level. A built-in hysteresis avoids glitches on the receive digital samples. The input gain is switched to 0dB if the input analog instantaneous level exceeds -12dBm and to 12dB if the instantanenous level never exceeds -30dBm for 8ms. The FRZGAIN bit in _GAINCTL will be automatically set following the detection of phase reversals in the synchronization sequence for V.17, V.29, V.27 reception modes. This insures reliable demodulation for the receiver and, during a particular connection, the receive attenuation will not appreciably change.

RDQUA (R) Equalizer error energy gives an idea of signal to noise ratio seen by the receiver. The square of the equalizer error is updated once per baud (2400Hz for V.17, V.33, V.29, 1600Hz for V.27 4800bps, 1200Hz for V.27 2400bps) with a low pass 1st order IIR digital filter with a pole radius of 0.96875. This implies a time constant of around 80ms.

RDQUA has the following typical values :

Table 37

Value	RX SNR
$00C0	30dB
$0180	27dB
$0300	24dB
$0600	21dB
$0C00	18dB
$1800	15dB
$3000	12dB

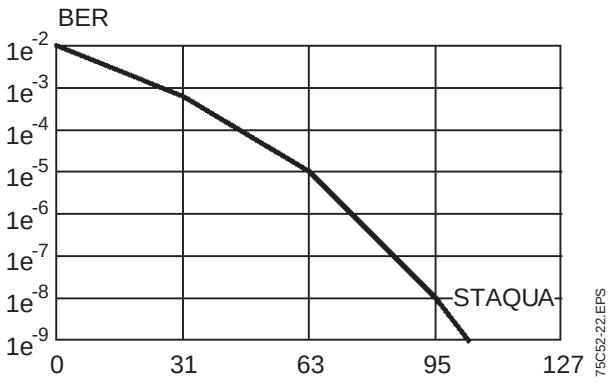
_RDQUA (R) A 16-bit number ranging between 0 and 127 indicating the receive quality (also available in 8-bit status word byte 2, STAQUA in dual port ram). The following formula is implemented in DSP software :

$$\_RDQUA = 127 - SCAQUA \times RDQUA$$

and is limited between 0 and 127. A value of 127 indicates a very good receive signal quality while 0 indicates a very poor signal quality. The coefficient SCAQUA is mode dependent and was chosen to give a value for _RDQUA of 63 when the receive SNR is such that the expected bit error rate is 10^{-5}, that is, 1 error for every 100000 bits received.

Refer to the following charts for expected values of _RDQUA, BER on flat telephone line.

Figure 65



SCAQUA (R/W) The coefficient for calculating _RDQUA above is automatically programmed according to the mode specified in the conf command and it is possible to overwrite its value at the end of the synchronization sequence if the user desires a different value for the quality indication. Generally, reducing the value read by 1/2 will imply that an _RDQUA value of 31 will correspond with a 10-5 BER and doubling the value will imply that an _RDQUA value of 127 will correspond with a 10-5 BER in the above tables.

_SUCTH (R/W) A threshold value for _RDQUA for determining the programming of pnsucs bit in _SHSK word described below. The default value is programmed to 64 at the execution of a conf command can be modified thereafter (espacially for short train applications).

_RDCPT (R) Output of Demodulator. Complex number, can be use to display the received eye pattern on a console or print-out. The user must perform a CR (complex read) command to insure reading of the real and imaginary parts of the signal during the same baud.

EQFRK0E (R/W) 32 Complex even equalizer coefficients.
EQFRK1E (R/W) 32 Complex odd equalizer coefficients.

Handshake, Synchronization

_SHSK (R) Contains information about the progress of the handshake or synchronization in all fax modes. This variable is also avalilable in optional status word 2 STAOPT2 in the dual port ram. The handshake bit positions are programmed on the 8 lsb of _SHSK and are defined below :

While Transmiting :

P1s = %00000001 generate echo protection tone
P2s = %00000010 generate phase reversals
PNs = %00000100 generate training sequence
PRs = %00001000 generate rate sequence
SCR1s = %00010000 generate scrambled one's

While Receiving :

P2s = %00000010 detect phase reversals
PNDETs = %00100000 detect training sequence (latched)
PNs = %00000100 detect training sequence
PRDETs = %01000000 detect rate sequence (latched)
PNSUCs = %10000000 detect scrambled one's (latched)
SCR1s = %00010000 detect scrambled one's note that PRs and PRDET are only valid in V.17 and V.33 Modes.

_TSPEED (R) Target speed initialized by CONF command.

%0000000000000011 = 2400bps
%0000000000000100 = 4800bps
%0000000000000101 = 7200bps
%0000000000000110 = 9600bps
%0000000000000111 = 1200bps
%0000000000001000 = 14400bps

_SPEED (R) Negotiated speed after synchronization May differ from _TSPEED for V.33 mode and has the same format as _TSPEED.

Carrier Detect

DETHF (R/W) Fast detection threshold
DETH (R/W) Slow detection threshold
LOSSTH (R/W) Slow loss threshold
LOSSTHF (R/W) Fast loss threshold

The carrier detect is displayed on status byte 0, bit 0 as well as on the **CD** Pin of the ST75C52/520 V.24 interface and is active at the end of the synchronization sequence for V.17, V.29, V.27, V.21 ch2 provided the detection threshold has been reached. For fsk modes, it is active provided the threshold has been reached. The carrier detect algorithms, 2 signal level integrators a fast integrator for quick detection with a limited precision and a slow integrator for enhanced precision. There are four thresholds programmed with default values for each of the modes V.33, V.17, FSK, V.29 and V.27 which can be modified by the user after the conf command. Typical values for V.17 are shown below as an example and doubling the value read will increase the threshold by approximately 6dB :

(-40dBm) $167 DETHF (fast detection threshold)
(-44dBm) $140 DETH (slow detectiion threshold)
(-47dBm) $D0 LOSSTH (slow loss threshold)
(-51dBm) $A0 LOSSTHF (fast loss threshold)

note that it is mandatory to have :
DETHF > DETH > LOSSTH > LOSSTHF

AVGLVL1 (R) Carrier detect level. This level is the ouput of the slow level integrator with a 200ms time constant and is automatically corrected for the possible 12dB analog gain explained above. The formula for the rx lvl on the line for a V.17 receive signal, for example, is a function of x, the value of the variable at address AVGLVL1 :

RXLEVEL = 20 x log(x) - 93 in dBm.

_FASTLVL (R) Fast carrier detect level. This level is the output of the fast level integrator calculated with a 10ms time constant and obeying the same formula as above with, of course, more ripple for a given level due to the smaller time constant.

_LVLSAV (R/W) Storage of value of (_FASTLVL/2) described above and memorized during the detection of P2 portion of sync sequence by the receiver. This is the threshold for the fast carrier detect comparator. Memorizing the level on a valid signal avoids false detection or non-detection due to noise thus providing a very accurate indication of presence of a carrier. It updates bit 7 of status byte 0 in the dual port ram. Its value can eventually be changed by the user by first reading and then writing into this memory location after p2s bit is activated in the optional status word 2.

V21FDET (R) Detection of presence of V.21 flag also available in status word 1 bit 6 (STA_FLAG). The detector signals presence of 2 or more consecutive sequences of $7E (%01111110) modulated according to the V.21 ch. 2 FSK specification (1 = 1850Hz, 0 = 1650Hz) at 300bps. The detector signals the loss of V.21 flag at the end of the first following erroneous bit and is automatically re-armed. The detector is always active during tone, dtmf, audio or V.21 channel 2 conf modes. It is active in V.17, V.33, V.29, V.27 Conf modes after the SYNC 1 command is issued and before the data mode (carrier detect active).

Tone Detector Programming

LEVOUT (R/W) 16 Programmable static levels.

BIQCOEF (R/W) 16*2*6 Biquad coeficients.

Coefficient order for each of 16 4th order cells :
C0, C1, C2, C3, C4, C5, C6, C7, C8, C9, CA, CB

Where each 4th order cell has the following transfer function :

$$\frac{OUT}{IN} = C_0 \cdot \frac{C_5 + 2 \cdot C_3 \cdot z^{-1} + 2 \cdot C_4 \cdot z^{-2}}{1 - 2 \cdot C_1 \cdot z^{-1} - 2 \cdot C_2 \cdot z^{-2}} \; C_6 \cdot \frac{C_B + 2 \cdot C_9 \cdot z^{-1} + 2 \cdot C_A \cdot z^{-2}}{1 - 2 \cdot C_7 \cdot z^{-1} - 2 \cdot C_8 \cdot z^{-2}}$$

When programming the coefficients, care must be taken to avoid overflow of internal nodes. Effectively, the structure of each 2nd order section is such that the recursive portion is executed before the non-recursive. Therefore, C0 and C6 must be chosen to insure that the maximum of :

$$C_0 \cdot \frac{1}{1 - 2 \cdot C_1 \cdot z^{-1} - 2 \cdot C_2 \cdot z^{-2}} \quad \text{or} \quad C_6 \cdot \frac{1}{1 - 2 \cdot C_7 \cdot z^{-1} - 2 \cdot C_8 \cdot z^{-2}}$$

never exceeds 1 ($7fff) or -1 ($8000)

POWCOEF (R/W) 16 Power coeficients p1, Power estimator using absolute value of the input signal :

$$\frac{OUT}{IN} = P1 \cdot \frac{z^{-1}}{1 - (1 - P1) \cdot z^{-1}}$$

BPWIRE (R/W) 16 Biquad and pwr estimator input wiring addresses
FORMAT = [4TH ORDER BIQ(MSB), PWR(LSB)]

CPWIRE (R/W) 16 Comparator input wiring addresses
FORMAT = [COMPARATOR+(MSB), COMPARATOR-(LSB)]

The wiring addresses furnished in bpwire, cpwire are from the following possible sources :

GND	$00
Rx signal	$01
Rx signal*2	$02
Rx signal*4	$03
4th order biquad output	$10 to $1F
Power output	$20 to $2F
Static levels	$30 to $3F

Notes : 1. A value of $276 on RX signal corresponds to a real signal level on the line of -25dBm. For example, suppose one wants to detect a certain RXLVL on the line via RX SIGNAL assuming a gain of 1.0 in the biquadratic filter. The value of Levout, the comparison threshold, can be calculated : Levout = 10[(RXVL+81)/20]

2. The 0 or 12dB analog gain is automatically compensated for at the power outputs and need not be accounted for in the above formula. Some modifications to the calculated value may be needed for low detection levels near -50dBm, or the RX SIGNAL*2 input may be used.

_NTDCELL (R/W) Number of tone detector cells active (0-15). The default values for _NTDCELL are according with the following Phases : see Figure 66 and Table 38.

The user can modify _NTDCELL on-the-fly but must be careful to avoid real time kernel errors (ERR_RTK) in the SYSERR status byte. The execution time of each cell is roughly 200 machine cycles. For example, if the HDLC is not used, 400 additional machine cycles could be available for additional cells.

_TONEDET (R) Outputs of tone detectors. The low byte of _TONEDET contains the outputs of tone detectors cells 0 to 7. The low byte of _TONEDET+1 contains outputs of cells 8 to 15. When the corresponding bit is "1" the signal at the positive input of the comparator is higher that at the negative input. Only _NTDCELL bits are valid at any one time and the others are 0.

_RING (R) Output of the RING Detector.This word is identiqual to the STAOP2 byte when in Tone mode (neither DTMF receiver neither Modem mode). The content of that word is the duration of the RING Period.

The formula to compute the RING Frequency - in Hz) is :

$$RING\_Frequency = \frac{1}{RING \cdot 2400}$$

This value is updated at each falling edge of the RING Signal. Refer to the following diagram for the phase relation between the STA_RING and the RING Signal (see Figure 67).

General Purpose

_TXGAIN (R/W) Transmit gain. Any signal to transmit is multyplied by this number. This is the value modified by **SETGN** command.

_FSKSYNC (R/W) $FFFF, for V.21 ch2 and 0 for all other modes. The user must use the memory write command to write 0 to this variable when passing from V.21 ch2 to FAX modes just before sending the corresponding **CONF** command.

Figure 66

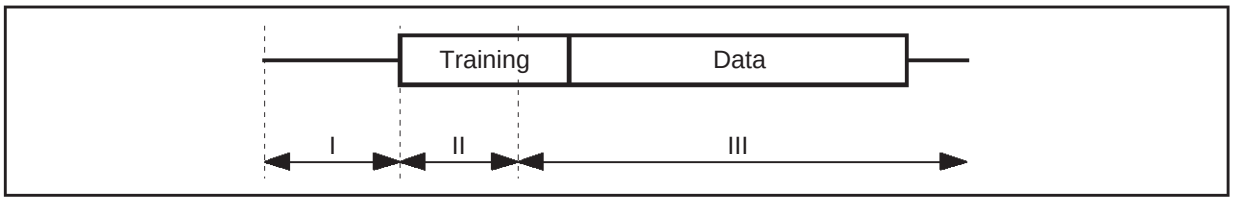
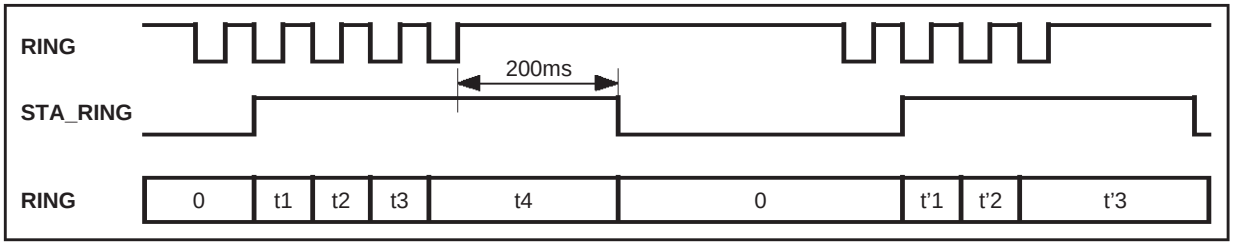


Table 38

Mode/Phase	Config.	Phase I	Phase II	Phase III
Tone, DTM (1), Voice	16 (2)	-	-	-
FSK Full Duplex	-	4	4	4
V.21 Ch 2 Tx	-	16 (2)	8 (2)	8 (2)
V.21 Ch 2 Rx	-	4 (2)	4 (2)	4
V.17/V.33/V.29/V.27 Tx	-	8	8	8
V.17/V.33/V.29/V.27 Rx	-	8 (2)	2 (2)	2

Notes : 1. The DTMF Receiver uses 12 of the 16 cells.
2. The V.21 Flag detector is active.

Figure 67



Tone Generator

_TGNFLG (R/W) Tone generator flag. Each of the four low bits of this variable define if the corresponding tone generator is enabled. This is the value modified by a **TGEN** and **TONE** command.

_TGNBLK (R/W) For each of the four tone generators (i) contains :

_TGNBLK+(3*i) : Frequency of tone (freq*32767/4800).
_TGNBLK+1+(3*i) : Instantanous phase (0 to 65535).
_TGNBLK+2+(3*i) : Amplitude ($7FFF refers to maximum signal).

Address Equivalences for Version 1.0 and 1.1 (DSP software version)

Timing Recovery	
FRQOFFT	$15D9
PSITHRSH	$15E3
FRQ	$1777
PLLCOUNT	$15DF
Carrier Recovery	
FRQOFF	$15F1
Equalizer, AGC	
_RX_STA	$1015
_AGCSCA	$10CF
_GAINSTA	$17D3
_GAINCTL	$17D2
RDQUA	$11DD
_RDQUA	$1054
SCAQUA	$11DC
_SUCTH	$17DD
_RDCPT	$1044
EQFRKOE	$1438
EQFRK1E	$1478
Handshake, Synchronisation	
_SHSK	$10F1
_TSPEED	$10E5
_SPEED	$1012
Carrier Detect	
DETHF	$16C2
DETH	$16C1
LOSSTH	$16C4
LOSSTHF	$16C3
AVGLVL1	$16BF
_FASTLVL	$172B
_LVLSAV	$16DF
V21FDET	$17B8
Tone Detector Programming	
LEVOUT	$122A
BIQCOEF	$12BA
POWCOEF	$137A
BPWIRE	$129A
CPWIRE	$12AA
_NTDCELL	$1006
_TONEDET	$1007
_RING	$1554
General Purpose	
_TXGAIN	$1001
_FSKSYNC	$16E8
Tone Generator	
_TGNFLG	$1002
_TG0PHC	$1003
_TGNBLK	$11EC

XI - PERFORMANCES

The curves hereafter define performances under various line conditions. All tests were run half duplex with a ST75C52/520 REV 1.0 as reference modem. The tests are run under the following conditions.

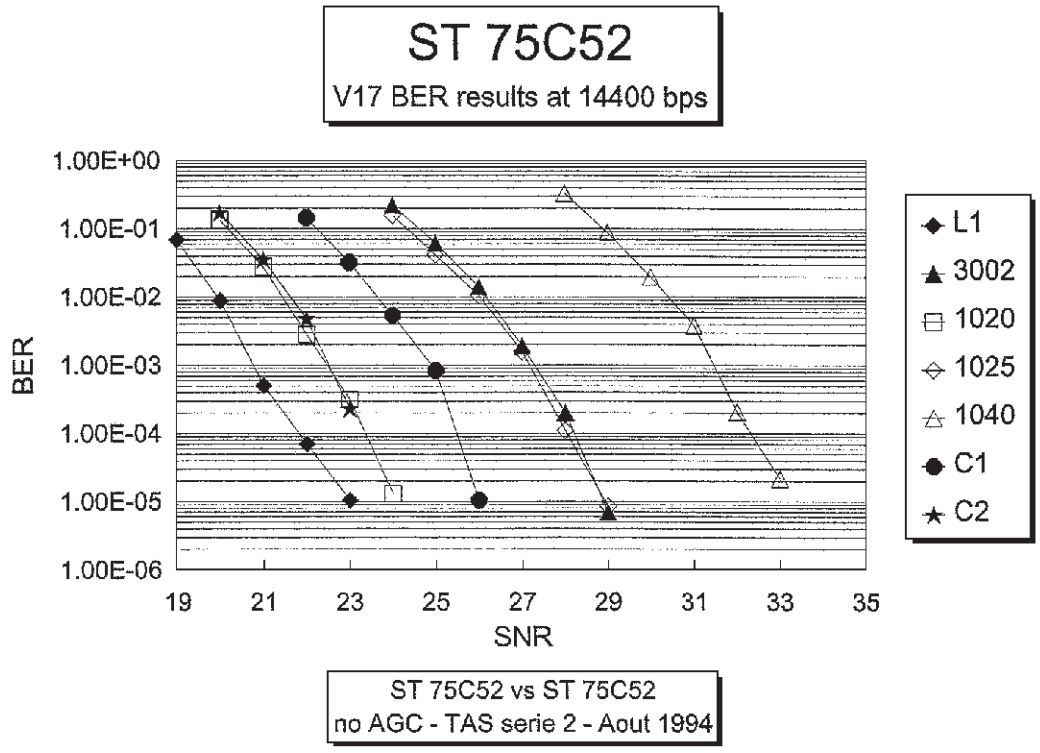
US LINES (type of channel) :
- Flat line ; US lines 3002, C1,C2
- Rx level : -25dBm
- Tx level : - 9dBm
- No AGC

EUROPEAN LINES (type of channel) :
- 1040, 1020 and 1025
- Rx level : -25dBm
- Tx level : - 9dBm
- No AGC

JAPANESE LINES (type of channel) :
- JPN1, JPN2, JPN3, JPN4, JPN5, JPN6, JPN7
- Rx level : -25dBm
- Tx level : - 9dBm
- AGC V56 (rms)

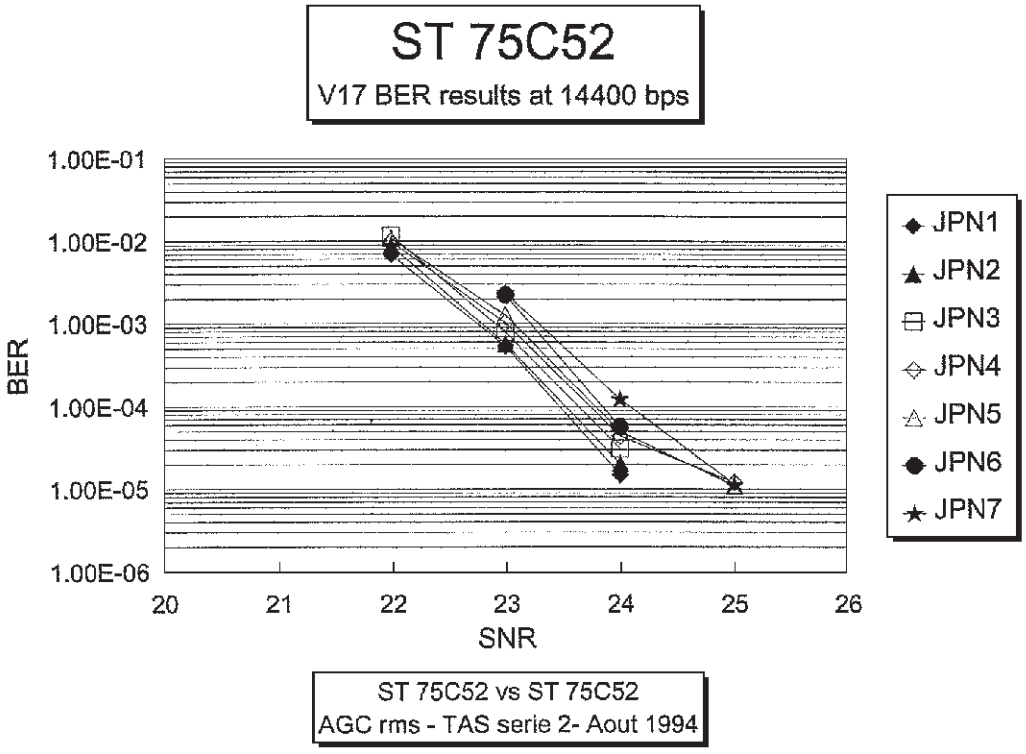
Figures 68 to 71 show performances of fax modes on all lines above in V.17 14400 and in V.29 9600.

Figure 68 : V.17 14400bps BER versus SNR on European and US Lines



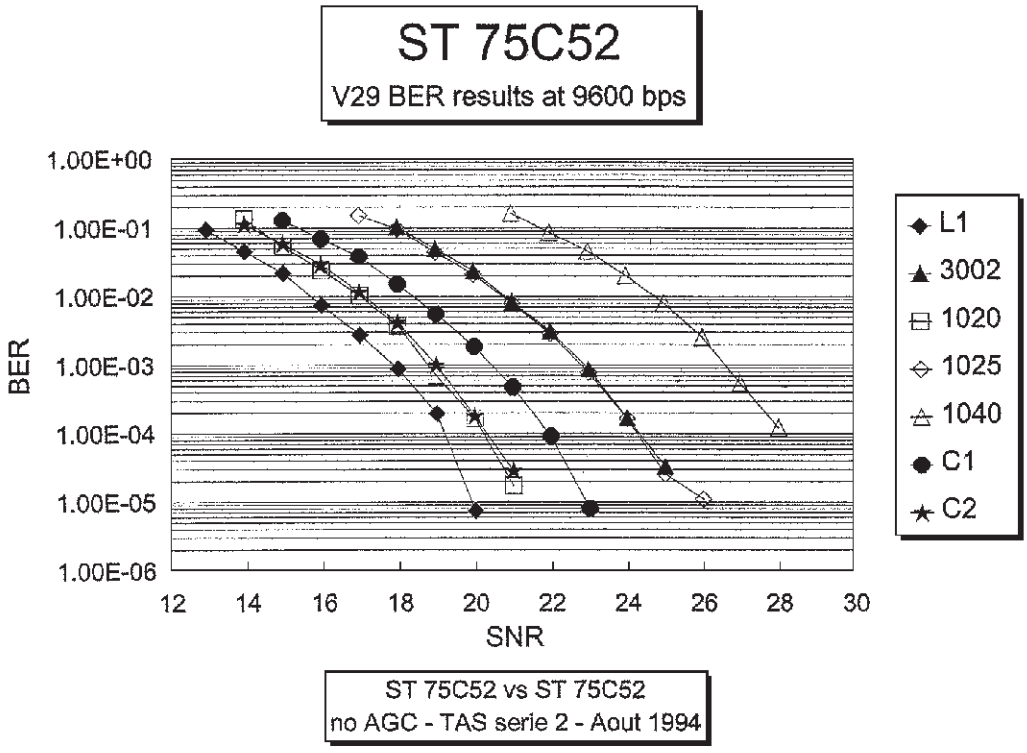
75C52-89.TIF

Figure 69 : V.17 14400bps BER versus SNR on Japanese Lines



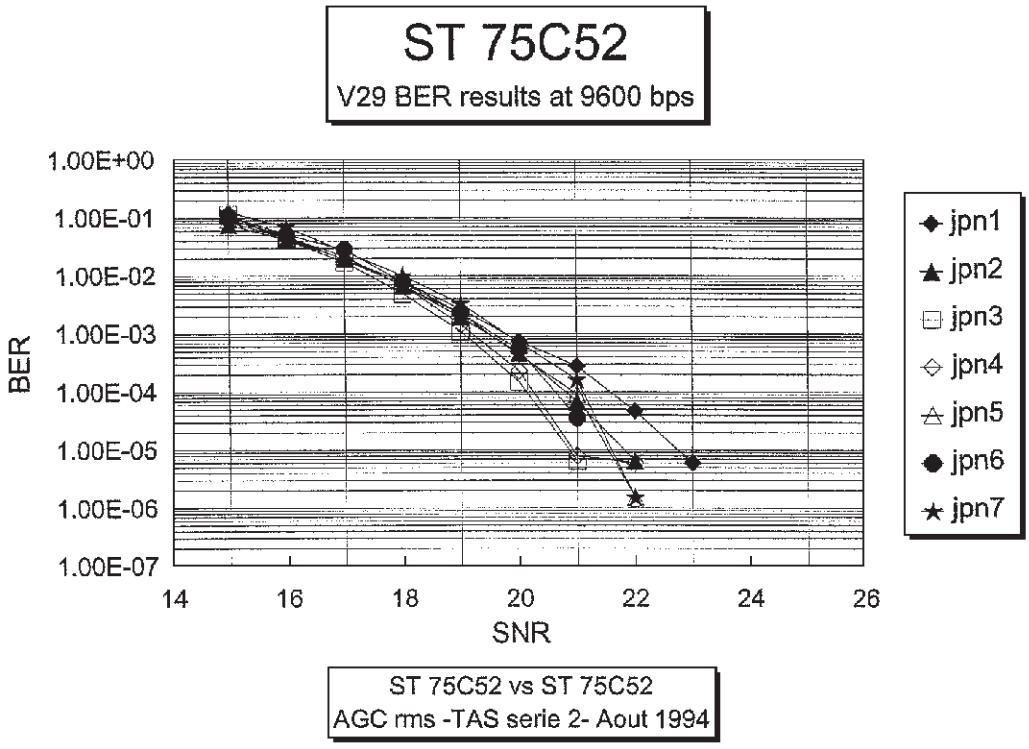
75C52-90.TIF

Figure 70 : V29 9600bps BER Results versus SNR on European and US Lines



75C52-91.TIF

Figure 71 : V29 9600bps BER Results versus SNR on Japanese Lines



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