

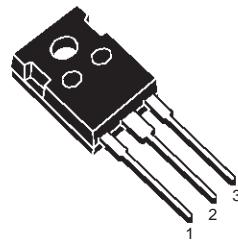
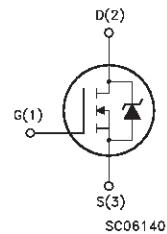
**N - CHANNEL ENHANCEMENT MODE
POWER MOS TRANSISTOR**

TYPE	V _{DSS}	R _{DS(on)}	I _D
STW50N10	100 V	< 0.035 Ω	50 A

- TYPICAL R_{DS(on)} = 0.027 Ω
- AVALANCHE RUGGED TECHNOLOGY
- 100% AVALANCHE TESTED
- REPETITIVE AVALANCHE DATA AT 100°C
- HIGH CURRENT CAPABILITY
- 175°C OPERATING TEMPERATURE
- APPLICATION ORIENTED CHARACTERIZATION

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- POWER MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS
- SYNCRONOUS RECTIFICATION


TO-247
INTERNAL SCHEMATIC DIAGRAM


SC06140

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source Voltage (V _{GS} = 0)	100	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	100	V
V _{GS}	Gate-source Voltage	± 20	V
I _D	Drain Current (continuous) at T _c = 25 °C	50	A
I _D	Drain Current (continuous) at T _c = 100 °C	35	A
I _{DM(•)}	Drain Current (pulsed)	200	A
P _{tot}	Total Dissipation at T _c = 25 °C	180	W
	Derating Factor	1.2	W/°C
T _{stg}	Storage Temperature	-65 to 175	°C
T _j	Max. Operating Junction Temperature	175	°C

(•) Pulse width limited by safe operating area

I_{SD} ≤ 60 A, di/dt ≤ 200 A/μs, V_{DD} ≤ V_{(BR)DSS}, T_j ≤ T_{JMAX}

STW50N10

THERMAL DATA

R _{thj-case}	Thermal Resistance Junction-case	Max	0.83	°C/W
R _{thj-amb}	Thermal Resistance Junction-ambient	Max	30	°C/W
R _{thc-sink}	Thermal Resistance Case-sink	Typ	0.1	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		300	°C

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I _{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T _j max, δ < 1%)	50	A
E _{AS}	Single Pulse Avalanche Energy (starting T _j = 25 °C, I _D = I _{AR} , V _{DD} = 25 V)	400	mJ

ELECTRICAL CHARACTERISTICS (T_{case} = 25 °C unless otherwise specified)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 250 μA V _{GS} = 0	100			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = Max Rating V _{DS} = Max Rating T _c = 125 °C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20 V			± 100	nA

ON (*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	2	3	4	V
R _{D(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 25 A		0.027	0.035	Ω
I _{D(on)}	On State Drain Current	V _{DS} > I _{D(on)} × R _{D(on)max} V _{GS} = 10 V	50			A

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (*)	Forward Transconductance	V _{DS} > I _{D(on)} × R _{D(on)max} I _D = 25 A	20	45		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 25 V f = 1 MHz V _{GS} = 0		4100 600 150	5200 800 200	pF pF pF

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Time Rise Time	$V_{DD} = 50 \text{ V}$ $I_D = 25 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$		25 75	35 105	ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 80 \text{ V}$ $I_D = 50 \text{ A}$ $V_{GS} = 10 \text{ V}$		120 20 50	170	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 80 \text{ V}$ $I_D = 50 \text{ A}$ $R_G = 4.7 \Omega$ $V_{GS} = 10 \text{ V}$		30 35 65	45 50 95	ns ns ns

SOURCE DRAIN DIODE

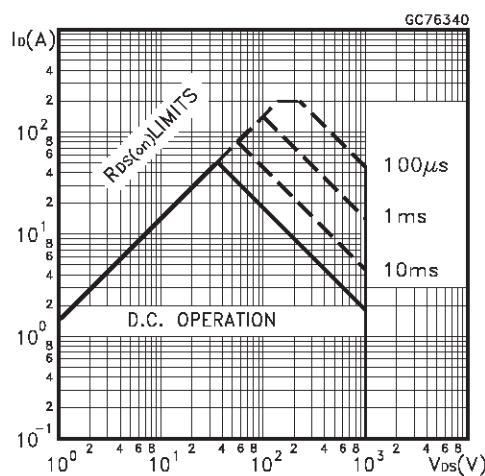
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM}(\bullet)$	Source-drain Current Source-drain Current (pulsed)				50 200	A A
$V_{SD} (\ast)$	Forward On Voltage	$I_{SD} = 50 \text{ A}$ $V_{GS} = 0$			1.5	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 50 \text{ A}$ $di/dt = 100 \text{ A}/\mu\text{s}$			200	ns
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 30 \text{ V}$ $T_j = 150^\circ\text{C}$			1.4	μC
I_{RRM}	Reverse Recovery Current				14	A

(*) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %

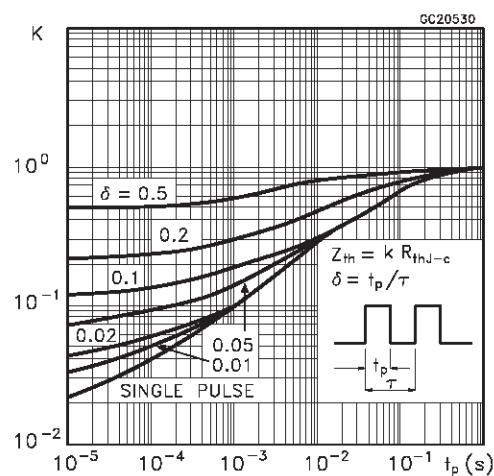
(•) Pulse width limited by safe operating area

(1) $I_{SD} \leq 60 \text{ A}$, $di/dt \leq 200 \text{ A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$

Safe Operating Area

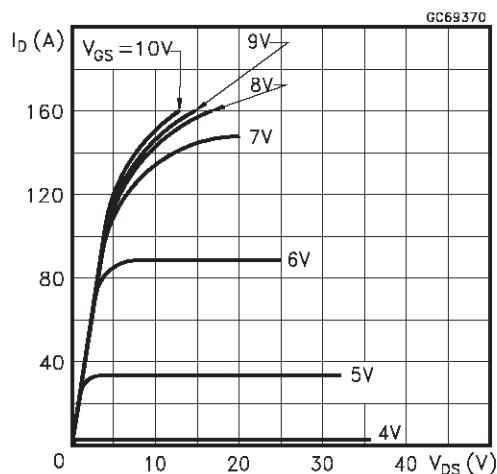


Thermal Impedance

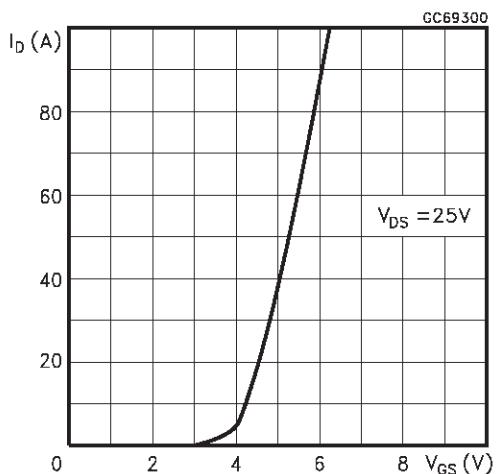


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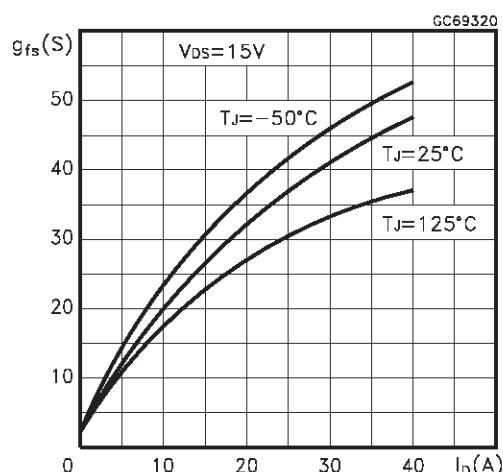
Output Characteristics



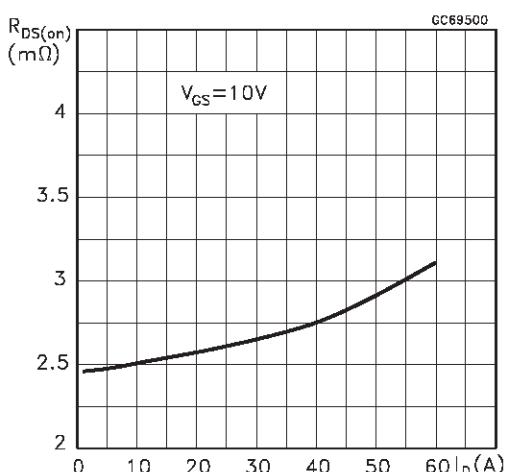
Transfer Characteristics



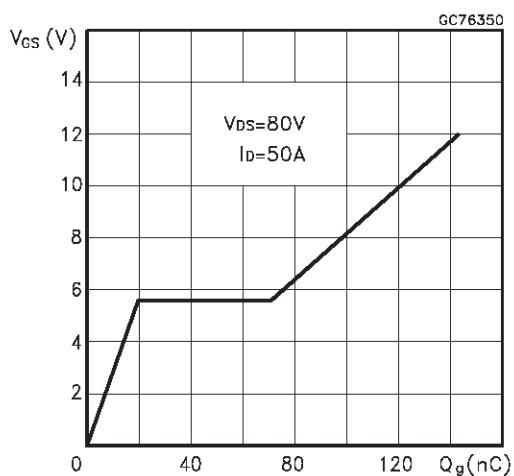
Transconductance



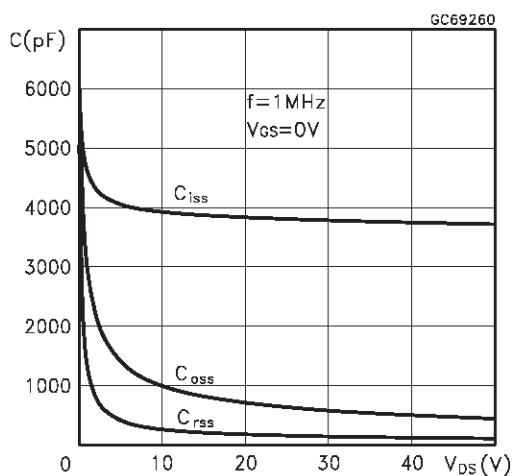
Static Drain-source On Resistance



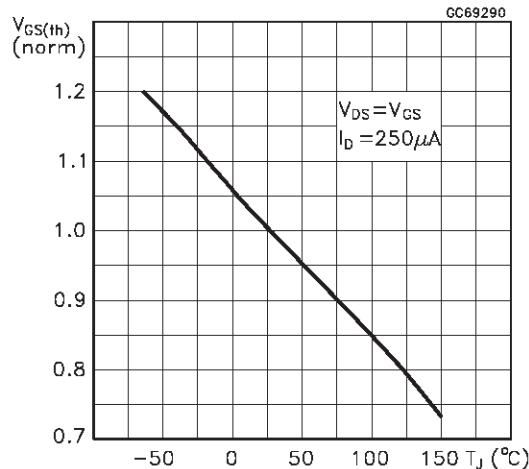
Gate Charge vs Gate-source Voltage



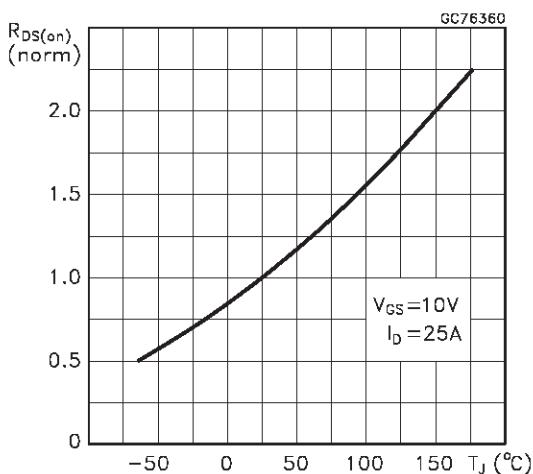
Capacitance Variations



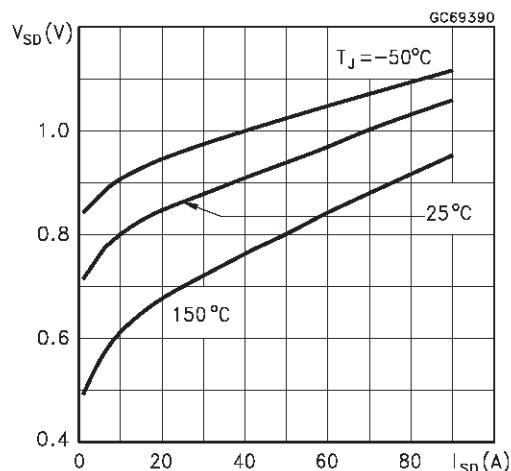
Normalized Gate Threshold Voltage vs Temperature



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics



STW50N10

Fig. 1: Unclamped Inductive Load Test Circuit

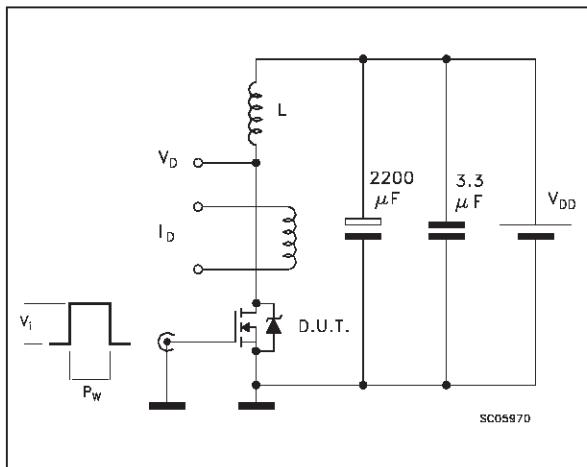


Fig. 2: Unclamped Inductive Waveform

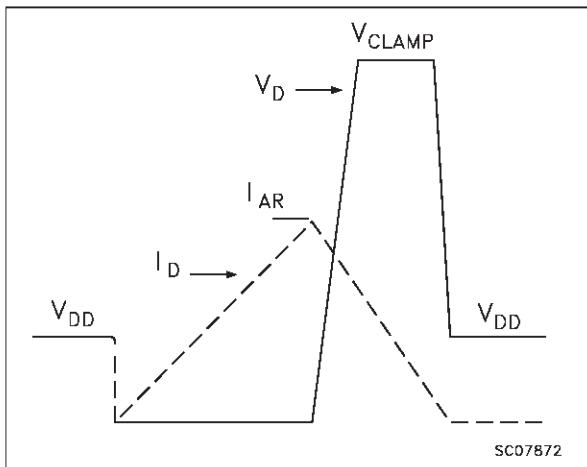


Fig. 3: Switching Times Test Circuits For Resistive Load

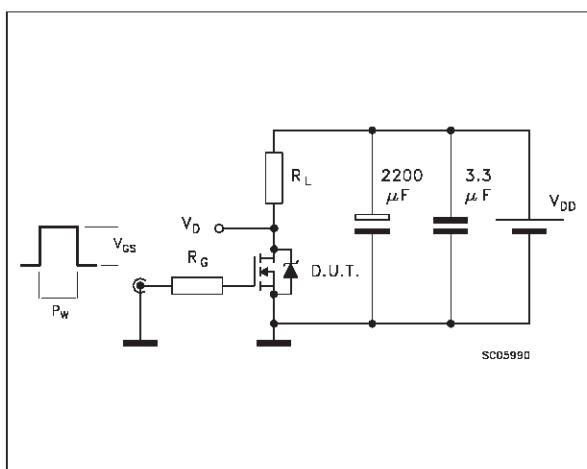


Fig. 4: Gate Charge test Circuit

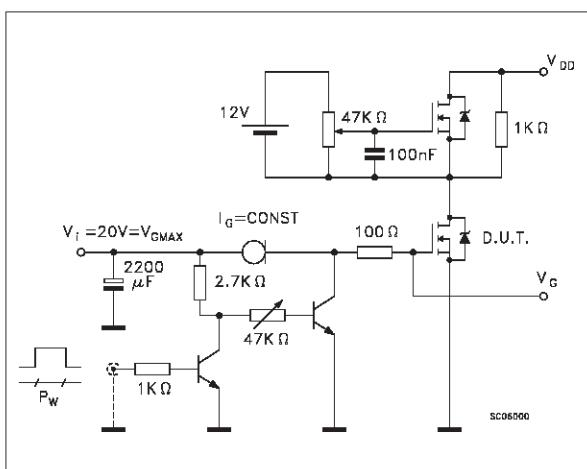
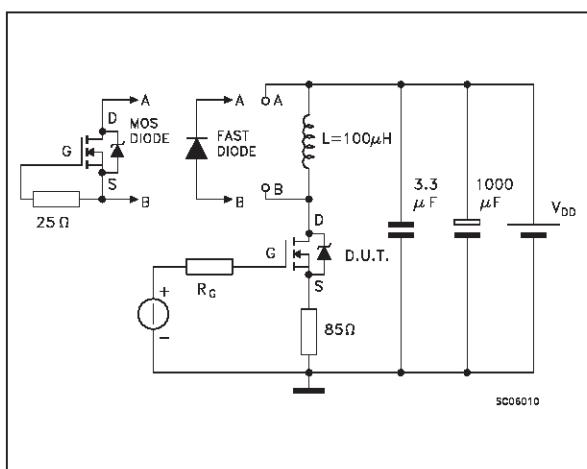
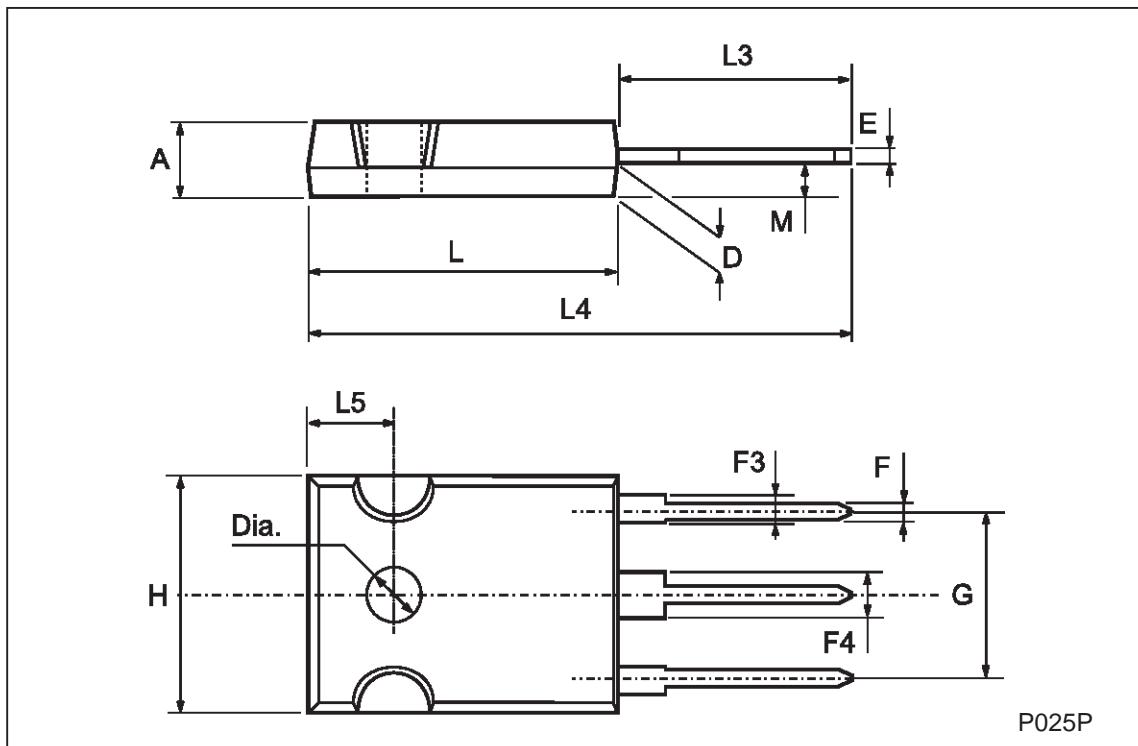


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-247 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.7		5.3	0.185		0.209
D	2.2		2.6	0.087		0.102
E	0.4		0.8	0.016		0.031
F	1		1.4	0.039		0.055
F3	2		2.4	0.079		0.094
F4	3		3.4	0.118		0.134
G		10.9			0.429	
H	15.3		15.9	0.602		0.626
L	19.7		20.3	0.776		0.779
L3	14.2		14.8	0.559	0.413	0.582
L4		34.6			1.362	
L5		5.5			0.217	
M	2		3	0.079		0.118
Dia	3.55		3.65	0.140		0.144



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