SGS-THOMSON MICROELECTRONICS

QUALITY & RELIABILITY REPORT

October 1996 to September 1997 - EPROM, FLASH Memory, EEPROM and SRAM Products

INTRODUCTION

SGS-THOMSON manufactures a wide range of memory types which include:

Non-volatile memories: Flash memory, UV EPROM, OTP EPROM and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; Flash memories in 1.2 to 0.6µ CMOS technology; OTP EPROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Non-volatile RAMS: ZEROPOWER and TIMEKEEPER ranges are manufactured in 1.2-0.8µ HCMOS technology.

Packages for ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from October 1996 to September 1997. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

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Table 1. Final Average Outgoing Quality (AOQ), October 1996 to September 1997

Process	Electrical ppm				Visual ppm			
	3Q97	2Q97	1Q97	4Q96	3Q97	2Q97	1Q97	4Q96
UV EPROM								
CMOS	17	19	17	20	15	12	16	19
NMOS	0	0	0	0	20	0	18	12
OTP EPROM								
CMOS	18	20	19	16	14	6	7	5
FLASH								
CMOS	0	4	17	5	5	4	0	6
SRAM								
CMOS	0	0	0	4	4	4	3	3
EEPROM								
CMOS	1	1	3	5	4	5	9	8

Table 2. Failure Rate Predictions (Fit), October 1996 to September 1997

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C ($\times 10^6$)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs ($\times 10^6$)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -35%	4.99	140	0.6	4.0	1,372	0	0.7	1.7
CMOS E6 - DM	3.40	140	0.6	4.0	933	0	1.0	2.5
NMOS E3	1.45	140	0.6	2.6	188	0	4.8	12
OTP EPROM								
CMOS E5 -35%	2.70	140	0.6	4.0	697	0	1.3	3.3
FLASH								
CMOS T5 -20%	6.34	140	0.6	4.0	1,644	0	0.5	1.4
CMOS T6	9.15	140	0.6	4.6	2,729	0	0.3	0.8
SRAM								
CMOS Spectrum	1.57	125	0.7	64	7,745	0	0.1	0.3
HCMOS S3	1.81	125	0.7	64	8,927	2	0.4	0.6
HCMOS 4DZ	2.25	125	0.7	6.0	1,042	1	1.9	3.7
EEPROM								
CMOS F4	1.19	140	0.6	3.0	279	0	3.2	8.2
CMOS F4S	4.04	140	0.6	3.0	949	0	1.0	2.4

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	88	0	40	0	1,001	0	1,651	0	258	0	84	0
		– 168 hrs	88	0	40	0	1,001	0	1,651	0	258	0	84	0
		– 500 hrs	88	0	40	0	192	0	635	0	80	0	84	0
		– 1000 hrs	88	0	40	0	192	0	635	0	80	0	84	0
Retention Bake	1008	250°C,												
		– 48 hrs	43	0	40	0	593	0	867	0	173	0	100	0
		– 168 hrs	43	0	40	0	593	0	867	0	173	0	100	0
		– 500 hrs	43	0	40	0	513	0	867	0	173	0	100	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	1,004	0
		– 168 hrs	80	0
		– 500 hrs	80	0
		– 1000 hrs	80	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	80	0
		– 168 hrs	80	0
		– 500 hrs	80	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 5A. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001 (E)		M27C1024		M27C2001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	5,490	0	1,081	0	234	0	3,304	0
		– 168 hrs	1,101	0	80	0	80	0	224	0
		– 500 hrs	623	0	80	0	80	0	160	0
		– 1000 hrs	623	0	80	0	80	0	160	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	727	0	80	0	80	0	198	0
		– 168 hrs	727	0	80	0	80	0	198	0
		– 500 hrs	727	0	80	0	80	0	198	0
		– 1000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 5B. CMOS E5/0.6µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (E)		M27C801		M27C4002		M27C256 M87C257	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 48 hrs	255	0	26,318	0	1,009	0	4,219	0
		– 168 hrs	255	0	2,217	0	855	0	754	0
		– 500 hrs	80	0	806	0	400	0	656	0
		– 1000 hrs	80	0	726	0	400	0	576	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,								
		– 48 hrs	168	0	1,178	0	412	0	605	0
		– 168 hrs	168	0	1,178	0	412	0	605	0
		– 500 hrs	168	0	1,098	0	412	0	605	0
		– 1000 hrs		-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 6. CMOS E6/0.6µm Process (-10% upgrade) UV EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (F)	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	1,170	0
		– 168 hrs	400	0
		– 500 hrs	400	0
		– 1000 hrs	320	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	400	0
		– 168 hrs	400	0
		– 500 hrs	320	0
		– 1000 hrs	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 7. CMOS E6DM/0.6µm Process UV EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C160 (F)		M27C800 (F)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 48 hrs	5,856	0	20,321	0	21,572	0
		– 168 hrs	495	0	418	0	432	0
		– 500 hrs	415	0	418	0	352	0
		– 1000 hrs	415	0	338	0	352	0
		– 2000 hrs	-	-	-	-	-	-
Retention Bake	1008	250°C,						
		– 48 hrs	408	0	420	0	436	0
		– 168 hrs	408	0	420	0	436	0
		– 500 hrs	328	0	420	0	356	0
		– 1000 hrs	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,354 3,354 3,219	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,265	0
Resistance to Solvents	2015	4 Solvent Solutions	276	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	200	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9. CMOS E5/0.8µm Process (–20% Upgrade) OTP EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz		
		– 168 hrs	60	0
		– 500 hrs	60	0
		– 1000 hrs	60	0
		– 2000 hrs	-	-
Retention Bake	1008	150°C,		
		– 168 hrs	60	0
		– 500 hrs	60	0
		– 1000 hrs	60	0
		– 2000 hrs	-	-

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 10. CMOS E5/0.8µm Process (–20% Upgrade) OTP EPROM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 - - - -	 - - - -
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 - - - -	 - - - -
Pressure Pot		121°C, 2Atm, – 48 hrs – 96 hrs – 168 hrs – 240 hrs	 60 60 60 60	 0 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 60 60 60	 0 0 0
Solderability:				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = -/-	
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = -/-	
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-	

Table 11A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 M87C257		M27C512		M27C1001 (E)		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz								
		– 168 hrs	180	0	480	0	834	0	414	0
		– 500 hrs	120	0	360	0	834	0	414	0
		– 1000 hrs	60	0	360	0	774	0	354	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	120	0	300	0	714	0	354	0
		– 500 hrs	60	0	180	0	714	0	354	0
		– 1000 hrs	60	0	120	0	654	0	294	0
		– 2000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 11B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (E)		M27C4002		M27C516		M27C4001	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz								
		– 168 hrs	608	0	264	0	60	0	90	0
		– 500 hrs	608	0	264	0	60	0	90	0
		– 1000 hrs	608	0	264	0	60	0	90	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	548	0	294	0	60	0	60	0
		– 500 hrs	548	0	294	0	60	0	60	0
		– 1000 hrs	548	0	294	0	60	0	60	0
		– 2000 hrs	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 12A. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256 M87C257		M27C512		M27C1001 (E)		M27C1024	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Fail	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	180	0	480	0	834	0	414	0
		– 500 hrs	120	0	360	0	834	0	414	0
		– 1000 hrs	60	0	360	0	774	0	354	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	75	0	205	0	407	0	198	0
		– 96 hrs	75	0	205	0	407	0	198	0
		– 168 hrs	-	-	-	-	-	-	-	-
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	120	0	560	0	894	0	414	0
		– 96 hrs	120	0	360	0	894	0	414	0
		– 168 hrs	120	0	360	0	894	0	414	0
		– 240 hrs	120	0	360	0	894	0	414	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	120	0	548	0	834	0	385	0
		– 500 cycles	120	0	548	0	834	0	385	0
		– 1000 cycles	120	0	548	0	834	0	385	0
Solderability:			See cumulative data on Table 12B							
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr								
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr								
Resistance to Solvents	2015	4 Solvent Solutions								

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 12B. CMOS E5/0.6µm Process (–35% Upgrade) OTP EPROM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C2001 (E)		M27C4002		M27C516		M27C4001	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Fail	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	618	0	264	0	60	0	90	0
		– 500 hrs	618	0	264	0	60	0	90	0
		– 1000 hrs	618	0	264	0	60	0	90	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	289	0	97	0	25	0	45	0
		– 96 hrs	289	0	97	0	25	0	45	0
		– 168 hrs	-	-	-	-	25	0	-	-
		– 240 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	618	0	264	0	60	0	90	0
		– 96 hrs	618	0	264	0	60	0	90	0
		– 168 hrs	618	0	264	0	60	0	90	0
		– 240 hrs	618	0	264	0	60	0	90	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	579	0	240	0	60	0	90	0
		– 500 cycles	579	0	240	0	60	0	90	0
		– 1000 cycles	579	0	240	0	60	0	90	0
Solderability:										
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 780/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 150/0							
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 332/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 13. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz		
		– 168 hrs	180	0
		– 500 hrs	180	0
		– 1000 hrs	180	0
		– 2000 hrs	-	-
Retention Bake	1008	150°C,		
		– 168 hrs	180	0
		– 500 hrs	180	0
		– 1000 hrs	180	0
		– 2000 hrs	-	-

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 14. CMOS E6/0.6µm Process (–10% Upgrade) OTP EPROM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	180	0
		– 500 hrs	180	0
		– 1000 hrs	180	0
		– 2000 hrs	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,		
		– 48 hrs	75	0
		– 96 hrs	75	0
		– 168 hrs	-	-
		– 240 hrs	-	-
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	180	0
		– 96 hrs	180	0
		– 168 hrs	180	0
		– 240 hrs	180	0
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	180	0
		– 500 cycles	180	0
		– 1000 cycles	180	0
Solderability:				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	50	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	-	-
Resistance to Solvents	2015	4 Solvent Solutions	20	0

Table 15. CMOS E6DM//0.6µm Process OTP EPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001		M27C160	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 168 hrs	180	0	60	0
		– 500 hrs	180	0	60	0
		– 1000 hrs	180	0	-	-
		– 2000 hrs	-	-	-	-
Retention Bake	1008	150°C,				
		– 168 hrs	120	0	60	0
		– 500 hrs	120	0	-	-
		– 1000 hrs	60	0	-	-
		– 2000 hrs	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 16. CMOS E6DM/0.6µm Process OTP EPROM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C4001 (F)		M27C160	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	180	0	60	0
		– 500 hrs	180	0	60	0
		– 1000 hrs	180	0	-	-
		– 2000 hrs	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	80	0	25	0
		– 96 hrs	80	0	25	0
		– 168 hrs	-	-	-	-
		– 240 hrs	-	-	-	-
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	180	0	60	0
		– 96 hrs	180	0	60	0
		– 168 hrs	180	0	60	0
		– 240 hrs	180	0	-	-
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	180	0	-	-
		– 500 cycles	-	-	-	-
		– 1000 cycles	-	-	-	-
Solderability:						
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 75/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 25/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 32/0			

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 17. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 24 hrs	463	0	398	0	112,179	0	52,638	0
		– 168 hrs	300	0	360	0	1,365	0	677	0
		– 500 hrs	240	0	360	0	1,365	0	557	0
		– 1000 hrs	180	0	240	0	1,365	0	497	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	300	0	300	0	1,804	0	767	0
		– 500 hrs	240	0	300	0	1,744	0	707	0
		– 1000 hrs	240	0	240	0	1,648	0	647	0
Retention Bake	1008	250°C,								
		– 168 hrs	-	-	-	-	120	0	-	-
		– 500 hrs	-	-	-	-	120	0	-	-
		– 1000 hrs	-	-	-	-	120	0	-	-
Write/Erase Cycling		1,000 cycles	2,651	0	3,451	0	19,104	0	12,891	0
		10,000 cycles	-	-	-	-	2,403	0	-	-
Retention Bake	1008	150°C, 36 hrs	2,651	0	3,451	0	16,701	0	12,891	0

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 18. CMOS T5/0.8µm Process (–20% upgrade) Flash Memory Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)		M28F102 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	300	0	360	0	1,375	0	624	0
		– 500 hrs	240	0	360	0	1,315	0	564	0
		– 1000 hrs	180	0	240	0	1,255	0	504	0
		– 2000 hrs	-	-	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	150	0	150	0	720	0	313	0
		– 96 hrs	150	0	150	0	720	0	313	0
		– 168 hrs	150	0	150	0	720	0	313	0
		– 240 hrs	90	0	60	0	510	0	193	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	300	0	300	0	1,296	0	624	0
		– 96 hrs	300	0	300	0	1,296	0	624	0
		– 168 hrs	240	0	300	0	1,296	0	564	0
		– 240 hrs	240	0	300	0	1,296	0	564	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	240	0	300	0	1,298	0	624	0
		– 500 cycles	180	0	300	0	1,298	0	564	0
		– 1000 cycles	180	0	300	0	1,298	0	504	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability:										
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 425/0							
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 150/0							
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 232/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 19. CMOS T6/0.6µm Process Flash Memory Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 M28F410 M28F420		M29F040 M29W040		M28F201		M28F210 M28F211 M28F220	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,								
		– 24 hrs	48,626	0	112,195	0	54,364	0	57,601	0
		– 168 hrs	999	0	1,065	0	504	0	300	0
		– 500 hrs	999	0	1,005	0	444	0	300	0
		– 1000 hrs	999	0	945	0	384	0	240	0
Retention Bake (1)	1008	150°C,								
		– 168 hrs	1,219	0	1,140	0	504	0	444	0
		– 500 hrs	1,219	0	1,110	0	444	0	444	0
		– 1000 hrs	1,219	0	1,050	0	384	0	384	0
Retention Bake	1008	250°C,								
		– 168 hrs	712	0	478	0	144	0	-	-
		– 500 hrs	712	0	478	0	144	0	-	-
		– 1000 hrs	545	0	178	0	144	0	-	-
Write/Erase Cycling		1,000 cycles	10,157	0	21,176	0	7,095	0	6,907	0
		10,000 cycles	828	0	834	0	180	0	-	-
		100,000 cycles	384	0	270	0	120	0	-	-
		150°C, 36 hrs	10,695	0	21,722	0	7,095	0	6,907	0
Retention Bake	1008									

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.

Table 20. CMOS T6/0.6µm Process Flash Memory Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F411 M28F410 M28F420		M29F040 M29W040		M28F201		M28F211 M28F210 M28F220	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	1,017	0	1,008	0	504	0	300	0
		– 500 hrs	1,017	0	948	0	444	0	300	0
		– 1000 hrs	1,017	0	888	0	444	0	240	0
		– 2000 hrs	60	0	-	-	-	-	-	-
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,								
		– 48 hrs	512	0	510	0	252	0	150	0
		– 96 hrs	512	0	510	0	252	0	150	0
		– 168 hrs	512	0	510	0	252	0	120	0
		– 240 hrs	422	0	360	0	132	0	30	0
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	1,017	0	1,010	0	504	0	444	0
		– 96 hrs	1,017	0	1,010	0	504	0	444	0
		– 168 hrs	1,017	0	950	0	504	0	444	0
		– 240 hrs	1,017	0	950	0	444	0	444	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	934	0	834	0	441	0	427	0
		– 500 cycles	934	0	774	0	441	0	427	0
		– 1000 cycles	926	0	714	0	381	0	372	0
Thermal Shock	1011	–55 to 125°C,								
		– 100 cycles	-	-	-	-	-	-	-	-
		– 500 cycles	-	-	-	-	-	-	-	-
Solderability:										
– TSOP, SO Package	CECC 90,000	215°C, 3sec. Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 365/0							
Resistence to Solvents	2015	4 Solvent Solution	Cumulative Sample/Fail = 184/0							

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 21. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C02 ST24W02		ST24C08		ST93C06C ST93C46C		ST95010		ST95020		M28C64C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,												
		– 24 hrs	-	-	-	-	13,800	0	-	-	-	-	-	-
		– 168 hrs	-	-	-	-	1,800	0	-	-	-	-	-	-
		– 500 hrs	-	-	-	-	1,800	0	-	-	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,												
		– 168 hrs	-	-	-	-	950	0	-	-	-	-	-	-
		– 500 hrs	-	-	-	-	950	0	-	-	-	-	-	-
		– 1000 hrs	-	-	-	-	950	0	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	-	-	-	-	1,200	0	-	-	-	-	-	-
		1,000,000 cycles	-	-	-	-	1,200	0	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	-	-	-	-	1,200	0	-	-	-	-	-	-

Table 22. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C02 ST24W02		ST24C08		ST93C06C ST93C46C		M28C64C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	-	-	-	-	860	0	-	-
		– 500 hrs	-	-	-	-	860	0	-	-
		– 1000 hrs	-	-	-	-	860	0	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	-	-	-	-	650	0	50	0
		– 96 hrs	-	-	-	-	650	0	50	0
		– 168 hrs	-	-	-	-	650	0	50	0
		– 240 hrs	-	-	-	-	650	0	50	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	-	-	-	-	650	0	50	0
		– 200 cycles	-	-	-	-	-	-	-	-
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability:										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 25/0							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 25/0							
– PLCC Package			Cumulative Sample/Fail = -/-							
– TSOP Package			Cumulative Sample/Fail = -/-							
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 24/0							
Resististance to Surface Mount:										
– SO Package			Cumulative Sample/Fail = 50/0							
– TSOP Package			Cumulative Sample/Fail = -/-							

Table 23. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24LC21		ST24C16 ST25C16		ST24E32 ST25E32	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,									-	-	-	-	-	-
		– 24 hrs	14,650	0	12,600	0	9,600	0	6,450	0	-	-	-	-	-	-
		– 168 hrs	1,650	0	2,600	0	1,600	0	450	0	-	-	-	-	-	-
		– 500 hrs	1,650	0	2,600	0	1,600	0	450	0	-	-	-	-	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-						
Retention Bake	1008	150°C,														
		– 168 hrs	650	0	600	0	600	0	200	0	-	-	-	-	-	-
		– 500 hrs	650	0	600	0	600	0	200	0	-	-	-	-	-	-
		– 1000 hrs	650	0	600	0	600	0	200	0	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	1,100	0	1,200	0	1,200	0	400	0	-	-	-	-	-	-
		1,000,000 cycles	1,100	0	1,200	0	1,200	0	400	0	-	-	-	-	-	-
Retention Bake	1008	150°C, 168 hrs	1,100	0	1,200	0	1,200	0	400	0	-	-	-	-	-	-

Table 24. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24E32 ST25E32		ST24C16 ST25C16	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	800	0	960	0	510	0	180	0	-	-	420	0
		– 500 hrs	800	0	960	0	510	0	180	0	-	-	420	0
		– 1000 hrs	800	0	960	0	510	0	180	0	-	-	420	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	1,000	0	1,300	0	600	0	200	0	450	0	600	0
		– 96 hrs	1,000	0	1,300	0	600	0	200	0	450	0	600	0
		– 168 hrs	1,000	0	1,300	0	600	0	200	0	450	0	600	0
		– 240 hrs	1,000	0	1,300	0	600	0	200	0	450	0	600	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	850	0	1,100	0	550	0	100	0	450	0	600	0
		– 200 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		–40 to 150°C,												
		– 500 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Solderability:														
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 144/0											
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 48/0											
– PLCC Package			Cumulative Sample/Fail = -/-											
– TSOP Package			Cumulative Sample/Fail = -/-											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 184/0											
Resististance to Surface Mount:														
– SO Package			Cumulative Sample/Fail = 5,560/0											
– TSOP Package			Cumulative Sample/Fail = -/-											

Table 25. CMOS SPECTRUM/2.0μm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f =1MHz		
		– 168 hrs	2,051	0
		– 500 hrs	1,639	0
		– 1000 hrs	1,366	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 26. CMOS SPECTRUM/2.0μm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 671 396 307	 0 0 0
Temperature Cycling Caphat	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 238 - -	 1 (a) - -
Resistance to Solvents	2015	4 Solvent Solutions	80	0

Note: Fail a. Solder joint failure.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 27. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f =1KHz		
		– 168 hrs	2,111	2 (a)
		– 500 hrs	1,902	0
		– 1000 hrs	1,651	0

Note: Fail a. - Power fail deselect voltage failure. Trip point shifted slightly.
- Mechanical domage on metal 2 write signal.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 28. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08 MK48T18	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 876 796 716	 0 0 1 (a)
Temperature Cycling CAPHAT	1010	–40 to 100°C, – 100 cycles – 500 cycles – 1000 cycles	 80 - -	 0 - -
Resistance to Solvents	2015	4 Solvent Solutions	60	0

Note: Fail a. Solder joint failure.

Table 29. HCMOS 4DZ/0.8µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz				
		– 168 hrs	298	1 (a)	2,464	0
		– 500 hrs	297	0	1,608	0
		– 1000 hrs	297	0	1,428	0
		– 2000 hrs	297	0	-	-

Note: Fail a. Contact spiking, was corrected using a double RTA (Annealing process) and verified with HTOL and static bake.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 30. HCMOS 4DZ/0.8µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, October 1996 to September 1997

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M48T35 M48T35Y		M48T58 M48T58Y	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 - - -	 - - -	 - - -	 - - -
Hast	CECC 90,000	130°C, RH=85%,Vcc = 5V, - 96 hrs - 168 hrs - 240 hrs	 66 66 -	 0 0 -	 - - -	 - - -
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 423 423 265	 0 0 0	 800 720 640	 0 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 56/0			

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

– Electromigration in metal connections
– Contact spiking
– Process contamination
– Oxides defects
– Misplaced or weakened wire bonds
– Damaged wires
– Device surface damage

Table 31. Statistical Process Control: CMOS E5/0.8µm Process UV EPROM and OTP EPROM, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q 97		2Q 97		1Q 97		4Q 96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	2.01	1.85	1.95	1.86	1.86	1.84	1.86	1.68
Silicon Nitride Thickness	1.60	1.59	1.60	1.60	1.54	1.52	1.66	1.63
Field Oxide Thickness	2.38	2.24	1.52	1.47	1.98	1.96	1.76	1.64
Gate Oxide Thickness	1.46	1.34	1.51	1.47	1.46	1.46	1.57	1.51
Interpoly Oxide Thickness	1.84	1.77	1.66	1.56	1.62	1.61	1.56	1.41
Intermediate Dielectric Thickness	1.82	1.75	1.80	1.77	1.90	1.86	1.72	1.68
Polysilicon I Thickness	1.63	1.55	1.49	1.48	1.34	1.33	1.84	1.76
Active Area Critical Dimensions	2.24	2.17	1.39	1.38	1.83	1.68	1.99	1.81
Policide Critical Dimensions	1.81	1.79	1.59	1.59	1.95	1.61	2.09	1.76

Key Electrical Parameters	3Q 97		2Q 97		1Q 97		4Q 96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	1.92	1.38	2.15	1.65	2.20	1.72	2.17	1.56
VT P-Channel 25 x 25 µm	2.48	1.72	1.52	1.50	2.07	1.32	2.13	1.31
VT Natural 25 x 25 µm	3.46	3.12	3.23	2.97	3.52	3.28	3.43	2.99
VT Memory Cell 0.8 x 0.8 µm	1.52	1.41	1.68	1.32	1.53	1.50	1.31	1.25
I_{DON} N-Channel 25 x 0.8 µm	2.65	2.61	2.31	2.23	2.49	2.40	2.51	2.33
N+ Active Area Contact Chain	(*)	6.60	(*)	5.92	(*)	2.85	(*)	2.20
AL-W Silicide Contact Chain Resistance	(*)	2.98	(*)	2.86	(*)	2.27	(*)	2.50

(*) one side limit only

Table 32. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	3Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	2.27	2.23						
Polysilicon I Thickness	2.93	2.89						
Gate Oxide Thickness (1)	1.34	1.28						
Tunnel Oxide Thickness	2.32	2.23						
ONO Bottom Oxide Thickness	1.53	1.50						
ONO Nitride Thickness	1.77	1.66						
ONO Top Oxide Thickness	3.28	3.22						
Active Area Critical Dimensions	1.85	1.50						
Polysilicon II Critical Dimensions	2.20	1.92						

Notes: 1. Exhaust problems (progressive obstruction) solved in week 45 by rebuilding part of the exaust, to avoid this problems detectors have been installed.

Key Electrical Parameters	3Q 97							
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.37	2.06						
VT P-Channel 25 x 25 µm	2.56	1.75						
BV N-Channel 25 x 0.8 µm	(*)	4.75						
BV P-Channel 25 x 0.9 µm	(*)	3.00						
VT Memory Cell 0.8 x 0.8 µm	1.95	1.78						
I_{DON} N-Channel 25 x 0.8 µm	2.59	2.23						
Al-N+ Contact Chain	(*)	3.93						
Al-W Silicide Contact Chain Resistance	(*)	4.01						

(*) one side limit only

Table 33. Statistical Process Control: CMOS T5/0.8µm Process (-20% upgrade) Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 97		2Q 97		1Q 97		4Q 96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.65	1.60	1.69	1.67	2.01	1.96	1.70	1.68
Polysilicon I Thickness (1)	1.22	1.14	1.35	1.25	1.20	1.16	1.23	1.20
Gate Oxide Thickness	1.78	1.55	1.94	1.78	1.91	1.83	1.58	1.72
Tunnel Oxide Thickness	2.04	1.86	1.77	1.65	1.91	1.87	2.24	2.18
ONO Bottom Oxide Thickness	1.46	1.44	1.42	1.39	1.55	1.49	1.40	1.38
ONO Nitride Thickness	1.59	1.52	1.66	1.60	1.52	1.49	1.40	1.37
ONO Top Oxide Thickness	2.02	2.01	1.58	1.57	1.93	1.86	1.76	1.58
Active Area Critical Dimensions	1.39	1.34	1.63	1.38	1.64	1.64	1.48	1.41
Polysilicon II Critical Dimensions	1.38	1.33	1.36	1.36	1.60	1.51	1.32	1.28

Key Electrical Parameters	3Q 97		2Q 97		1Q 97		4Q 96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	1.63	1.36	1.66	1.52	1.74	1.36	1.92	1.50
VT P-Channel 25 x 25 µm	1.59	1.42	1.51	1.48	1.45	1.41	1.57	1.42
BV N-Channel 25 x 0.8 µm	2.15	1.82	1.59	1.39	1.92	1.45	4.84	3.63
BV P-Channel 25 x 0.9 µm	3.25	2.48	2.42	1.84	4.36	3.31	3.75	2.86
VT Memory Cell 0.8 x 0.8 µm	1.70	1.66	2.19	1.73	1.51	1.43	2.05	1.83
I_{DON} N-Channel 25 x 0.8 µm	2.45	2.12	1.53	1.49	1.80	1.60	1.79	1.75
Al-N+ Contact Chain	4.19	3.12	2.43	1.48	4.45	2.72	3.78	2.49
Al-W Silicide Contact Chain Resistance	3.62	3.01	2.83	2.31	1.98	1.70	2.59	1.77

Notes: 1. The furnace temperature control system alignment is going to be implemented.

Table 34. Statistical Process Control: CMOS T6/0.6µm Process Flash Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q97		2Q 97		1Q 97		4Q96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.46	1.42	1.69	1.67	1.95	1.90	1.73	1.71
First Poly Thickness (1)	1.21	1.19	1.45	1.39	1.20	1.16	1.28	1.24
Gate Oxide Hv Thickness	1.85	1.83	1.94	1.78	1.91	1.83	1.68	1.61
Tunnel Oxide Thickness	1.66	1.64	1.77	1.65	1.91	1.87	2.14	2.14
Gate Oxide Lv Thickness (2)	1.39	1.37	1.54	1.44	1.31	1.18	2.29	2.25
ONO Bottom Oxide Thickness	1.49	1.45	1.72	1.55	1.52	1.45	1.49	1.47
ONO Nitride Thickness	1.53	1.49	1.66	1.60	1.52	1.49	1.93	1.93
ONO Top Oxide Thickness	1.70	1.68	1.54	1.44	1.93	1.86	1.69	1.62
Active Area T6U10	1.51	1.49	1.47	1.40	1.72	1.65	1.55	1.51
Second Poly T6U10 C.D.	1.44	1.43	1.64	1.62	1.44	1.41	1.48	1.43

Notes: 1. The furnace temperature control system alignment is going to be implemented.

2. The low value is due to the introduction of this recipe on a vertical furnace. The optimization of the recipe is going on.

Key Electrical Parameters	3Q97		2Q 97		1Q 97		4Q96	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
LV-NCh LVS (10 x .8) SAT.CURRENT	2.26	2.20	2.01	1.97	1.86	1.82	2.95	2.87
LV-PCh LVS (10 x .9) BV	2.61	2.55	3.13	3.09	2.03	1.97	2.25	2.20
LV-PCh (10 x .9)LVS SAT. CURRENT	1.96	1.94	2.08	2.08	1.60	1.56	1.45	1.45
LVP-Ch SQ. VTh	1.41	1.39	1.46	1.41	1.42	1.38	1.90	1.85
HV-NCh (10 X 1.2) LVS BV	1.63	1.59	2.01	1.99	2.01	1.91	2.56	2.56
HV-NCh SQ. VTh	1.63	1.61	1.69	1.65	1.83	1.77	2.36	2.32
HV-NCh (10 X 1.2) LVS SAT.CURRENT	2.47	2.45	2.59	2.57	1.44	1.38	1.92	1.89
HV-PCh (10 x 1.3) BV	2.23	2.18	2.83	2.79	2.40	2.36	3.10	3.03
HV-PCh (10 x 1.3) SAT.CURRENT	1.92	1.90	1.55	1.51	2.52	2.48	2.95	2.95
HVP-Ch SQ. VTh	1.39	1.37	1.41	1.37	1.39	1.35	2.14	2.12
UV ERASED CELL VTh	1.38	1.35	1.44	1.40	1.65	1.61	1.68	1.62
N+ CONTACT CHAIN	2.20	2.00	2.10	2.04	3.53	3.49	3.95	3.95
SILICIDE CONTACT CHAIN	2.36	2.32	3.04	2.96	2.81	2.73	3.34	3.32
LV-NCh (10 X .8) BV	2.20	2.18	1.96	1.94	1.65	1.61	3.15	3.08

Table 35. Statistical Process Control: UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	3Q 97	2Q 97	1Q 97	4Q 96
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	37.14	45.75	16.02	13.57
Stud Pull	1.71	1.35	1.69	1.59
Bond Strength (W.B.)	5.29	4.01	4.07	4.18
SN Thickness (Tin Plate)	1.48	1.58	1.50	1.54

Table 36. Statistical Process Control: TSOP Package Assembly Line, Singapore

Key Process Parameters	3Q 97	2Q 97	1Q 97	4Q 96
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	3.13	2.13	-	-
Ball Shear (W.B.)	1.89	2.54	-	-
Bond Strength (W.B.)	1.57	1.86	-	-
Coplanarity	3.55	4.06	-	-
Plating Thickness	2.00	1.47	-	-

Table 37. Statistical Process Control: PLCC Package Assembly Line, Singapore

Key Process Parameters	3Q 97	2Q 97	1Q 97	4Q 96
	CPK	CPK	CPK	CPK
Shear Test (D.A.)	4.18	3.46	-	-
Ball Shear (W.B.)	2.05	1.88	-	-
Bond Strength (W.B.)	1.62	1.47	-	-
Plating Thickness	3.56	2.77	-	-