AN966
APPLICATION NOTE

L6561, ENHANCED TRANSITION MODE POWER FACTOR CORRECTOR

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The TM (Transition Mode) technique is widely used for Power Factor Correction in low power applications, such as lamp ballasts or low-end monitors. The L6561 is the latest ST's proposal for this market and the emerging ones that are supposed to require a low-cost Power Factor Correction. Based on a well-established architecture, the L6561 offers excellent performance that enlarges its field of application considerably.

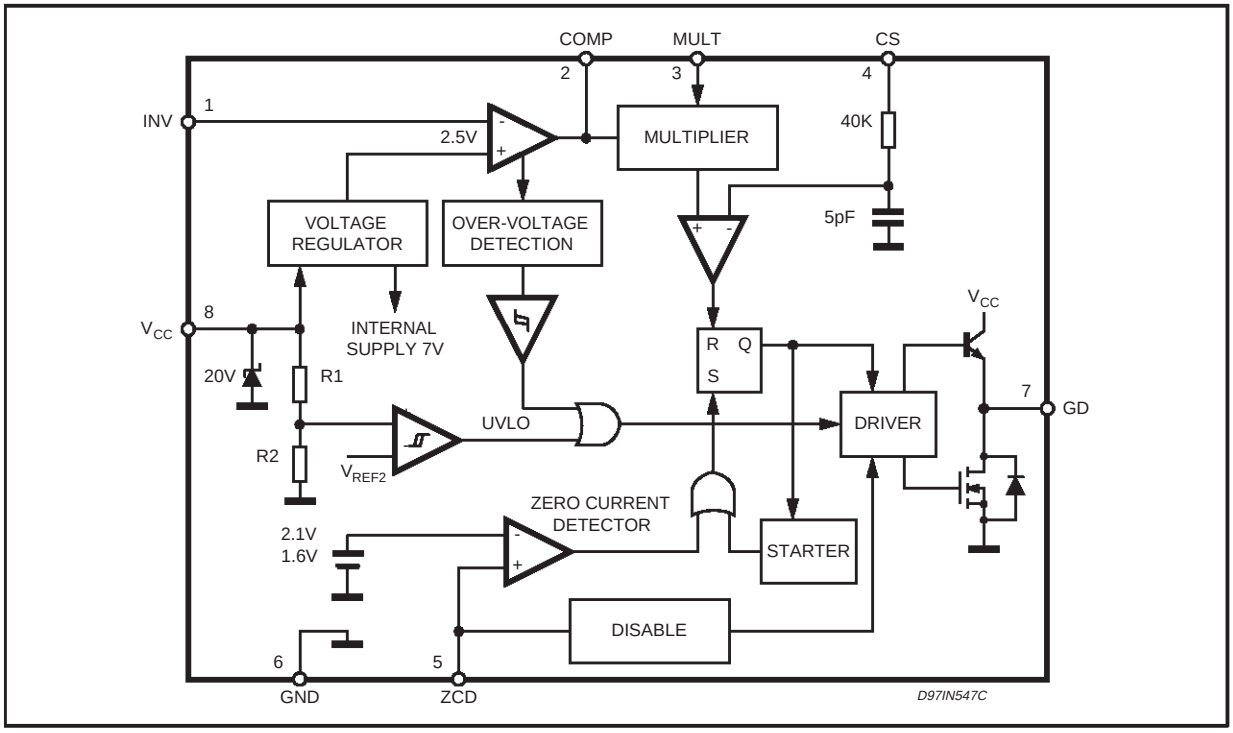
Introduction

The front-end stage of conventional off-line converters, typically made up of a full wave rectifier bridge with a capacitor filter, gets an unregulated DC bus from the AC mains. The filter capacitor must be large enough to have a relatively low ripple superimposed on the DC level. This means that the instantaneous line voltage is below the voltage on the capacitor most of the time, thus the rectifiers conduct only for a small portion of each line half-cycle. The current drawn from the mains is then a series of narrow pulses whose amplitude is 5-10 times higher than the resulting DC value.

Lots of drawbacks result from that: much higher peak and RMS current drawn from the line, distortion of the AC line voltage, overcurrents in the neutral line of the three-phase systems and, after all, a poor utilisation of the power system's energy capability.

This can be measured in terms of either harmonic contents, as norms EN61000-3-2 envisage, or Power Factor (PF), intended as the ratio between the real power (the one transferred to the output) and the apparent power (RMS line voltage times RMS line current) drawn from the mains, which is more immediate. A traditional input stage with capacitive filter has a low PF (0.5-0.7) and high harmonic contents.

Figure 1. Internal Block Diagram of the L6561.



By using switching techniques, a Power Factor Corrector (PFC) preregulator, located between the rectifier bridge and the filter capacitor, allows to draw from the mains a quasi-sinusoidal current, in-phase with the line voltage. The PF becomes very close to 1 (more than 0.99 is possible) and the aforesaid drawbacks are eliminated.

Theoretically, any switching topology can be used to achieve a high PF but, in practice, the boost topology has become the most popular because of the advantages it offers:

1) mainly, the circuit requires the fewest external parts, thus it is the cheapest. Additionally:
2) the boost inductor located between the bridge and the switch causes the input di/dt to be low, thus minimizing the noise generated at the input and, therefore, the requirements on the input EMI filter;
3) the switch is source-grounded, therefore is easy to drive.

However, boost topology requires the DC output voltage to be higher than the maximum expected line peak voltage (400VDC is a typical value for 220V or wide range mains applications). Besides, there is no isolation between input and output, thus any line voltage surge will be passed on to the output.

Two methods of controlling a PFC preregulator are currently widely used: the fixed frequency average current mode PWM and the Transition Mode (TM) PWM (fixed ON-time, variable frequency). The first method needs a complex control that requires a sophisticated controller IC (ST's L4981A, with the variant of the frequency modulation offered by the L4981B) and a considerable component count. The second one requires a simpler control (implemented by ST's L6561), much fewer external parts and is therefore much less expensive.

With the first method the boost inductor works in continuous conduction mode, while TM makes the inductor work on the boundary between continuous and discontinuous mode, by definition. For a given throughput power, TM operation then involves higher peak currents. This, also consistently with cost considerations, suggests its use in a lower power range (typically below 150W), while the former is recommended for higher power levels.

L6561 PFC controller Integrated Circuit

The L6561, whose internal block diagram is shown in fig. 1, is an IC intended to control PFC preregulators by using the Transition Mode technique. The device is available in Minidip and SO8 packages.

The most significant features of the L6561 concern the following points:

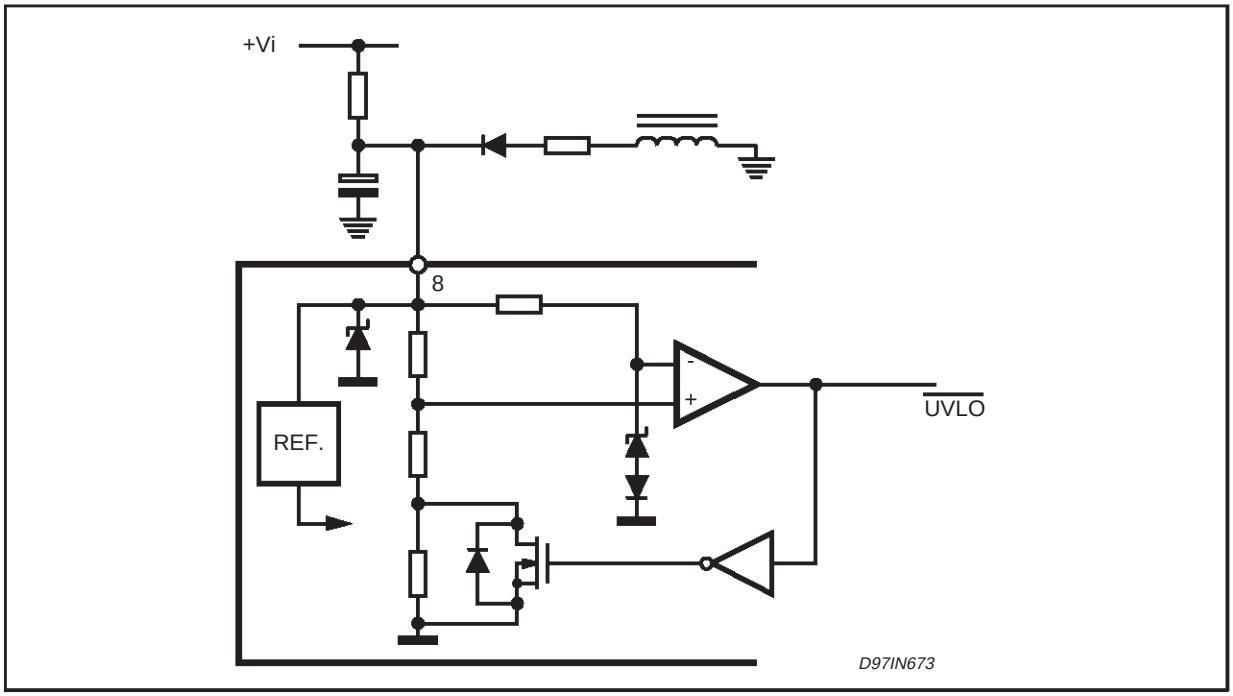
— undervoltage lockout with hysteresis;
— true micropower start-up current (50µA typ., 90µA guaranteed) for simple start-up circuits (just one resistor) with very low power dissipation;
— internal reference with 1% precision guaranteed (@ Tj=25 °C);
— disable function to shut down the device and reduce its current consumption;
— two-level overvoltage protection;
— internal starter and Zero Current Detection circuit for TM operation;
— multiplier with extended dynamics for wide range mains applications, with excellent THD;
— on-chip RC filter on the current sense pin;
— high capability totem pole output for MOSFET or IGBT drive.

The IC is optimised for controlling PFC preregulators based on boost topology in electronic lamp ballasts, AC-DC adapters and low power (<150 W) SMPS. However, its excellent performance along with the extremely reduced external parts count allows also the use in unconventional topologies/applications. Low power off-line AC-DC converters (using isolated flyback topology) with or without Power Factor Correction are the most noticeable examples.

Device Blocks Description

SUPPLY BLOCK
As shown in fig. 1, a linear voltage regulator supplied by Vcc generates an internal 7V rail used to supply the whole integrated circuit, except for the output stage which is supplied directly from Vcc. In addition, a bandgap circuit generates the precise internal reference (2.5V±1% @ 25°C) used by the control loop to ensure a good regulation.
In fig.2 is shown the undervoltage lockout (UVLO) comparator with hysteresis used to enable the chip as long as the Vcc voltage is high enough to ensure a reliable operation.

Figure 2. Internal Supply Block.



ERROR AMPLIFIER AND OVERVOLTAGE DETECTOR BLOCK (see fig. 3 and 4):

The Error Amplifier (E/A) inverting input, through an external divider connected to the output bus, compares a partition of the boosted output DC voltage, Vo, with the internal reference, so to maintain the preregulator output DC voltage constant.

The E/A output is used for frequency compensation, usually realised with a feedback capacitor connected to the inverting input. The E/A bandwidth will be extremely low because the output of the E/A must be constant over a line half-cycle to achieve high PF.

The dynamics of the E/A output is internally clamped so that it can swing between 2V and 5.8V in order to speed up the recovery after the E/A saturates low due to an overvoltage or saturates high because of an overcurrent.

The device is provided with a two-level overvoltage protection (OVP), realized by using the pin connected to the E/A output.

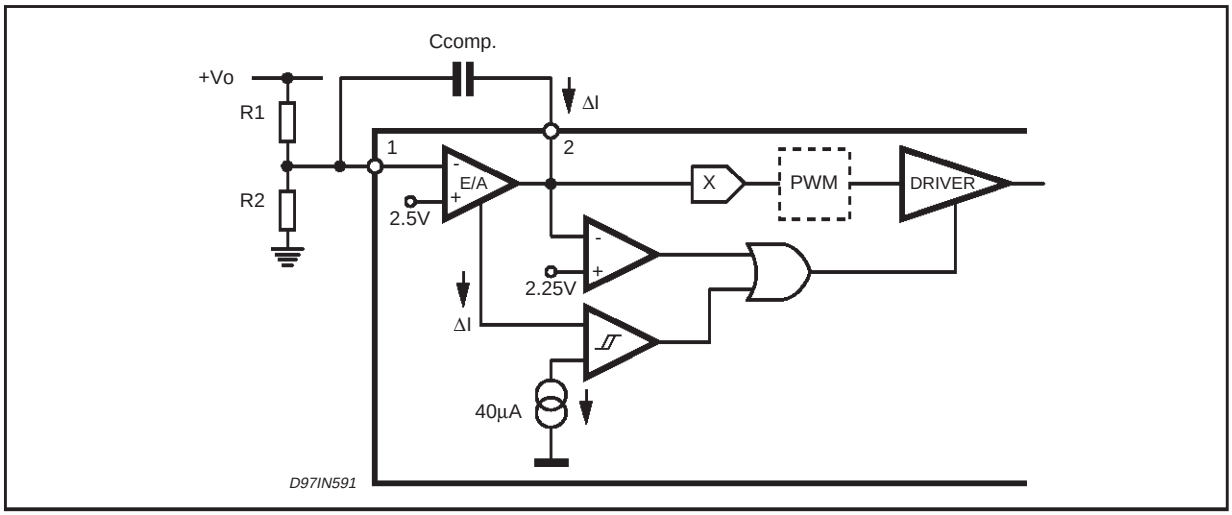
In case of overvoltage, the output of the E/A will tend to saturate low but the E/A response is very slow, so it will take a long time to go into saturation. On the other hand, an overvoltage must be corrected immediately. Hence a fast OVP detector, based on a different concept, is necessary.

In steady state condition, the current through R1 is equal to the current in R2 because the compensation capacitor does not allow DC current to flow (neither does the high-impedance inverting input of the E/A):

$$I_{R1,R2} = \frac{V_o - 2.5}{R1} = \frac{2.5}{R2}$$

When the output voltage rises because of a step load change, the current in R1 builds up as well but the current through R2, fixed by the internal 2.5V reference, does not because of the E/A slowness. The current in excess will then flow through the feedback capacitor and enter the low-inpedance E/A output, where it is sensed. In case, a two-step procedure can occur.

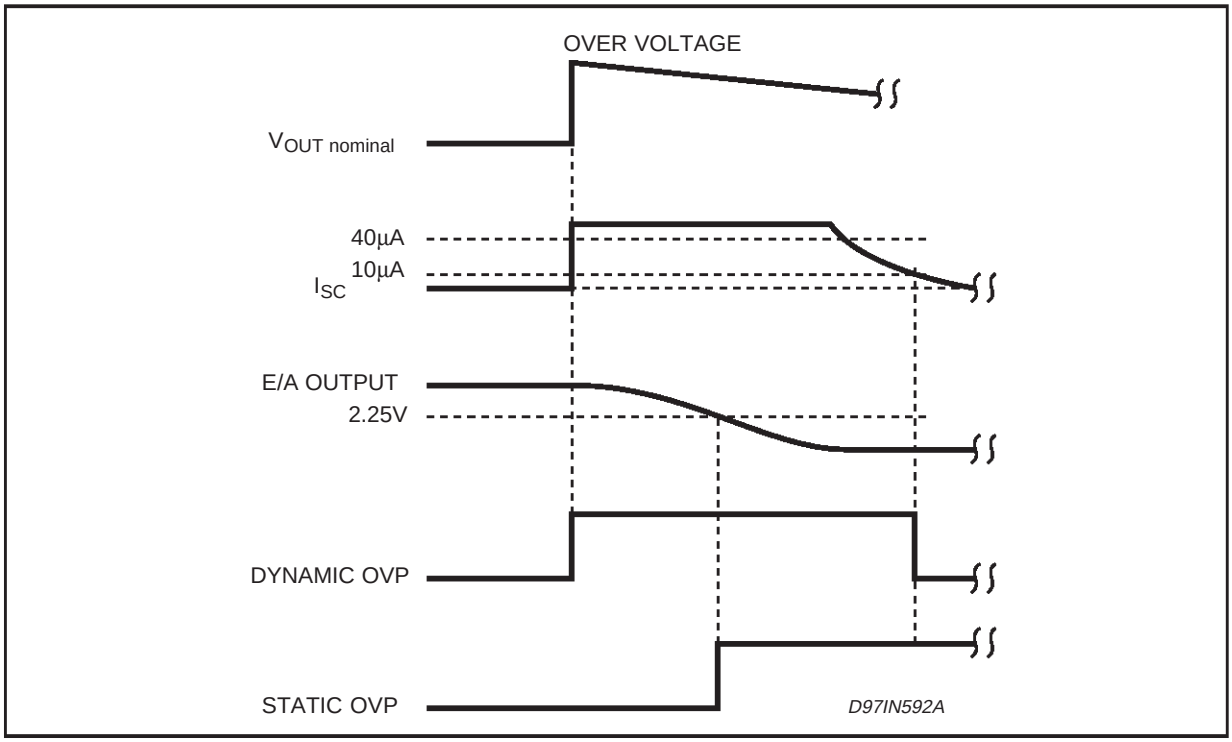
Figure 3. Error Amplifier and Overvoltage Detector Block.



When the current in excess reaches about 37μA, the output voltage of the multiplier is forced to decrease thus the energy drawn from the mains is reduced. This slows down the rate of rise of the output voltage. In some cases, this "soft braking" action is able to prevent the output voltage from exceeding the regulated value too much.

If the output voltage further increases despite the soft braking, so that the current entering the E/A reaches 40μA, a "sharp braking" takes place. The output of the multiplier is pulled to ground, thus turning off the output stage and the external MOSFET. Also the internal starter is switched off. The internal current comparator is provided with hysteresis, thus the pull-down will be released and the output stage re-enabled as the current entering the E/A falls approximately below 10μA.

Figure 4. Dynamic and Static OVP operation.



This dynamic OVP, with its combination of soft and sharp braking, is effective to handle most of load changes but does not provide a complete protection. In fact it is sensitive to output voltage variations (whence the appellative "dynamic") and cannot reveal a steady overvoltage, which is likely to occur in case of load disconnection.

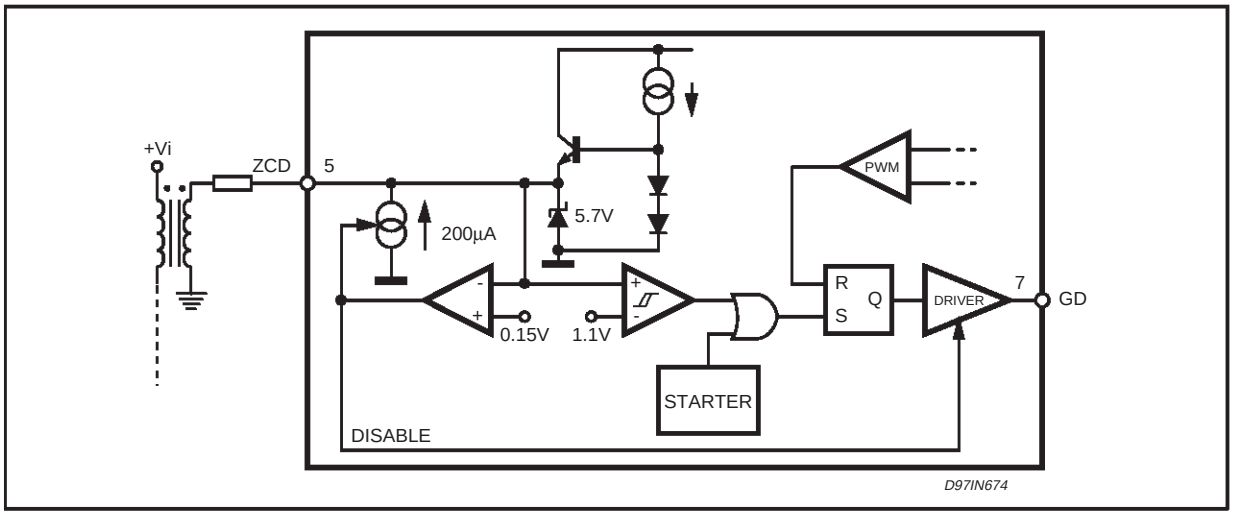
The above mentioned concept of the E/A saturation is effective to achieve a "static" OVP. If the overvoltage lasts so long that the output of E/A goes below 2.25V (the E/A is in linear dynamics up to 2.5V), the protection is activated. Besides turning off the output stage and the external MOSFET, it disables some internal blocks reducing the quiescent current of the chip to 1.4mA (typ). The operation of the device is re-enabled as the E/A output goes back into its linear region.

Fig. 4 illustrates the combined action of dynamic and static OVP.

ZERO CURRENT DETECTION AND TRIGGERING BLOCK (see fig. 5)

The Zero Current Detection (ZCD) block switches on the external MOSFET as the voltage across the boost inductor reverses, just after the current through the boost inductor has gone to zero. This feature allows TM operation.

Figure 5. Zero Current Detection, Triggering and Disable Block.



As the circuit is running, the signal for ZCD is obtained with an auxiliary winding on the boost inductor. Of course, a circuit is needed that turns on the external MOSFET at start-up since no signal is coming from the ZCD. This is realized with an internal starter, which forces the driver to deliver a pulse to the gate of the MOSFET, producing also the signal for arming the ZCD circuit.

The repetition rate of the starter is greater than 70 ms (≅ 14 kHz) and this maximum frequency must be taken into account at design time.

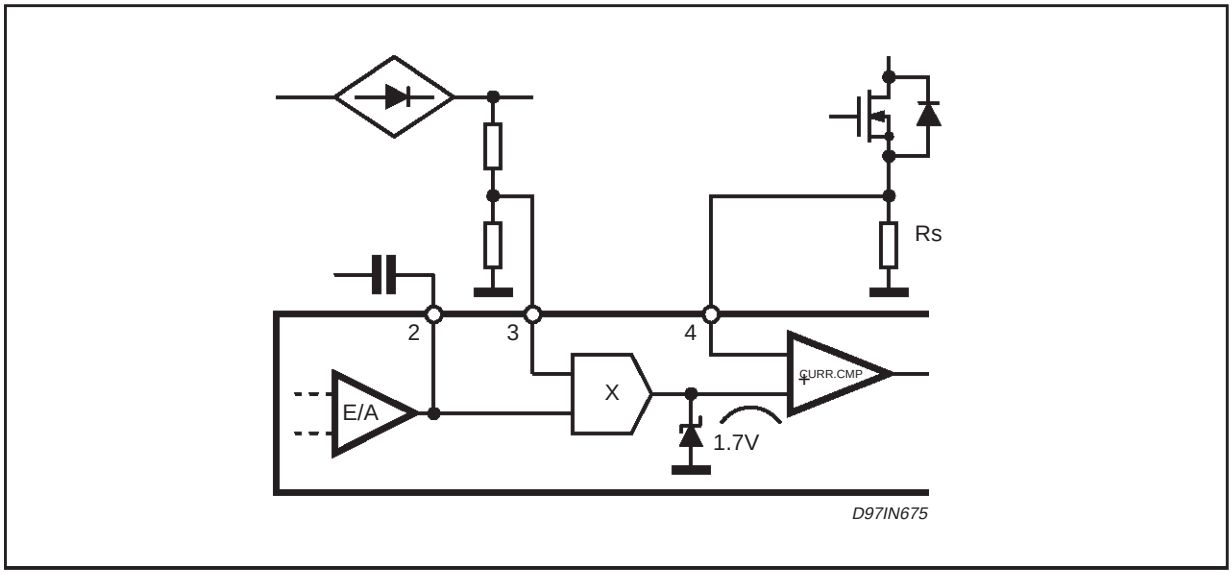
DISABLE BLOCK (see fig. 5)

The ZCD pin is used also to activate the Disable Block. If the voltage on the pin is taken below 150 mV the device will be shut down. As a result, its current consumption will be reduced. To re-enable the device operation, the pull-down on the pin must be released.

MULTIPLIER BLOCK (see fig. 6)

The multiplier has two inputs: the first one takes a partition of the instantaneous rectified line voltage and the second one the output of the E/A. If this voltage is constant (over a given line half-cycle) the output of the multiplier will be shaped as a rectified sinusoid too. This is the reference signal for the current comparator, which sets the MOSFET peak current cycle by cycle.

Figure 6. Multiplier Block.

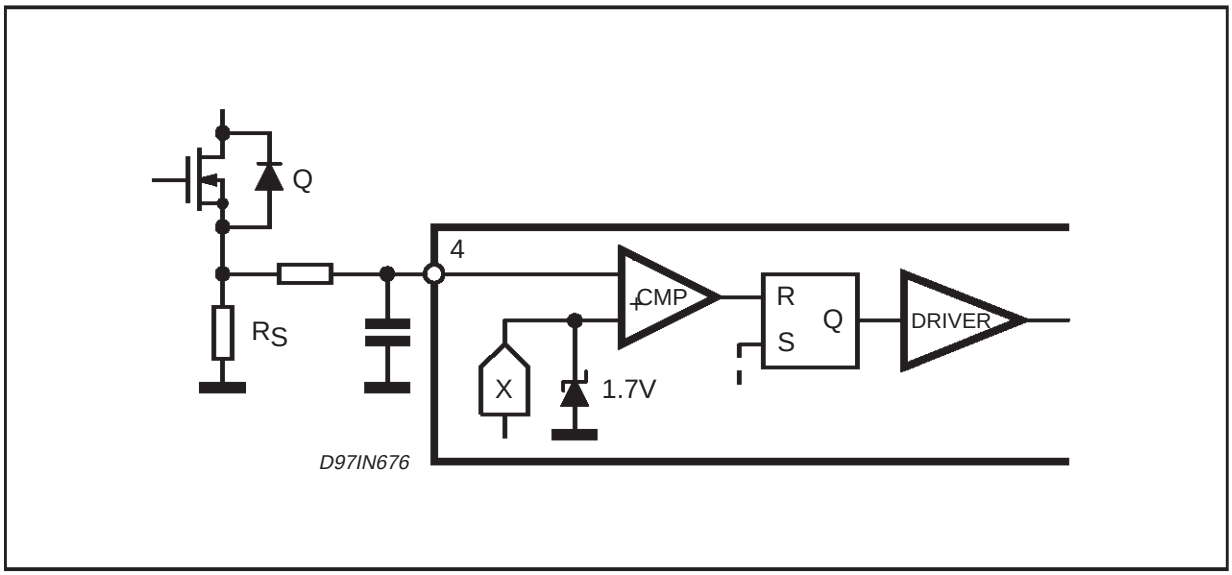


CURRENT COMPARATOR AND PWM LATCH (see fig.7):

The current comparator senses the voltage across the current sense resistor (Rs) and, by comparing it with the programming signal delivered by the multiplier, determines the exact time when the external MOSFET is to be switched off. The PWM latch avoids spurious switchings of the MOSFET which might result from the noise generated.

The output of the multiplier is internally clamped to 1.7V, (typ.) thus current limiting occurs if the voltage across Rs reaches this value.

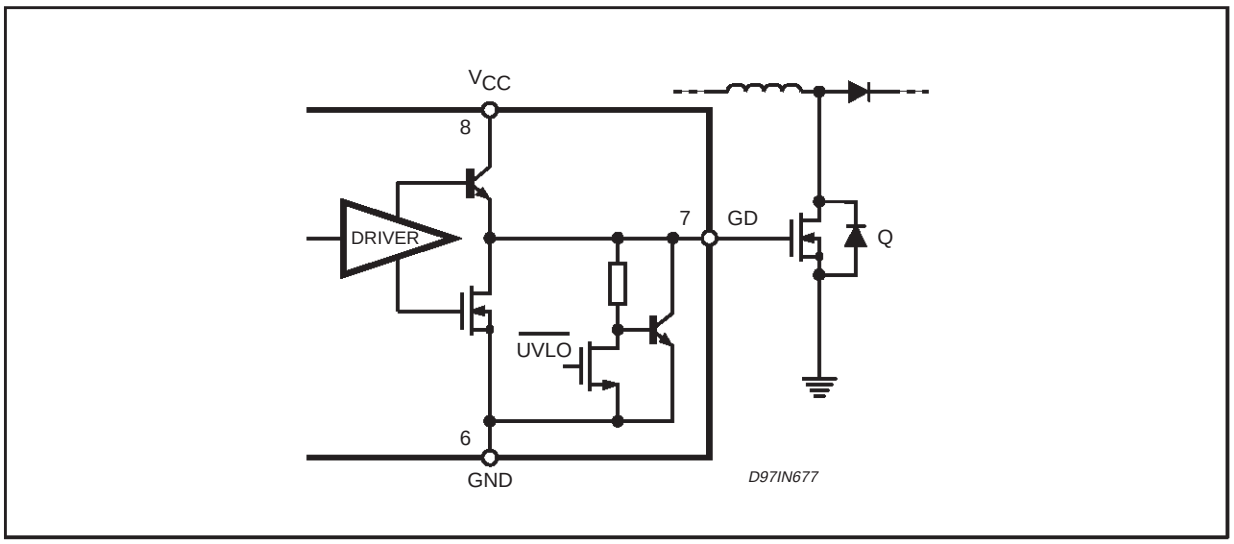
Figure 7. Current Comparator and PWM latch



DRIVER (see fig.8)

A totem pole buffer, with 400mA source and sink capability, allows to drive an external MOSFET. An internal pull-down circuit holds the output low when the device is in UVLO conditions, to ensure that the external MOSFET cannot be turned on accidentally.

Figure 8. Output Driver.



TM PFC Operation (Boost Topology)

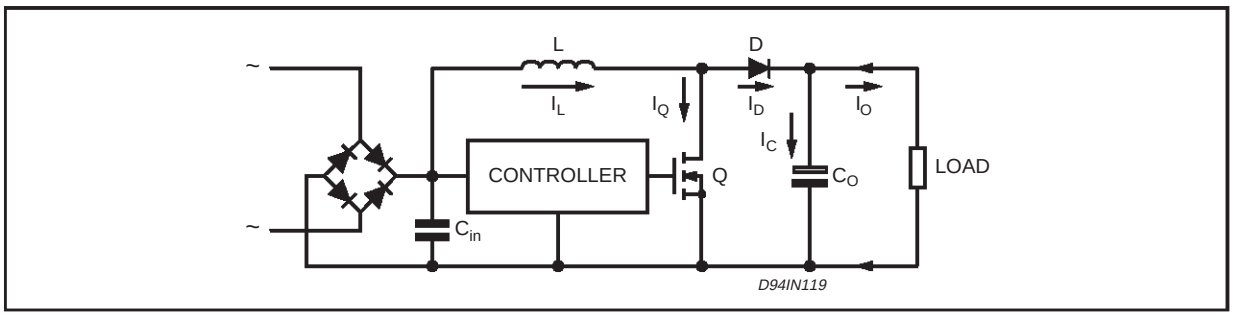
The operation of the PFC Transition Mode controlled boost converter, can be summarized in the following description.

The AC mains voltage is rectified by a diode bridge and the rectified voltage delivered to the boost converter. This, using a switching technique, boosts the rectified input voltage to a regulated DC output voltage (Vo).

The boost converter consists of a boost inductor (L), a controlled power switch (Q), a catch diode (D), an output capacitor (Co) and, obviously, a control circuitry (see fig. 9).

The goal is to shape the input current in a sinusoidal fashion, in-phase with the input sinusoidal voltage. To do this the L6561 uses the so-called Transition Mode technique.

Figure 9. Boost Converter Circuit.



The error amplifier compares a partition of the output voltage of the boost converter with an internal reference, generating a signal error proportional to the difference between them. If the bandwidth of the error amplifier is narrow enough (say, below 20 Hz), the error signal is a DC value over a given half-cycle.

The error signal is fed into the multiplier block and multiplied by a partition of the rectified mains voltage. The result will be a rectified sinusoid whose peak amplitude depends on the mains peak voltage and the value of the error signal.

The output of the multiplier is in turn fed into the (+) input of the current comparator, thus it represents a sinusoidal reference for PWM. In fact, as the voltage on the current sense pin (istantaneous inductor current times the sense resistor) equals the value on the (+) of the current comparator, the conduction of the external MOSFET is terminated. As a consequence, the peak inductor current will be enveloped by a

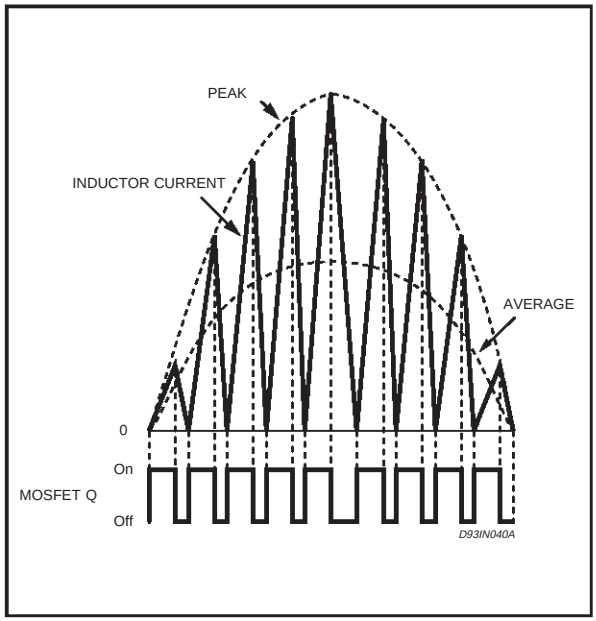
rectified sinusoid. It is possible to prove also that this operation produces a costant ON-time over each line half-cycle.

After the MOSFET has been turned off, the boost inductor discharges its energy into the load until its current goes to zero. The boost inductor has now run out of energy, the drain node is floating and the inductor resonates with the total capacitance of the drain. The drain voltage drops rapidly below the instantaneous line voltage and the signal on ZCD drives the MOSFET on again and another conversion cycle starts.

This low voltage across the external MOSFET at turn-on reduces both the switching losses and the equivalent drain capacitance energy that is dissipated inside the external MOSFET.

The resulting inductor current and the timing intervals of the MOSFET are shown in fig. 10, where it is also shown that, by geometric relationships, the average input current (the one which will be drawn from the mains) is just one-half of the peak inductor current waveform.

Figure 10. Inductor Current waveform and MOSFET timing



The system operates (not exactly on but very close to) the boundary between continuous and discontinuous current mode and that is why this system is called a Transition Mode PFC.

Besides the simplicity and the few external parts required, this system minimizes the inductor size due to the low inductance value needed. On the other hand, the high current ripple on the inductor involves high RMS current and high noise on the rectified main bus, which needs a heavier EMI filter to be rejected. These drawbacks limit the use of the TM PFC to lower power range applications.

Design Criteria

Here below some design criteria are described. The basic design specification concerns the following data:

- Mains Voltage Range: $V_{irms(min)}$ - $V_{irms(max)}$
- Regulated DC Output Voltage: V_o
- Rated Output Power: P_o
- Minimum Switching Frequency: f_{sw}
- Maximum Output Voltage ripple: ΔV_o
- Maximum Overvoltage admitted: ΔV_{OVP}

For reference, it is useful to define also the following quantities:

- Expected efficiency: η
- Input Power: Pi (= P_o/η)
- Maximum Mains RMS current: I_{rms} (= $Pi/V_{irms(min)}$)
- Rated Output Current: Io (= Po/Vo)

POWER SECTION DESIGN

Input Bridge

The input diodes bridge can use standard slow recovery, low-cost devices. The quantities to consider will be just the input current (I_{rms}), the maximum peak mains voltage and the thermal data of the diodes.

Input Capacitor

The input high frequency filter capacitor (C_{in}) has to attenuate the switching noise due to the high fre-

quency inductor current ripple (twice the average line current, see fig. 9). The worst conditions will occur on the peak of the minimum rated input voltage.

The maximum high frequency voltage ripple is usually imposed between 1% and 10% of the minimum rated input voltage. This is expressed by a coefficient r (r = 0.01 to 0.1):

$$C_{in} = \frac{I_{rms}}{2\pi \cdot f_{sw} \cdot r \cdot V_{irms\ (min)}}$$

In real conditions the input capacitance will be designed taking the EMI filter into account.

Output Capacitor

The output bulk capacitor (C_o) selection depends on the DC output voltage, the admitted overvoltage, the output power and the desired voltage ripple.

The 100 to 120Hz (twice the mains frequency) voltage ripple (ΔV_O= 1/2 ripple peak-to-peak value) is a function of the capacitor impedance and the peak capacitor current ($I_{C(2f)pk} = I_o$):

$$\Delta V_O = I_O \cdot \sqrt{\frac{1}{(2\pi \cdot 2f \cdot C_O)^2} + ESR^2}$$

With a low ESR capacitor the capacitive reactance is dominant, therefore:

$$C_O \geq \frac{I_O}{4\pi \cdot f \cdot \Delta V_O} = \frac{P_O}{4\pi \cdot f \cdot V_O \cdot \Delta V_O}$$

ΔVo is usually selected in the range of 1 to 5% of the output voltage.

Although ESR usually does not affect the output ripple, it has to be taken into account for power losses calculation. The total RMS capacitor ripple current, including mains frequency and switching frequency components, is:

$$I_{Crms} = \sqrt{\frac{32\sqrt{2}}{9\pi} \cdot I_{rms}^2 \cdot \frac{V_{irms}}{V_o} - I_o^2}$$

If the application has to guarantee a specified hold-up time, the selection criterion of the capacitance will change: Co has to deliver the output power for a certain time (t_{Hold}) with a specified maximum dropout voltage:

$$C_O = \frac{2 \cdot P_O \cdot t_{Hold}}{V_{o\_min}^2 - V_{op\_min}^2}$$

where Vo_min is the minimum output voltage value (which takes load regulation and output ripple into account) and Vop_min is the minimum output operating voltage before the 'power fail' detection from the downstream system supplied by the PFC.

Boost Inductor

Designing the boost inductor involves several parameters and different approaches can be used.

First, the inductance value must be defined. The inductance (L) is usually determined so that the minimum switching frequency is greater than the maximum frequency of the internal starter, to ensure a correct TM operation. It is possible to write:

$$P_i \approx \frac{L \cdot f_{sw} \cdot I_{Lpk}^2}{2 \cdot \delta}$$

$$L \approx \frac{2 \cdot P_i \cdot \delta}{I_{Lpk}^2 \cdot f_{sw}}$$

where $\delta = 1-V_{it}/V_o$ is the duty cycle, V_{it} is the instantaneous mains voltage and I_{Lpk} is the peak inductor current.

With unity PF, the ratio between the input voltage and the input current is constant and therefore the ON-time of Power MOSFET is constant too. The switching frequency varies with the instantaneous mains voltage and is minimum (along with the duty cycle) on the crest of the sinusoid. In the above formula it will be then considered:

$$f_{sw} = f_{sw(min)}$$

$$\delta = \delta_{min} = \frac{V_o - \sqrt{2} \cdot V_{irms}}{V_o}$$

$$I_{Lpk} = I_{Lpkmax} = 2\sqrt{2} \cdot \frac{P_i}{V_{irms}}$$

The absolute minimum frequency can occur at either the maximum or the minimum mains voltage, thus the inductor value is defined by:

$$L \cong \frac{V^2_{irms} \cdot (V_O - \sqrt{2} \cdot V_{irms})}{2 \cdot f_{sw(min)} \cdot P_i \cdot V_O}$$

where V_{irms} can be either $V_{irms(min)}$ or $V_{irms(max)}$, whichever gives the lower value for L.

The minimum suggested value for $f_{sw(min)}$ is 15 kHz, not to interfere with the internal starter (see ZCD and triggering block description), .

Once defined the value of L, the real design of the inductor can start. As to the magnetic material and the geometry, the need of isolation due to the high voltage, and the operating frequency range make the standard high frequency ferrite (gapped core-set with bobbin) the usual choice in PFC applications. Among the various types offered by manufacturers the most suitable one will be selected with technical and economic considerations.

The next step is to estimate the core size. To get the approximated value of the minimum core size, it is possible to use the following practical formula:

$$Volume \geq 4 \cdot L \cdot I^2_{rms}$$

where Volume is expressed in cm^3 and L in mH.

Then the winding must be specified. The turns number and the wire cross-section are the quantities to be defined.

The input power (P_1) can be expressed in terms of the energy stored inside the core:

$$P_i = \frac{A_e \cdot l_{eff} \cdot \Delta H \cdot \Delta B \cdot f_{sw}}{2 \cdot \delta}$$

where: A_e is the effective area of the core section, l_e is the effective magnetic path length (both data are taken from the data sheet of the core set), ΔH is the excursion of the magnetic field strength and ΔB is the excursion of the magnetic flux density.

To prevent the core from saturating because of its high permeability and allow an adequate ΔH, it is necessary to introduce an air gap.

Despite the gap lenght l_{gap} is few per cent of l_e, the permeability of ferrite is so high (for power ferrites, typically $\mu r = 2500$) that it is possible to assume all the magnetic field concentrated in the air gap with good approximation. For instance, with 1% of l_{gap}/l_e (which is the minimum suggested value) the error caused by this assumption is about 4%. The error will be smaller if the l_{gap}/l_e ratio is bigger.

As a result, the last formula can be re-written as:

$$P_i \cong \frac{A_e \cdot l_{gap} \cdot \Delta H_{gap} \cdot \Delta B \cdot f_{sw}}{2 \cdot \delta}$$

and simplified with:

$$P_i \approx \frac{L \cdot f_{sw} \cdot I_{Lpk}^2}{2 \cdot \delta}$$

to obtain:

$$A_e \cdot l_{gap} \cdot \Delta H_{gap} \cdot \Delta B \cong L \cdot I_{Lpk}^2 .$$

Since

$$l_{gap} \cdot \Delta H_{gap} \cong N \cdot I_{Lpk}$$

and, inside the air gap:

$$\Delta B = \mu_o \cdot \Delta H$$

finally it is possible to obtain:

$$N \cong \sqrt{\frac{L \cdot l_{gap}}{A_e \cdot \mu_o}}$$

where N is the turns number of the winding.

As N is defined, it is recommended to check for the saturation of the core (see Pin 4 description). If the check shows a result too close to the rated limit, an increase of l_{gap} and a new calculation will be necessary.

The wire gauge selection is based on limiting the copper losses at acceptable value:

$$P_{CU} = \frac{4}{3} \cdot I_{rms}^2 \cdot R_{CU};$$

due to the high frequency ripple the effective wire resistance R_{CU} is increased by skin and proximity effects. For this reason Litz wire or multi-wire solutions are recommended.

Finally, the space occupied by the winding will be evaluated and, if it does not fit the winding area of the bobbin, a bigger core set will be considered and the winding calculation repeated.

It is now necessary to add an auxiliary winding to the inductor, in order for the ZCD pin to recognize when the current through the inductor has gone to zero. It is anyway a low cost thin wire winding and the turns number is the only parameter to be defined (see Pin 4 description).

POWER MOSFET

The choice of the MOSFET concerns mainly its R_{DSon}, which depends on the output power, since the breakdown voltage is fixed just by the output voltage, plus the overvoltage admitted and a safety margin.

The MOSFET's power dissipation depends on conduction and switching losses.

The conduction losses are given by:

$$P_{ON} = I_{Qrms}^2 \cdot R_{DSon}$$

where:

$$I_{Qrms} = 2 \cdot \sqrt{2} \cdot I_{rms} \cdot \sqrt{\frac{1}{6} - \frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{irms}}{V_O}} \quad .$$

The switching losses due to current-voltage cross occur only at turn-off because of the TM operation:

$$P_{CROSS} = V_O \cdot I_{rms} \cdot t_{fall} \cdot f_{sw},$$

where t_{fall} is the crossover time at turn-off. At turn-on the loss is due to the discharge of the total drain capacitance inside the MOSFET itself. In general, these losses are given by:

$$P_{CAP} = \left(3.3 \cdot C_{oss} \cdot V_{DRAIN}^{1.5} + \frac{1}{2} \cdot C_d \cdot V_{DRAIN}^2\right) \cdot f_{sw} \ ,$$

where C_{oss} is the internal drain capacitance of the MOSFET (@ V_{DS} = 25V), Cd is the total external drain parasitic capacitance and V_{DRAIN} is the drain voltage at MOSFET turn-on. In practice it is possible to give only a rough estimate of the total switching losses because both f_{sw} and V_{DRAIN} change along a given line half-cycle. V_{DRAIN}, in particular, is affected not only by the sinusoidal change of the input voltage but also by the drop due to the resonance of the boost inductor with the total drain capacitance (see fig. 12). This causes, at low mains voltage, V_{DRAIN} to be zero during a significant portion of each line half-cycle.

BOOST DIODE

The boost freewheeling diode will be a fast recovery one. The value of its DC and RMS current, useful for losses computation, are respectively:

$$I_{Do} = I_o$$

$$I_{Drms} = 2 \cdot \sqrt{2} \cdot I_{rms} \cdot \sqrt{\frac{4\sqrt{2}}{9\pi} \cdot \frac{V_{irms}}{V_O}} \quad .$$

The conduction losses can be estimated as follows:

$$P_{DON} = V_{to} \cdot I_{Do} + R_d \cdot I_{Drms}^2 \ ,$$

where V_{to} (threshold voltage) and R_d (differential resistance) are parameters of the diode.
The breakdown voltage is fixed with the same criterion as the MOSFET.

L6561 Biasing Circuitry (pin by pin)

Please, refer to the schematic circuit shown in fig. 13.

Pin 1 (INV) leads both to the inverting input of the E/A and to the OVP circuit. A resistive divider will be connected between the regulated output voltage of the boost and the pin.
The internal reference on the non-inverting input of the E/A is 2.5V and the OVP alarm level current is 40µA. R7 and R8 will be then selected as follow:

$$\frac{R7}{R8} = \frac{V_O}{2.5V} - 1 \quad R7 = \frac{\Delta V_{OVP}}{40\ \mu A} \ ,$$

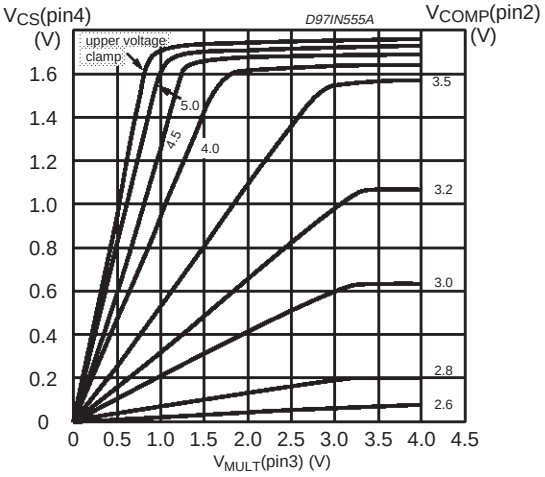
Pin 2 (COMP) is the output of the E/A and also one of the two inputs of the multiplier. A feedback compensation network, placed between this pin and INV (1), reduces the bandwidth so to avoid the attempt of the system to control the output voltage ripple (100-120Hz).
In the simplest case, this compensation is just a capacitor, which provides a low frequency pole as well as a high DC gain. A simple criterion to define the capacitance value, is to set the bandwidth (BW) from 20 to 30Hz:

$$BW = \frac{1}{2\pi \cdot (R7 \,//\, R8) \cdot C3}$$

$$C3 = \frac{1}{2\pi \cdot (R7 \,//\, R8) \cdot BW}$$

Please refer to [1] for more information on how to compensate the E/A.

Figure 11. Multiplier characteristics family



Pin 3 (MULT) is the second multiplier input. It will be connected, through a resistive divider, to the rectified mains to get a sinusoidal voltage reference. The multiplier can be described by the relationship:

$$V_{cs} = k \cdot (V_{COMP} - 2.5V) \cdot V_{MULT}$$

where V_{CS} (Multiplier output) is the reference for the current sense, k is the multiplier gain, V_{COMP} is the voltage on pin 2 (E/A output) and V_{MULT} is the voltage on pin 3.

A complete description is given by the diagram of fig. 11, which shows the typical multiplier characteristics family. The linear operation of the multiplier is guaranteed inside the range 0 to 3V of V_{MULT} and the range 0 to 1.6V of V_{CS}, while the minimum guaranteed value of the maximum slope of the characteristics family ($\Delta V_{CS}/\Delta V_{COMP}$) is 1.65. Taking this into account, the following is the suggested procedure to set properly the operating point of the multiplier.

First, the maximum peak value for V_{MULT}, $V_{MULTpkx}$, is selected. This value, which will occur at maximum mains voltage, should be 3V or nearly so in wide range mains and less in case of single mains. The minimum peak value, occurring at minimum mains voltage will be:

$$V_{MULTpkmin} = V_{MULTpkx} \cdot \frac{V_{irms(min)}}{V_{irms(max)}}$$

This value, multiplied by the minimum guaranteed $\frac{\Delta V_{CS}}{\Delta V_{COMP}}$ will give the maximum peak output voltage of the multiplier:

$$V_{XCSpk} = 1.65 \cdot V_{MULTpkmin}$$

If the resulting V_{XCSpk} exceeds the linearity limit of the current sense (1.6V), the calculation should be repeated beginning with a lower $V_{MULTpkx}$ value.

In this way, the divider will be such that:

$$\frac{R10}{R9 + R10} = \frac{V_{MULTpkx}}{\sqrt{2} \cdot V_{irms(max)}}$$

the individual values can be chosen by setting the current through R10, in the hundreds μA or less to minimise power dissipation.

Pin 4 (CS) is the inverting input of the current sense comparator. Through this pin, the L6561 reads the instantaneous inductor current, converted to a proportional voltage by an external sense resistor (Rs). As this signal crosses the threshold set by the multiplier output, the PWM latch is reset and the power MOSFET is turned off. The MOSFET will stay in OFF-state until the PWM latch is set again by the ZCD signal. An internal circuit ensures that the PWM latch cannot be set until the signal on pin 4 has disappeared.

The sense resistor value is calculated as follows:

$$R_S \leq \frac{V_{XCSpk}}{I_{Rspk}}$$

where V_{XCSpk} has been calculated as per described earlier and:

$$I_{Rspk} = 2\sqrt{2} \cdot I_{rms},$$

The power dissipated in Rs, given by:

$$P_{Rs} = \frac{4}{3} \cdot R_s \cdot I_{rms}^2 ,$$

will not exceed 1% of the rated output power.
The internal 1.8V (max.) zener clamp on the non-inverting input of the PWM comparator sets a current limitation threshold, so that the maximum current through Rs is:

$$I_{Rspkmax} = \frac{1.8}{R_s}.$$

This will be the maximum inductor current as well, therefore this value has to be used when checking for the ferrite core saturation.

Pin 5 Pin 5 (ZCD) is the input to the Zero Current Detector circuit. The ZCD pin will be connected to the auxiliary winding of the boost inductor through a limiting resistor.

The ZCD circuit is negative-going edge-triggered: when the voltage on the pin falls below 1.6 V the PWM latch is set and the MOSFET is turned on. To do so, however, the circuit must be armed first: prior to falling below 1.6V the voltage on pin 5 must experience a positive-going edge exceeding 2.1 V (due to MOSFET's turn-off).

The maximum main-to-auxiliary winding turn ratio, m, has to ensure that the voltage delivered to the pin during MOSFET's OFF-time is sufficient to arm the ZCD circuit. Then:

$$m \leq \frac{V_o - \sqrt{2} \cdot V_{irms\ (max.)}}{2.1}$$

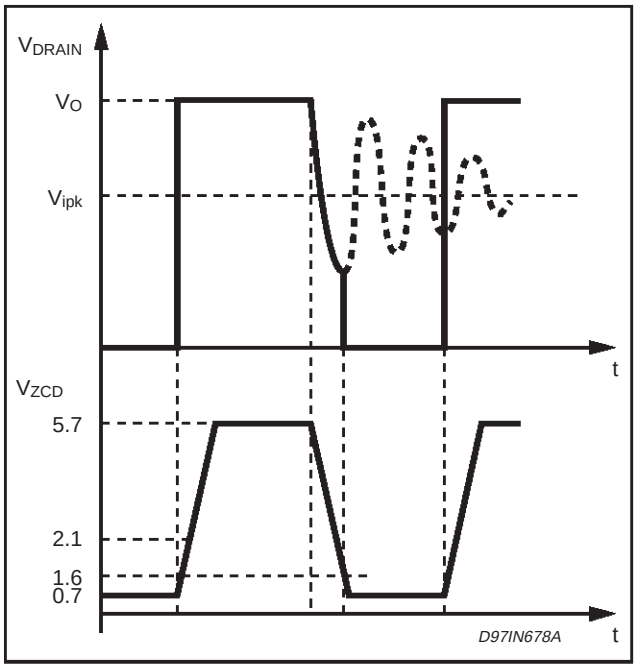
If the winding is used also for supplying the IC, the above criterion may not be compatible with the Vcc voltage range. To solve this incompatibility the self-supply network shown in the schematic of fig. 13 can be used. The minimum value of the limiting resistor can be found assuming 3 mA current through the pin and considering the maximum voltage (the absolute value) across the auxiliary winding.

The actual value can be then fine-tuned trying to make the turn-on of the MOSFET occur exactly on the valley of the drain voltage oscillation (the boost inductor, completely discharged, is ringing with the drain capacitance, see fig. 12). This will minimize the power dissipation at turn-on.

If the pin is driven by an external signal, the L6561 will be synchronized to (the negative-going edges of) that signal. If left floating, the L6561 will work at the frequency of its internal starter. Obviously, neither TM operation will take place nor high PF will be achieved in this case, but these characteristics can be exploited in applications other than PFC.

This pin incorporates also a disable function. The device will be shut down if the voltage on the pin is forced externally below 150mV. To do so, up to 10mA must be sunk from the pin. The quiescent current of the IC will be reduced at about 1.4 mA. The device will restart as the external pull-down is removed since an internal 150µA generator pulls up the pin.

Figure 12. Optimum MOSFET Turn-on



Pin 6 (GND). This pin acts as the current return both for the signal internal circuitry and for the gate drive current. When layouting the printed circuit board, these two paths should run separately.

Pin 7 (GD) is the output of the driver. The pin is able to drive an external MOSFET with 400mA source and sink capability.

To avoid undesired switch-on of the external MOSFET because of some leakage current when the supply of the chip is below the UVLO threshold, an internal pull-down circuit holds the pin low. The circuit guarantees 0.3V maximum on the pin (@ I_{sink} = 10mA), with V_{cc} > 3V. This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET used to this purpose.

Pin 8 (V_{cc}) is the supply of the device. This pin will be externally connected to the start-up circuit (usually, one resistor connected to the rectified mains) and to the self-supply circuit.

Whatever the configuration of the self-supply system, a capacitor will be connected between this pin and ground.

To start the L6561, the voltage must exceed the start-up threshold (13V max.). Below this value the device does not work and consumes less than 90µA from V_{cc}. This allows the use of high value start-up resistors (in the hundreds kΩ), which reduces power consumption and optimises system efficiency at low load, especially in wide range mains applications.

When operating, the current consumption (of the device only, not considering the gate drive current) rises to a value depending on the operating conditions but never exceeding 4.5mA.

The device keeps on working as long as the supply voltage is over the UVLO threshold (10.3V max).

If the Vcc voltage exceeds 18V an internal zener diode, 30 mA rated, will be activated in order to clamp the voltage. In that case the power consumption of the device will increase considerably.

PRACTICAL DESIGN EXAMPLE

To fix the main concepts, here below the wide range demonstration board design is described and the results of the board evaluation are presented.

The target specifications are summarised in table1. To meet them an appropriate selection, especially as to critical components, is an important step.

Table 1. Wide Range PFC Target Specification.

AC mains RMS voltage	V_{irms} = 85 to 265V
DC output regulated voltage	V_o = 400V
Rated output power	P_o = 80W
Minimum switching frequency	$f_{sw(min)}$ > 20kHz
Expected efficiency	η > 90%
Full load output voltage ripple	$\Delta V_o \leq \pm 10V$
Maximum output overvoltage	ΔV_{OVP} = 40V

POWER MOSFET:

Two parameters are useful to select the suitable device: the minimum blocking voltage $V_{(BR)DSS}$ and the R_{DSON} because of power dissipation.

The device selected is the STP8NA50 ($V_{(BR)DSS}$ = 500V, R_{DSON} = 0.85Ω @ 25°C, 1.5Ω @ 100°C). The estimated power dissipations are 1.3 W for conduction, and 0.2 W total switching losses (crossover + capacitive).

BOOST DIODE (D1):

Fast recovery diode suitable for rated breakdown voltage are used on demoboards. The plastic axial package BYT13-600 has been selected. The power dissipation is about 0.2W.

BOOST INDUCTOR (T):

The inductance value (L) is as high as 0.8 mH, which leads to a minimum switching frequency of 40kHz.

The minimum core size estimate gives a minimum volume of 3.3 cm^3. Considering the ETD series, the ETD29x16x10 core (5.4 cm^3 effective volume) is to be selected.

To reduce copper losses, a multiple wire (10 x 0.2mm) has been adopted. The resistance of the winding is about 1Ω at 40 kHz , so the maximum copper losses are about 1.1 W.

OUTPUT FILTER CAPACITOR (C5):

The specification on the output voltage ripple determines the capacitance value.

Assuming 50 Hz minimum line frequency, a 47µF/450V capacitor has been selected. This gives an output ripple ΔVo = ±7 V.

MULTIPLIER SETTING (R9 AND R10) AND SENSE RESISTOR (R6):

The multiplier divider is selected so to exploit all its linear dynamics ($V_{MULTpkx}$ = 3V) as per the procedure described in pin 3 description. The sense resistor is then determined.

As to R6, metallic film resistors are suitable because of the high peak current flowing in it.

OUTPUT DIVIDER (R7 AND R8):

R7 is selected so to achieve the desired overvoltage trip level (ΔV_{OVP} = 40V), while R8 is chosen so to get the specified output regulated voltage.

The schematic circuit of fig. 13 shows the values of all the parts used. In fig. 14 the printed circuit board and the component layout of the demonstration board are shown.

Figure 13. Wide Range Demonstration Board Electrical Circuit.

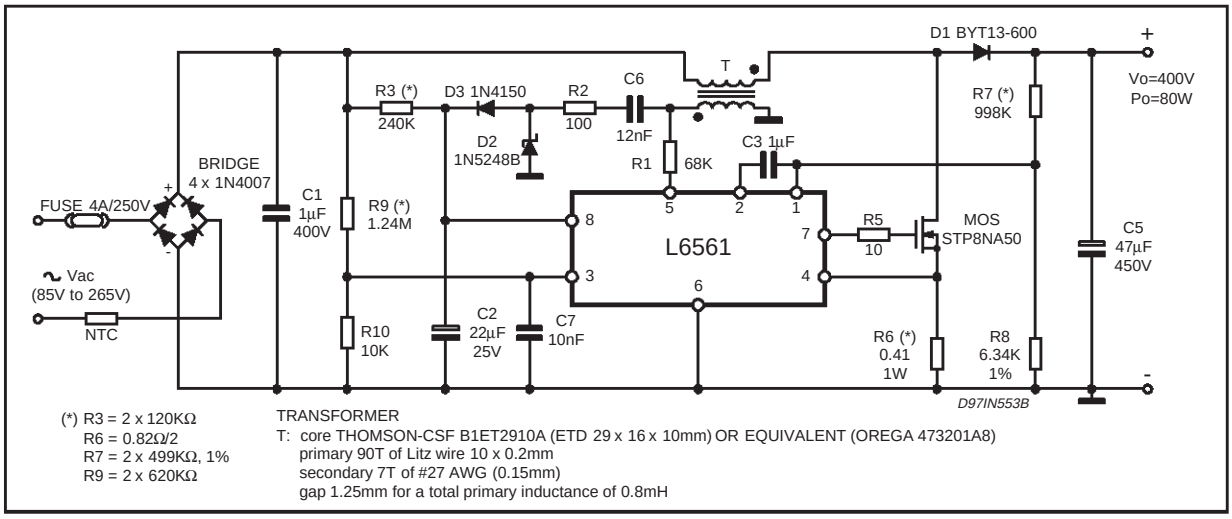
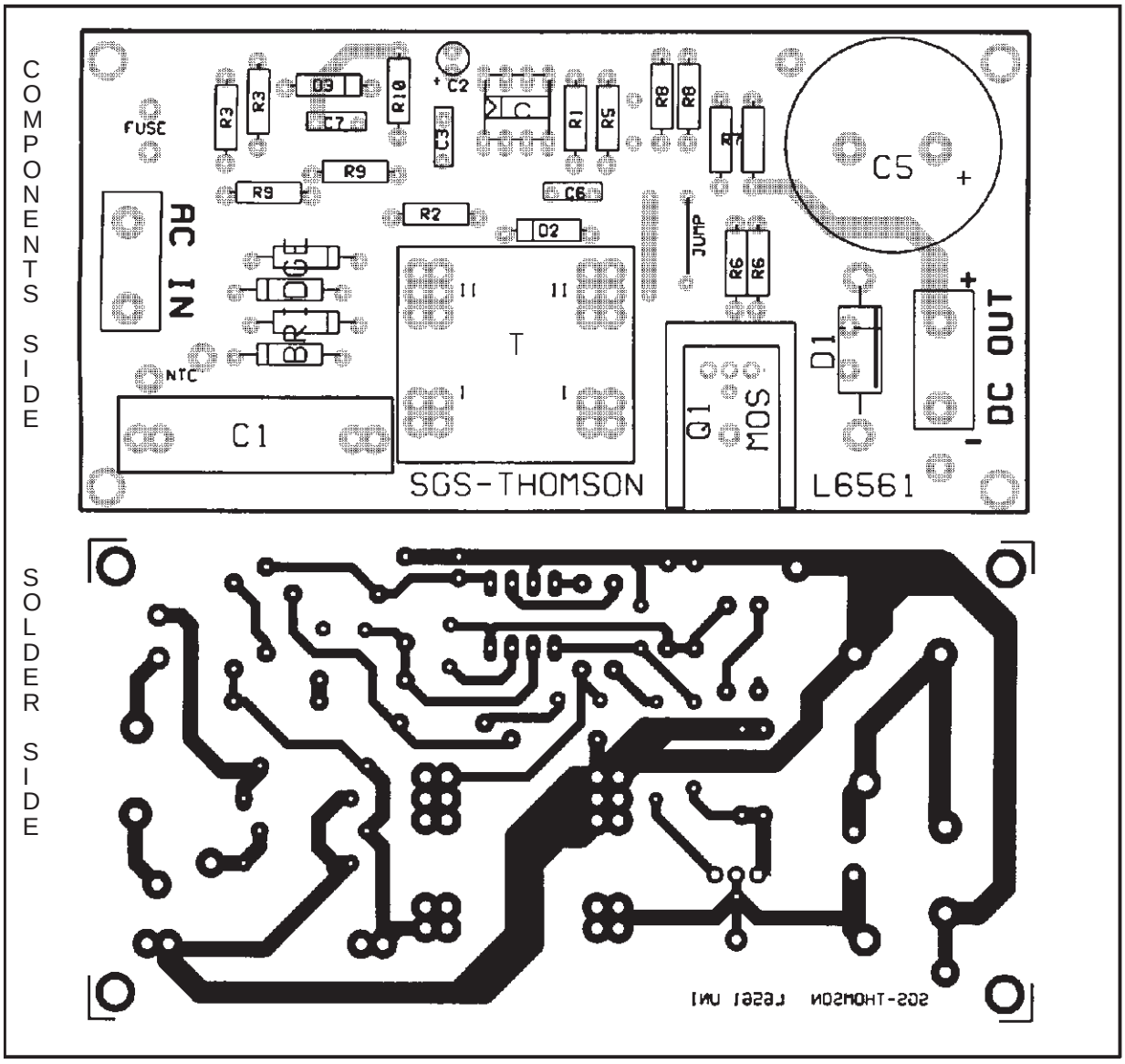


Table 2. Demonstration Board Evaluation Results.

V_{in} (Vac)	Pin (W)	V_o (Vdc)	ΔV_o (Vdc)	P_o (W)	η (%)	PF	THD (%)
85	89.8	399.7	14	82.5	91.9	0.999	4.9
110	88.4	399.8	14	82.6	93.4	0.998	5.9
135	87.4	399.8	14	82.6	94.5	0.995	6.8
175	87.1	399.8	14	82.6	94.8	0.988	7.9
220	86.8	399.8	14	82.6	95.1	0.977	8.8
265	86.6	399.8	14	82.6	95.3	0.972	9.8

Figure 14. P.C. Board and Components Layout of the Fig. 13 (1:1.25 scale)



DEMO BOARD EVALUATION RESULTS

To evaluate the performance of the PFC demonstration board, the following parameters have been measured: PF(Power Factor), THD%(Current Total Harmonic Distortion), ΔVo (Peak-to-Peak Output Voltage Ripple), Vo (Output Voltage), h (Efficiency).

The test equipment set-up is shown in fig. 15 and the results are shown in table 2.

The harmonic content measurement has been done with an EMI/RFI filter interposed between the AC source and the demo board under test, while the efficiency has been calculated without the filter contribution. The filter is configured as shown in fig. 16, where:

T1 = 1mH, T2 = 27mH, Cx = 0.47µF / 630V, Cy = 2.2nF / 630V

Figure 15. Test Equipment Set-up

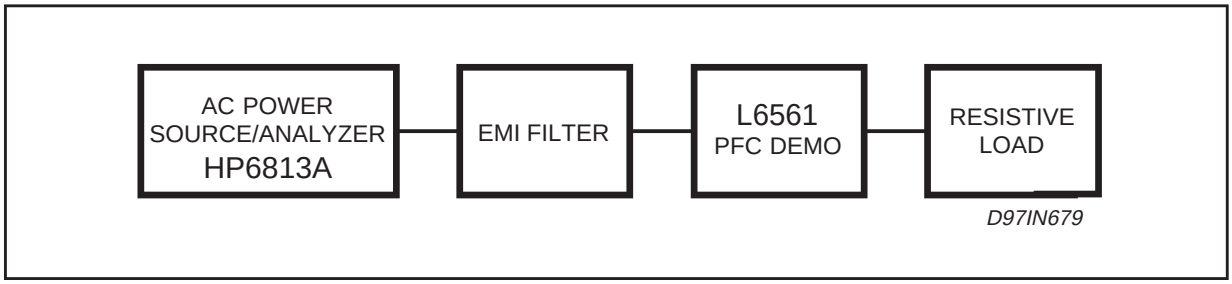
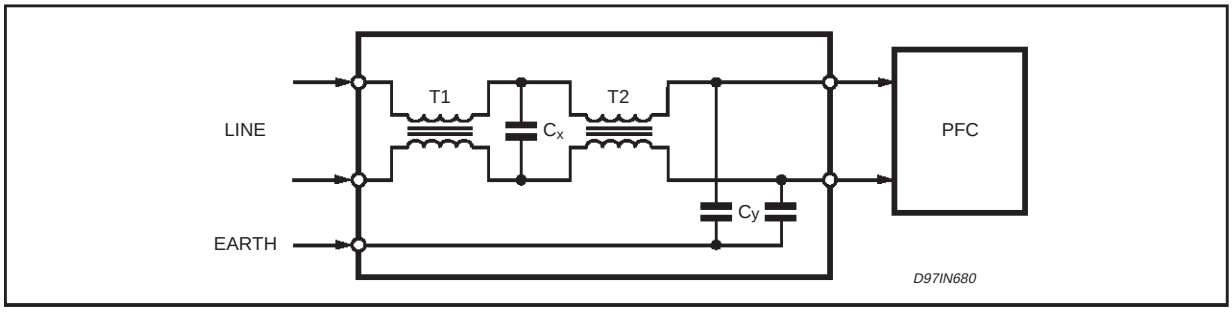


Figure 16. EMI Filter Configuration



APPLICATION IDEAS

The L6561 is a versatile device. Besides the typical application as a PFC preregulator based on boost topology, it fits also other applications and/or topologies. Some application hints are given in the following.

Figure 17. Wide Range 50W PFC, Flyback Topology.

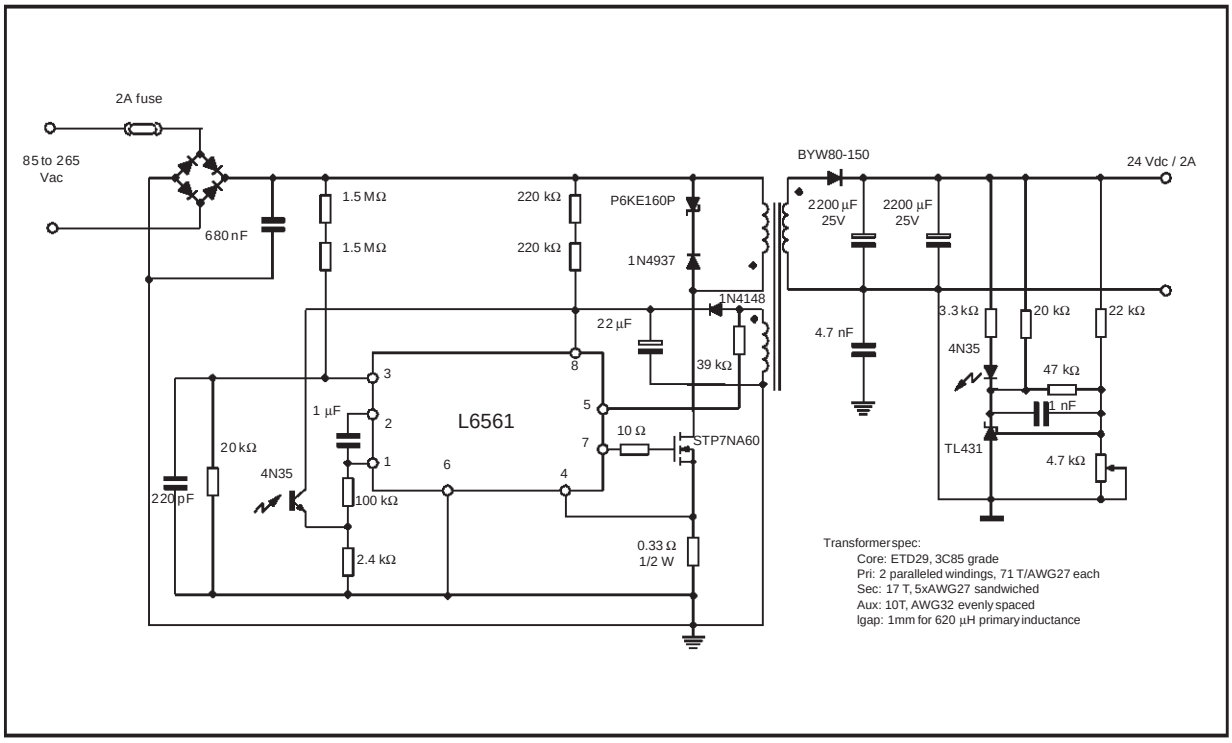


Figure 18. Power Factor Corrected Lamp Ballast using the L6569 driver.

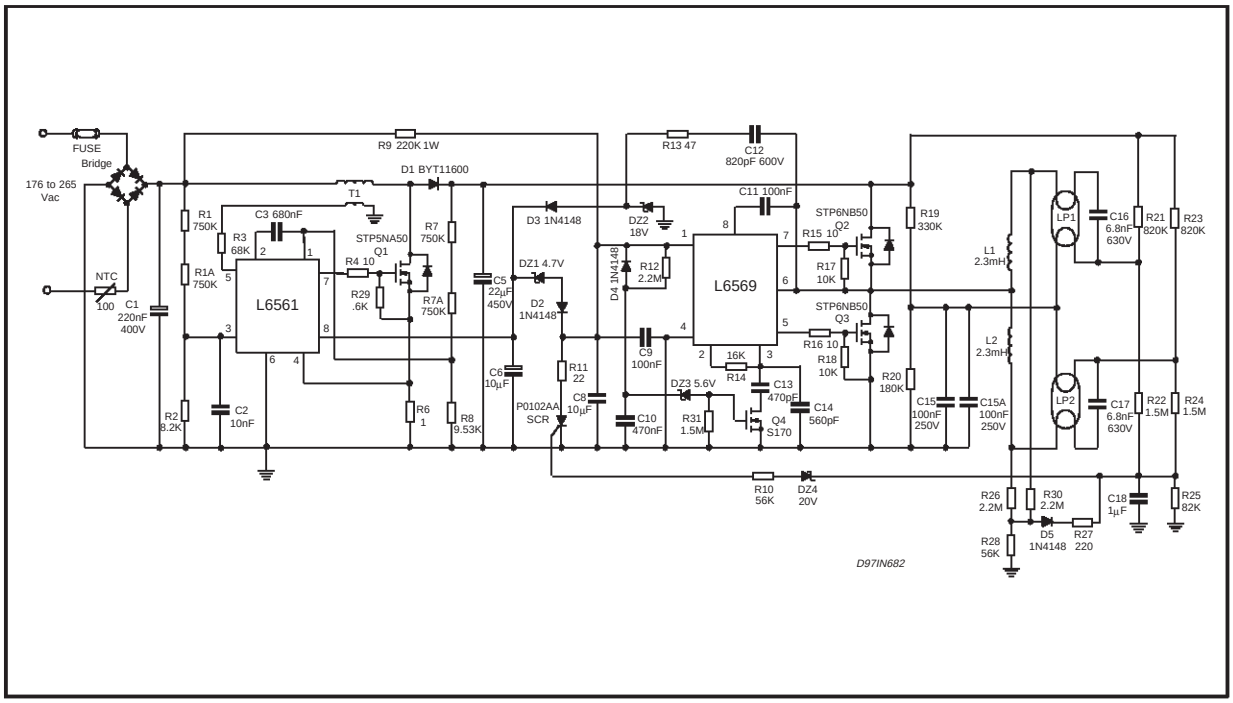
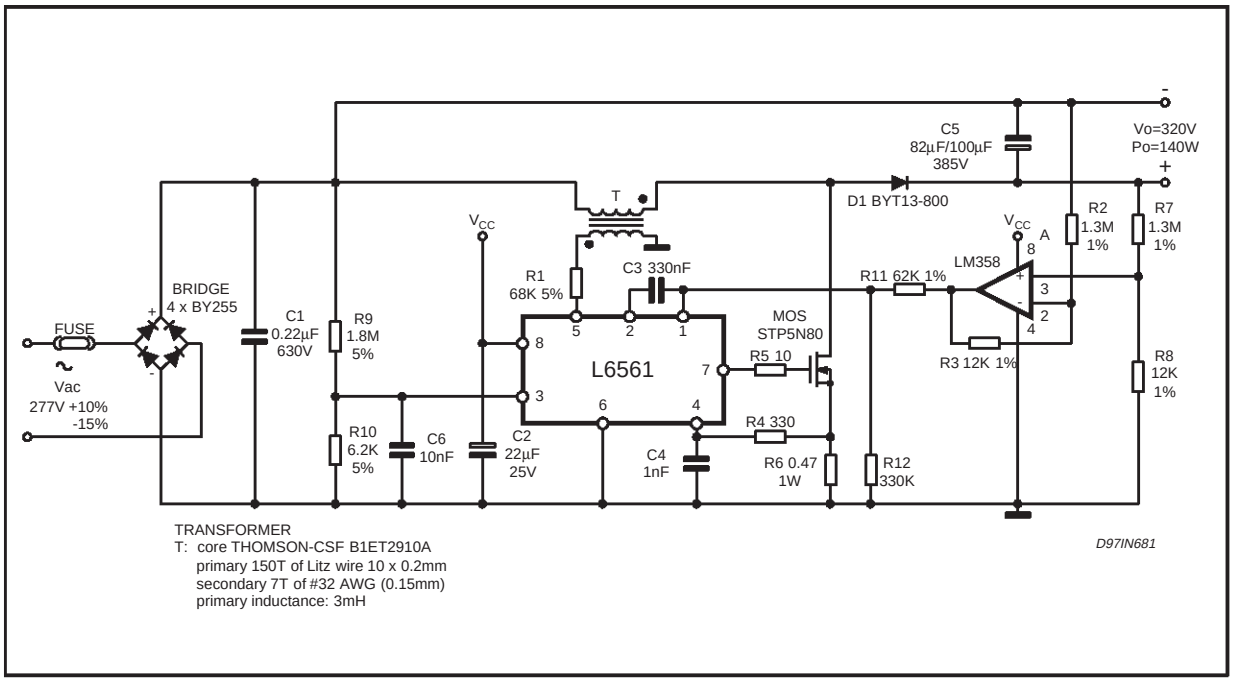


Figure 19. Vmains=277 Vac, Vo=320V, Po=140W buck-boost topology



REFERENCE:

[1] "Control loop modelling of L6561-based TH PFC" (AN1089).