

## ST75C520 REVISION 1.4

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## I - INTRODUCTION

The purpose of this document is helping the customer to use the Revision 1.4 of the ST75C520. So the ST75C520 Revision 1.4 Application Guide answers some questions as :

- are there some software differences between Revision 1.3 and Revision 1.4 ?
- what kind of problem the Revision 1.4 resolves and what kind of problem still remains ?
- what do I have to do with the Revision 1.4 if I want to bypass some problems I used to have with the Revision 1.3 ?

To answer those questions, SGS THOMSON proposes to the ST75C520 users two annotated lists :

- The ST75C520 DSP Code Update
- The ST75C520 Host Patch List

In the first list are described problems the customer may have been faced with. For those problems, SGS-THOMSON proposes a "Problem Fixing Status" which indicates whether a solution has been proposed or not. There are two kinds of solution. The first one is a sequence of commands the customer has to add in his application in order to bypass the problem. Generally, that solution is only valid for a specified revision of the ST75C520. All the informations the customer needs are gathered in the **ST75C520 Host Patch List** and the **ST75C520 DSP Code Update**. In that case, the Problem Fixing status is Patch xx, where xx is the

reference of the solution in the host patch list. The second kind of solution is a DSP sequence directly added in the Revision 1.4 of the DSP program. In that case, the Problem Fixing status is **Revision 1.4**. If no solution is yet proposed by SGS-THOMSON, the Problem Fixing status is —.

If the customer wants to use the Revision 1.4 of the ST75C520 and wants a problem to be solved, he checks a **Patch xx** or a **Revision 1.4** in the Problem Fixing Status box of the paragraph which describes that problem. If a **patch xx** is only indicated, the problem has not been corrected in the DSP code of Revision 1.4. So the customer will have to keep the sequence proposed in the **HPxx** reference of the host patch list. If a **Revision 1.4** is indicated in the Problem Fixing Status box, a solution for that problem has been implemented in the DSP code and thus the customer **MUST DELETE THE SEQUENCE HE USED WITH THE REVISION 1.2 or 1.3**. In other words the sequence proposed by SGS-THOMSON for Revision 1.2 or 1.3 is no longer required for Revision 1.4. We know that it will take some time for the customer to make his software compatible with the Revision 1.4 of the ST75C520. But in the other hand, the updated software will be more efficient and concise than the old one. We hope this guide will help you to achieve that goal.

Sincerely, the application team

## II - DSP CODE HISTORY

Since the first prototype in 1993, the ST75C520 DSP Code deeply changed. And the purpose of this part is to sum up the major differences which occurred between the three industrialized versions 1.2, 1.3 and 1.4.

### II.1 - Differences between ST75C520 Revision 1.2 and Revision 1.3

Apart from the two new features the Revision 1.3 offers (see below), there are no differences in term of problem solving between Revision 1.2 and 1.3.

#### II.1.1 - Transmit HDLC

Three new global variables have been added in the Revision 1.3 to allow the programming of new 7E flags before the first frame, between the data frames and after the last frame :

- `_NHFBF`: Number of flags before the first frame.
- `_NHFCF`: Number of flags between frames.
- `_NHFST`: Number of flags after the last frame.

The default value for these three variables is 0. The programming range is from 0 to 7FFF (32767) (see Figure 1).

These new variables are set to zero after a RESET or a **INIT** command. They can be overwritten at any time.

The absolute addresses in Rev 1.3 are:

- `_NHFBF` —> 0x17E2
- `_NHFCF` —> 0x17E3
- `_NHFST` —> 0x17E4

#### II.1.2 - Received HDLC

A new global variable `_RXCRC` copies the CRC of each received HDLC frame (it is valid until the end

of the current frame). The Receive CRC can be optionally read with a **MR** command or by programming two optional status bytes with the **DOSR** command.

Four new bytes are allocated inside the DUAL RAM space for the storage of the received CRC :

Address (Hexa)	Description	Size (Byte)	Mnemonic
\$18..\$19	CRC Rx Buffer 0	2,00	RXCRC0
\$1A..\$1B	CRC Rx Buffer 1	2,00	RXCRC1

If a new global variable called `_FLAGCRC` has a value different from zero, each time the ST75C520 writes the Receive Data in the one of the Receive buffer, it copies the received CRC into the DUAL RAM location `RXCRC0` (associated with `DRTBF0`) or `RXCRC1` (associated with `DTRBF1`). These bytes must be read when the bit `BUFF_EFRM` is set in the corresponding `DTRBSx` Byte (see Figure 2).

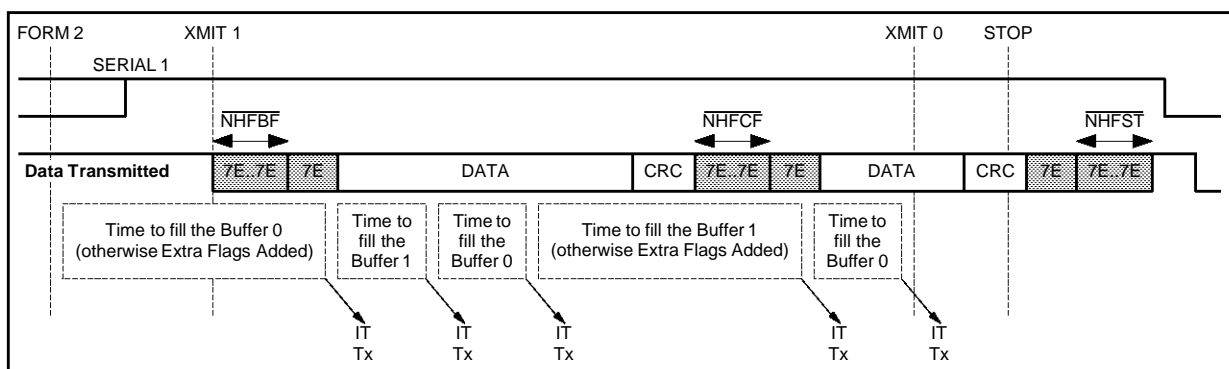
These variables are set to zero after a RESET or a **INIT** command and can be overwritten at any time.

The absolute addresses in Revision 1.3 are:

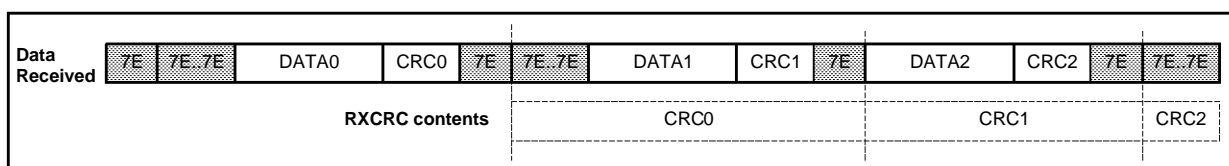
- `_FLAGCRC`: 0x17E7
- `_RXCRC`: 0x17E9

Remark : due to the time difference between the update of the Optional Status Words and the Receive Buffer mechanism, it is mandatory (if using the **DOSR** command to read the Received CRC) to wait 0.5ms after the `BUFF_EFRM` before reading the Optional Status Words.

**Figure 1 : Detailed Timing Diagram**



**Figure 2 : Detailed Timing Diagram**



## II - DSP CODE HISTORY (continued)

### II.2 - Differences between ST75C520 Revision 1.3 and Revision 1.4

The Revision 1.4 has been created to correct most of the Revision 1.3 problems in the DSP code. The software modification mandatory for Revision 1.4 are described in the **ST75C520 Rev 1.4 Code Update**.

#### II.2.1 - RAM Mapping

No Modification of the RAM Mapping between the revision 1.2, 1.3 and 1.4; all new variables have been added at the end of the memory.

#### II.2.2 - How to check the Software and Hardware Version of a ST75C520 chip ?

If you want to know what version of software version you are working with, we would like to remind you with the **IDT** command described page 21/ 44 in the ST75C520 databook.

If you send the IDT command to the Dual Port Ram, you will get in the COMREP[0] the DSP software number, and in the COMREP[1] the hardware reference (cf. page 28/ 44 in the ST75C520 databook.). But for that, you will have to wait for one of the three DSP acknowledgement (IT6, COMSYS = 0 or a new COMACK value).

For example, you can have :

0001 0010 in COMREP[0] → it means DSP soft Revision 1.2

0010 0000 in COMREP[1] → it means hardware reference = 2

## III - HOW TO USE THE ST75C520 CODE UPDATE

All the problems discovered by SGS-THOMSON are referenced by using the following structure :

Px	Name	Date of Discovery	Problem Appearance	Problem Fixing Status
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#### Description

The nature of the problem is described.

#### Condition

The problem's conditions of appearance are explained.

#### Consequence

Major consequences the problem leads to are precised.

#### Probability

When it is known, we precise the occurrence of the problem and we choose a severity status (cf. color code below).

#### Patch

SGS-THOMSON describes if some technical solution has been found to bypass the problem.

There are three possibilities for the **Problem Fixing Status** box :

- **Patch x** : a sequence HPx is proposed to bypass the problem.
- **Revision 1.x** : the problem is fixed in revision 1.x of the ST75C520.
- **for info** : the problem is described for customer information.
- **—** : there is no solution available to bypass the problem.
- **Patch included** : the host patch is described with the problem.

So there is no reference to the Host Patch list.

In parallel, you will find a color code on the numbering box to show the evaluated severity of the bug. This code is explained below.

The bug has to be corrected

The bug should be corrected for safety

The bug has few consequences on your application

All the host patches validated by the design are referenced by using the following structure :

HPx	Name	Date of Release	Revision 1.X	Pb corrected (Numbers)
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#### Host Patch Description

Description of the patch suitable for the revision 1.X release.

## ST75C520 REVISION 1.4

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### IV - PROBLEM LIST SUMMARY

P1	Slicer V17 B1 sequence	June, 96	Revision 1.2	Revision 1.4
P2	Timing recovery	June, 96	Revision 1.2	Revision 1.4
P3	V17 Fast Training	June, 96	Revision 1.2	Revision 1.4 or Patch 1
P4	Calcul of _SPEED variable	June, 96	Revision 1.2	Revision 1.4 or Patch 1
P5	Clearing of Input Samples	June, 96	Revision 1.2	Revision 1.4
P6	DTMF Detection	June, 96	Revision 1.2	Revision 1.4
P7	Time Recovery	June, 96	Revision 1.2	Revision 1.4 or Patch 3
P8	V29 False Lock detection routine	June, 96	Revision 1.2	Revision 1.4 or Patch 3
P9	DPLL for V21ch2	June, 96	Revision 1.2	Revision 1.4 or Patch 4
P10	V17 problem with AGC unfrozen	June, 96	Revision 1.2	Revision 1.4 or Patch 1
P11	STOP command in HDLC mode	June, 96	Revision 1.2	for info
P12	FSK Demodulator Bug (1)	Oct 18, 96	Revision 1.2	—
P13	FSK Demodulator Bug (2)	Oct 96	Revision 1.2	—
P14	HDLC long data frames	Oct 18, 96	Revision 1.2	Patch 2
P15	RING Polarity	Oct 96	Revision 1.2	—
P16	Various amplitude in V17	Sept 9, 96	Revision 1.2	for info
P17	V17 compatibility vs Rockwell ...	Sept 18, 96	Revision 1.2	Patch included
P18	Decimator failure after Reset	Sept 21, 96	Revision 1.4	Patch included
P19	JAPAN Line distorsion	Feb 1, 96	Revision 1.2	Patch 5

### V - HOST PATCH LIST SUMMARY

HP1	Sequence D	June, 96	Revision 1.2, 1.3	p3, p4, p10
HP2	HDLC 4Kb data lengh	Oct 24, 96	Revision 1.2 to 1.4	p14
HP3	Sequence for impulse noise	June 13, 96	Revision 1.2 to 1.4	p7, p8
HP4	DPLL control for V21 RX	June 4, 96	Revision 1.2 to 1.4	p9
HP5	JAPAN Line patch	Feb 1, 96	Revision 1.2 to 1.4	p19

**VI - DSP CODE UPDATE**

In this document is listed all the known problems discovered by SGS THOMSON. The correction of some of these problems are listed in the **ST75C520 Host Patch List**.

P1	Slicer V17 B1 sequence	June, 96	Revision 1.2	Revision 1.4
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**Description**

Slicer V17 B1 sequence needs to be 132, 68, 36, 20 points for fast training to avoid phase error in data mode entry.

**Conditions**

SNR at approximatively -25dB.

**Consequence**

Degradation of Phase C success rate.

**Probability**

1/200 of Phase C failure. Severity : LOW

**Patch**

No host path available.

P2	Timing recovery	June, 96	Revision 1.2	Revision 1.4
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**Description**

In the calcul of T2 value, the timing recovery can potentially fail when the number  $y/x$  is greater than 1.

**Conditions**

Some x and y values in the DSP. Never seen with the ST75C520 test card in any application.

**Consequence**

Potential degradation of Phase C success rate.

**Probability**

Less than 1/ 10 000. Severity : Very LOW

**Patch**

No host patch available.

P3	V17 Fast Training	June, 96	Revision 1.2	Revision 1.4 or Patch 1
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**Description**

A slightly modified sequence is necessary for V17 Fast Training (some DSP parameters have to be modified : \_RX\_STA, \_RXSTWRD, K2, K1INC, K2INC, BETATRAK, EQFROZ, AGCFROZ).

**Conditions**

Any value of SNR.

**Consequence**

Degradation of Phase C success rate.

**Probability**

Unknown. Severity : MEDIUM

**Patch**

See host patch number 1.

**VI - DSP CODE UPDATE (continued)**

P4	Calcul of _SPEED variable	June, 96	Revision 1.2	Revision 1.4 or Patch 1
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**Description**

The DSP sometimes calculates its internal variable \_SPEED with an error.

**Conditions**

Depends on relative phase of receive sample clock compared to that of the local oscillator at the end of Rate sequence detection during training.

**Consequence**

Degradation of Phase C success rate.

**Probability**

1/200 of TCF or Phase C. Severity : LOW.

**Patch**

See host patch number 1.

P5	Clearing of Input Samples	June, 96	Revision 1.2	Revision 1.4
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**Description**

The input samples are not properly cleared when the Carrier Detect is lost in m\_fax routine.

**Conditions**

No specific condition of noise or signal level.

**Consequence**

Potential drift of the equalizer coefficients.

**Probability**

Very low. Severity : Very LOW.

**Patch**

No host patch available.

P6	DTMF Detection	June, 96	Revision 1.2	Revision 1.4
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**Description**

The DTMF detection needs to be modified to increase the voice immunity. There are limitations to DTMF detection when DTMF frequencies are shifted and when DTMF level is around -20dBm (RXA pins).

**Conditions**

"Polish Tape" Voice Immunity Test (35mn). DTMF with +/-1.5% of frequency offset or -20dBm at RXA pins (a Test Report is available).

**Consequence**

80 false DTMF detections ("Polish Tape"). False digits or no digits detections (depend on the conditions).

**Probability**

See "consequence". Severity : HIGH.

**Patch**

See host patch number 6.

**VI - DSP CODE UPDATE (continued)**

P7	Time Recovery	June, 96	Revision 1.2	Revision 1.4 or Patch 3
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**Description**

The timing recovery in V27 ter 4800 and 2400bps can diverge.

**Conditions**

High impulse noise or gain hit higher than 20dB on the line.

**Consequence**

Transmission loss in V27 ter 4800 and 2400bps.

**Probability**

Unknown. Severity : LOW.

**Patch**

See host patch number 3.

P8	V29 False Lock detection routine	June, 96	Revision 1.2	Revision 1.4 or Patch 3
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**Description**

The receiver's V29 False Lock detection routine is inactive if EQ or AGC are frozen.

**Conditions**

EQ or AGC frozen and high impulse noise or gain hit higher than 20dB.

**Consequence**

Transmission loss in V29.

**Probability**

Unknown. Severity : LOW.

**Patch**

See host patch number 3.

P9	DPLL for V21ch2	June, 96	Revision 1.2	Revision 1.4 or Patch 4
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**Description**

The DPLL used for V21 channel 2 has a drift problem.

**Conditions**

The received data are only "0" (resp. "1").

**Consequence**

Extra or loss of zeros (resp. ones) while receiving in HDLC mode.

**Probability**

2/1000 RX\_CLOCK drift problems. Severity : MEDIUM.

**Patch**

See host patch number 4.

P10	V17 problem with AGC unfrozen	June, 96	Revision 1.2	Revision 1.4 or Patch 1
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**Description**

In Phase C, if the user unfreezes the AGC, the value of the analog gain swings by a factor of 8% between segment P2 and PN, causing the data constellation to collapse.

**Conditions**

AGC algorithm unfrozen during V17 Phase C.

**Consequence**

Broken Phase C.

**Probability**

Always. Severity : HIGH in those conditions.

**VI - DSP CODE UPDATE** (continued)**Patch**

See host patch number 1.

P11	STOP command in HDLC mode	June, 96	Revision 1.2	for info
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**Description**

In HDLC mode, if the STOP command occurs while you are not sending a frame, the \_NHFST flags are not transmitted.

Only \_NHFCF are sent. But on the contrary if you are still feeding the buffers and a STOP command occurs, then \_NHFST flags are transmitted instead of \_NHFCF between adjacent frames.

**Conditions**

STOP command sent long time after the last buffer feeding.

**Consequence**

For information only

**Probability**

Not defined. Severity : LOW.

P12	FSK Demodulator Bug (1)	Oct 18, 96	Revision 1.2	—
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**Description**

The FSK Demodulator has a bug for parallel mode. When RX\_BIT routine is called in fskrx.asm, the BSC register (which contains the EDGSHFT value) is destroyed. Because the RX\_BIT routine is called every 8 samples, you get a high bit rate error.

**Conditions**

FSK demodulation (V23) in parallel mode.

**Consequence**

V23 1200bps receiver not functional.

**Probability**

Always in those conditions. Severity : HIGH.

**Patch**

No patch available.

P13	FSK Demodulator Bug (2)	Oct 96	Revision 1.2	—
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**Description**

The calculation of the sample clock is shifted by one sample, giving a bad centering (-5, +3 instead of -4, +4). The fix consists in incrementing MODULO and testing for zero, instead of calling RX\_BIT routine before testing zero.

**Conditions**

FSK demodulation (V23).

**Consequence**

A high bit rate error.

**Probability**

Always. Severity : HIGH.

**Patch**

No patch available.



**VI - DSP CODE UPDATE (continued)**

P14	HDLC long data frames	Oct 18, 96	Revision 1.2	Patch 2
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**Description**

The frame length you can receive in HDLC mode must be shorter than 4Kbytes, otherwise an unpredictable error (Abort Frame) can be return in the STATUS word (see conditions). This is due to an internal bit counter (RXCTBIT) that wrap around when it comes near 32767.

**Conditions**

HDLC reception with data length greater or equal than 32760 bytes in all modes except V17 9600, V29 9600, V29 4800 and V27ter 4800.

**Consequence**

The oversized frame is lost.

**Probability**

Always in those conditions. Severity : MEDIUM.

**Patch**

See host patch number 2.

P15	RING Polarity	Oct 96	Revision 1.2	—
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**Description**

The RING polarity is correct for WakeUp but inverted for the RING detector because that detector is updated on the rising edge of the RING pin instead of the falling edge. If the SLEEP mode is not used, the detection time (STA\_RING set to 1) is either 0.5 or 1.5 a RING period.

**Conditions**

SLEEP mode used.

**Consequence**

An additional RING period is needed.

**Probability**

Always in those conditions. Severity : MEDIUM.

**Patch**

No host patch available.

P16	Various amplitude in V17	Sept 9, 96	Revision 1.2	for info
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**Description**

With very high level of noise in V17, if you want to handle various amplitude between TCF and Phase C, the data could collapse. This is due to the fact that there is no feedback between the equaliser error and the AGC.

**Conditions**

Various amplitude between TCF and Phase C in V17 mode with very high level of noise. AGC unfrozen.

**Consequence**

Data collapsing.

**Probability**

Potential. Severity : LOW.

**VI - DSP CODE UPDATE (continued)**

P17	V17 compatibility vs Rockwell ...	Sept 18, 96	Revision 1.2	Patch included
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**Description**

When using Rockwell V34 Data Pump in V17 FAX mode, AGC is jumping at the end of the TCF sequence. The following Phase C could collapse.

**Conditions**

V17 FAX mode versus a V34 Rockwell Data Pump. AGC unfrozen.

**Consequence**

Phase C collapsing.

**Probability**

Always. Severity : LOW.

**Patch**

Write MW 96 15 FF 7F (NORMTHSH) 2ms after the SYNC 1 command (this MW command is already included in the patch 1).

P18	Decimator failure after Reset	Sept 21, 96	Revision 1.4	Patch included
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**Description**

After a RESET (or INIT or SLEEP command), the decimator (9.6 to 7.2KHz) is not correctly initialised : instead of taking four samples as input, it takes one.

**Conditions**

After a RESET or INIT or SLEEP command.

**Consequence**

The Tone mode do not work properly.

**Probability**

Unknown. Severity : HIGH.

**Patch**

Send CONF 00 00 after INIT for the Tone mode (it is mandatory for Revision 1.4 and compatible for all the previous revisions).

P19	JAPAN Line distorsion	Feb 1, 96	Revision 1.2	Patch 5
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**Description**

On JAPAN lines, the TPG (Group Delay) is asymmetrical between 600Hz and 3000Hz. And thus some wrong "dots" can appear at the top of received pages. That problem is related to the Timing Recovery algorithm.

**Conditions**

Fax transmission on japanese telephone lines.

**Consequence**

Wrong "dots" at the top of received pages.

**Probability**

Unknown. Severity : LOW.

**Patch**

See host patch number 5.

## VII - HOST PATCH LIST

In the list below are described the host patches validated by SGS THOMSON to bypass some specific problems. the structure of that document is explain in the application notice How to use the ST75C520 Code Update.

HP1	Sequence D	June, 96	Revision 1.2, 1.3	p3, p4, p10
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### Host Patch Description

That CPU sequence is known as "Sequence D". It is used to solve V17 reception problems with Revision 1.2 and 1.3 (that sequence has been implemented in the Revision 1.4 and must not be used with that revision). There are two parts : the first for the TCF frame, the second for the short train reception.

TCF CONF V17

SYNC 1

**Wait 2ms**

MW 99 15 1F 00 /\* set AGC adaptation slow step size to a very high time constant (BETATRAK)\*/

MW F8 15 00 00 /\* K1 inc \*/

MW F9 15 00 00

MW FA 15 00 00 /\* K2 inc \*/

MW FB 15 00 00

MW 96 15 FF 7F /\* CONVTHSH \*/

**Wait P2s**

**Wait 40ms** /\* from 21 to 60ms \*/

MW 15 10 13 00 /\* AGC slow mode (\_RX\_STA) \*/

**Wait STA\_109 = 1**/\* wait carrier detect \*/

**Wait 0.6s** /\* This is "T1" time \*/ (\*\*)

MW 55 16 1F 00 /\* alpha \*/

MW F5 15 00 00 /\* K1 \*/

MW F4 15 00 00

**Wait 0.5s** /\* This is "T2" time \*/ (\*\*\*)

MW 15 10 05 00 /\* freeze AGC and equalizer (\_RX\_STA) \*/

(\*\*) In case of short data time for TCF (200ms instead of 1.5s), the minimum wait here is 130ms (256 bauds + 50 for margin). An additional command **MW E3 16 XX YY** is necessary immediatly after T1 to shorten the data mode. YY XX is a number of bauds given in hexadecimal value (SCNTR).The formula to calculate it is:

$$YY\ XX = \text{Hex} [ T2 / 0.417 ] \text{ (T1 and T2 times are defined in the sequence above)}$$

**N.B:** if T is the data time, you must have :  $T > (T1 + T2)$

**Example:** T1 = 130ms ; T2 = 20ms ; T = 200ms => YY XX = #30h

(\*\*\*) In case of short data time for TCF, the minimum wait here is 20ms.

### VII - HOST PATCH LIST (continued)

Phase C CONF V.17

MODC short train

SYNC 1

**Wait 2ms**

MW 99 15 1F 00 /\* set AGC adaptation slow step size to a very high time constant (BETATRAK)\*/

MW 12 10 08 00 /\* V17 14 400 \*/ (\*\*)

MW 15 10 1D 00 /\* \_RXSTA \*/

MW 20 17 55 00 /\* \_RXSTWRD \*/

MW 50 15 0B 00 /\* STEPSIZ \*/

MW F7 15 00 20 /\* K2 \*/

**Wait P2s**

MW 15 10 1B 00 /\* unfreeze AGC \*/

**Wait 40ms** /\* from 21 to 60ms \*/

MW 15 10 1F 00 /\* freeze AGC \*/

**Wait PNs**

MW 55 16 1F 00 /\* alpha \*/

MW F6 15 00 00 /\* K2\_lsb \*/

MW F7 15 00 00 /\* K2\_msb \*/

**Wait STA\_109 = 1** /\* wait carrier detect \*/

MW 55 16 04 00 /\* alpha \*/

MW F7 15 EA 06 /\* K2\_msb \*/

**Wait 110ms** /\* more than 256 bauds \*/

MW 15 10 05 00 /\* freeze equalizer and AGC \*/

(\*\*) the MW to use here depend on the V17 speed you want to use :

MW 12 10 08 00 /\* V17 14400 \*/

MW 12 10 07 00 /\* V17 12000 \*/

MW 12 10 06 00 /\* V17 9600 \*/

MW 12 10 05 00 /\* V17 7200 \*/

Remark : application sequence for a short data time reception with Revision 1.4

In that paragraph is described how configuring the ST75C520 Revision 1.4 for V17 short data time reception (from 200ms to 1.5s) :

CONF V17

SYNC 1 (\*\*)

**Wait STA\_109 = 1**

**Wait 130ms** /\* 256 bauds + 50 (margin) \*/

MW E3 16 XX YY /\* where YY XX is a number of bauds given in hexadecimal value (SCNTR) \*/

(\*\*) In case of short train instead of long train, an additional command must be written between CONF V17 and SYNC 1 : MODC short train

The formula to calculate the YY XX value is  $YY\ XX = \text{Hex} [ T2 / 0.417 ]$  (T1 and T2 times are defined in TCF part of P1 host patch)

N.B : if T is the data time, you must have :  $T > ( T1 + T2 )$

Example : T1 = 130ms ; T2 = 20ms ; T = 200ms => YY XX = #30h

**VII - HOST PATCH LIST** (continued)

HP2	HDLC 4Kb data lengh	Oct 24, 96	Revision 1.2 to 1.4	p14
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**Host Patch Description**

=> Lines to insert after the CONF command and the selection of the HDLC mode :

**DOSR 01 B7 96 00**

/\* write bit\_counter high byte in STAOPT1 \*/

=> Lines to insert while waiting for loss of Carrier Detect (end of data mode). But you can put them in any other places periodically read during the frame detection.

bit\_counter\_high\_byte= STAOPT1

if (bit\_counter\_high\_byte > 50h)

{ /\* test if bit\_counter is above #5000h (or 20480) \*/

**MW B7 16 00 04**

} /\* reset bit\_counter down to #0400 (or 1024) \*/

With that modification, you will be able to send HDLC frames with no limitation of data size. Because the bit counter will be kept away from #0000 and #7FFF limits.

HP3	Sequence for impulse noise	June 13, 96	Revision 1.2 to 1.4	p7, p8
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**Host Patch Description**

There is two different sequences for V29 and V27 ter modes. They should be useful too if the customer introduce short cuts of carrier during V29 or V27ter communications.

**V27 ter** CONF V.27ter

SYNC 1

MW E6 15 65 02 /\* K1ADR for timing recovery (COEF29) \*/

**Wait STA\_109 = 1**

**Wait 500ms (\*)(\*\*)**

MW 15 10 05 00 /\* RXSTA = EQ and AGC frozen \*/

MW 55 16 1F 00 /\* alpha \*/

MW F5 15 00 00 /\* K1 recovery\*/

**V29** CONF V.29

SYNC 1

**Wait STA\_109 = 1**

**Wait 500ms (\*)(\*\*)**

MW 15 10 05 00 /\* RXSTA = EQ and AGC frozen \*/

MW 55 16 1F 00 /\* alpha \*/

MW F5 15 00 00 /\* K1 recovery\*/

(\*) If you want to decrease this time you must use **MODC 01 00 00 00** command before SYNC 1. However, the DSP needs at least 256 bauds to compute the equalizer's coefficients after STA\_109 is set to 1.

(\*\*) If you are using the patch HP5, you will need to wait more than 4s. Because if you don't, you will see some compatibility problem.

Remark : in the Revision 1.4, the DSP software has a special algorithm to avoid rotation of the constellation in case of V29 9600. This algorithm was not always activated in Revision 1.2 and 1.3.

## VII - HOST PATCH LIST (continued)

HP4	DPLL control for V21 RX	June 4, 96	Revision 1.2 to 1.4	p9
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**Host Patch Description**

a) Temporary method for the Revision 1.2 and 1.3 (**only!**) :

Stop the DPLL with the **MW 10 10 99 00** command (\_CURMOD variable).

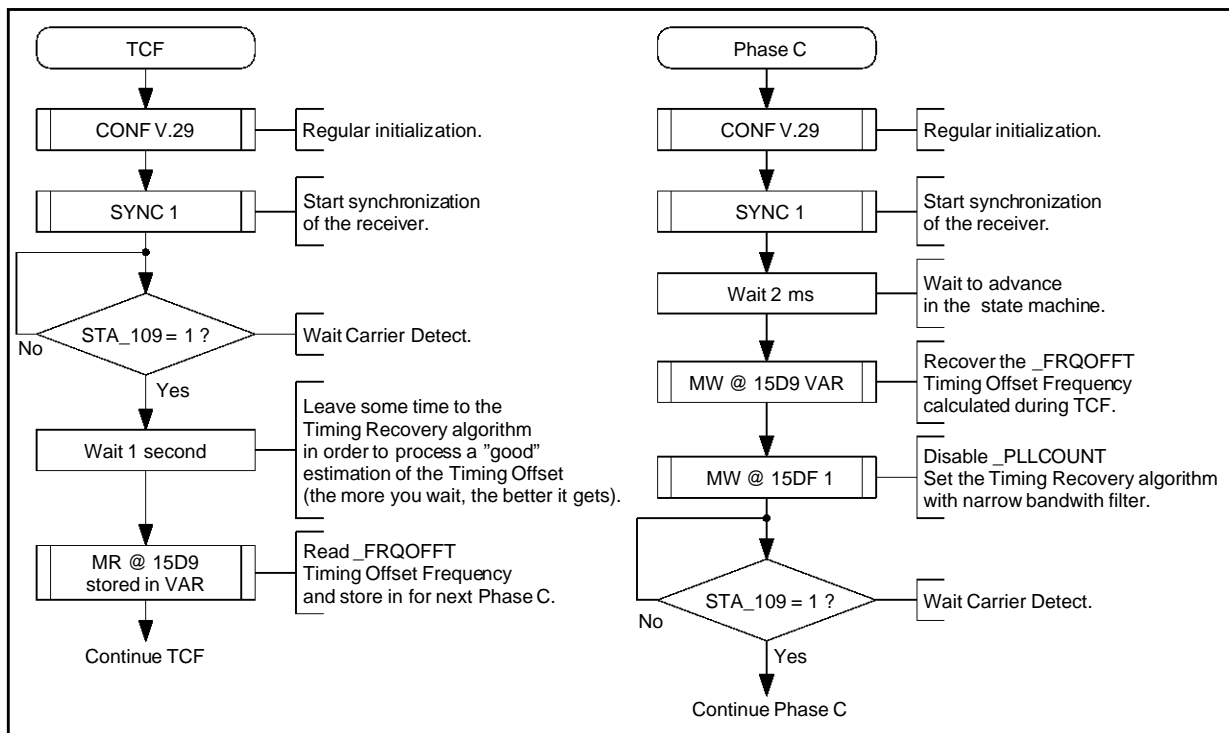
This MW command has to be written between CONF command and SYNC 1 command.

Remark : application feature for Revision 1.4

When detecting the continuous "0" data, the DSP stops automatically the DPLL. The number of continuous "0" after which the DSP stops the DPLL is programmable with \_NBZBYTES variable (adress 17F8) :

- \_NBZBYTES = 0 ———> the DSP always stops the DPLL (**default set up**)
- \_NBZBYTES = 1 ———> the DPLL stops after 8 bits equal to "0".
- \_NBZBYTES = 2 ———> the DPLL stops after 16 bits equal to "0".
- \_NBZBYTES = n ———> the DPLL stops after n x 8 bits equal to "0".

**Figure 3 : D**



HP5	JAPAN Line patch	Feb 1, 96	Revision 1.2 to 1.4	p19
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**Host Patch Description**

The sequence is described in the following flow chart.

## VII - HOST PATCH LIST (continued)

HP5	DTMF Detection patches	Dec 20, 96	Revision 1.2 to 1.4	p6
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**Host Patch Description for Revision 1.2 and 1.3**

Solution 1 : The Analog Gain Frozen mode :

**MW D2 17 02 00** analog gain frozen  
**CONF 04** DTMF detection enable

To keep the detection dynamic, you have to use the following sequence :

**MW EA 12 A5 0A** lowpass gain  
**MW 02 13 5E 65** hipass gain  
**MW 2E 12 E0 00** higher threshold for low pass filter  
**MW 2F 12 E0 00** higher threshold for high pass filter  
**MW 1A 13 8A 02** gain for 697Hz filter  
**MW 26 13 30 03** gain for 770Hz filter  
**MW 32 13 00 02** gain for 852Hz filter  
**MW 3E 13 40 04** gain for 941Hz filter

Solution 2 : The Analog Time Constant Low : in that mode, the time constant of the analog gain is lowered in order to avoid STA\_DTMF instability :

**CONF 04** DTMF detection enable  
**MW DE 17 00 F0** analog gain time constant low

**Host Patch Description for Revision 1.4**

Application patch :

Some Memory Writes have to be added after CONF command in order to meet the special requirements described in the ST75C520 Rev1.4 DTMF Detection Report. By default, Rev1.4 detects from -1dBm to -35dBm with a good speech immunity.

**MW 4A 13 89 05** 1dB attenuation for the 1209Hz filter  
**MW F2 17 00 14** comparaison threshold between 1209 and 1336Hz  
**MW F4 17 00 14** comparaison threshold between 1336 and 1477Hz  
**MW F5 17 00 14** comparaison threshold between 1336 and 1209Hz  
**MW 2E 12 60 00** lower threshold for low pass filter  
**MW 2F 12 60 00** lower threshold for high pass filter

Solution 1 to -20dBm problem : The AGC Frozen mode

**MW D2 17 02 00** analog gain frozen  
**CONF 04** DTMF detection enable

Solution 2 to -20dBm problem : The AGC Time Constant Low

**CONF 04** DTMF detection enable  
**MW DE 17 00 F0** analog gain time constant low

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