



INTRODUCTION TO SEMICONDUCTOR TECHNOLOGY

by Microcontroller Division Applications

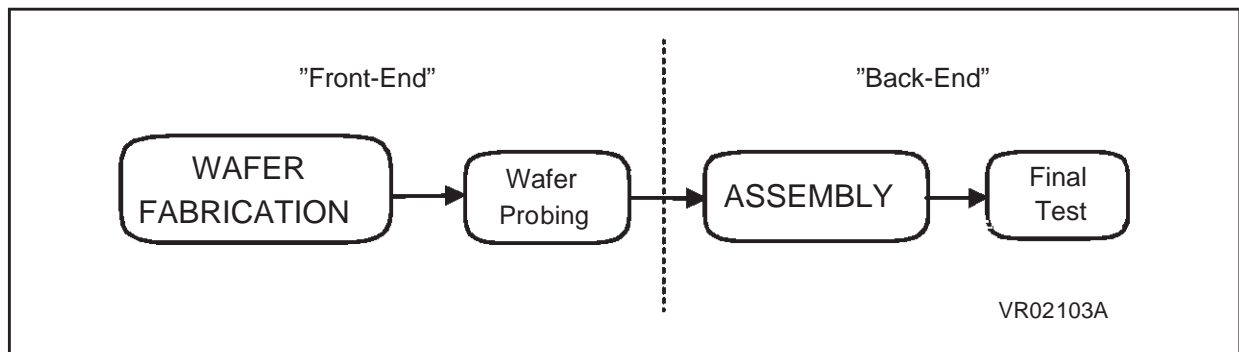
INTRODUCTION

An integrated circuit is a small but sophisticated device implementing several electronic functions. It is made up of two major parts: a tiny and very fragile silicon chip (die) and a package which is intended to protect the internal silicon chip and to provide users with a practical way of handling the component. This note describes the various “front-end” and “back-end” manufacturing processes and takes the transistor as an example, because it uses the MOS technology. Actually, this technology is used for the majority of the ICs manufactured at STMicroelectronics.

1 THE FABRICATION OF A SEMICONDUCTOR DEVICE

The **manufacturing phase** of an integrated circuit can be divided into **two steps**. The first, **wafer fabrication**, is the extremely sophisticated and intricate process of manufacturing the silicon chip. The second, **assembly**, is the highly precise and automated process of packaging the die. Those two phases are commonly known as “**Front-End**” and “**Back-End**”. They include two test steps: **wafer probing** and **final test**.

Figure 1. Manufacturing Flow Chart of an Integrated Circuit



1.1 WAFER FABRICATION (FRONT-END)

Identical integrated circuits, called **die**, are made on each wafer in a multi-step process. Each step adds a new layer to the wafer or modifies the existing one. These layers form the elements of the individual electronic circuits.

The main steps for the fabrication of a die are summarized in the following table. Some of them are repeated several times at different stages of the process. The order given here doesn't reflect the real order of fabrication process.

| | |
|---------------------------|--|
| PhotoMasking | This step shapes the different components. The principle is quite simple (see drawing on next page). Resin is put down on the wafer which is then exposed to light through a specific mask. The lightened part of the resin softens and is rinsed off with solvents (developing step). |
| Etching | This operation removes a thin film material. There are two different methods: wet (using a liquid or soluble compound) or dry (using a gaseous compound like oxygen or chlorine). |
| Diffusion | This step is used to introduce dopants inside the material or to grow a thin oxide layer onto the wafer. Wafers are inserted into a high temperature furnace (up to 1200 ° C) and doping gases penetrate the silicon or react with it to grow a silicon oxide layer. |
| Ionic Implantation | It allows to introduce a dopant at a given depth into the material using a high energy electron beam. |
| Metal Deposition | It allows the realization of electrical connections between the different cells of the integrated circuit and the outside. Two different methods are used to deposit the metal: evaporation or sputtering. |

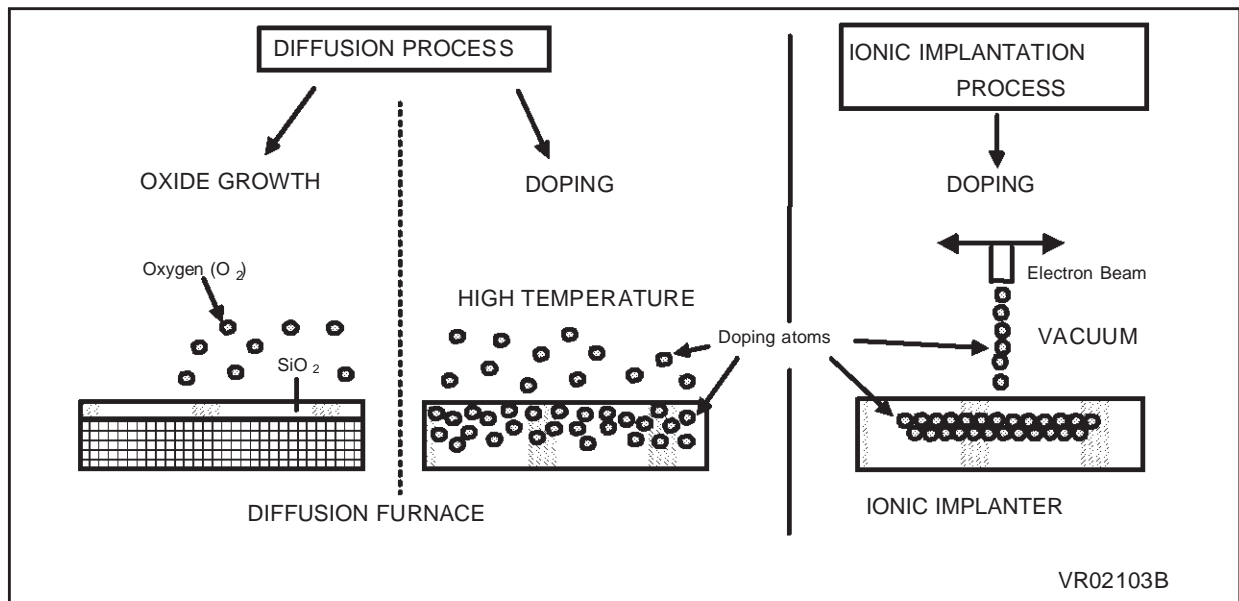
| | |
|--------------------|---|
| Passivation | Wafers are sealed with a passivation layer to prevent the device from contamination or moisture attack. This layer is usually made of silicon nitride or a silicon oxide composite. |
| Back-lap | It's the last step of wafer fabrication. Wafer thickness is reduced (for microcontroller chips, thickness is reduced from 650 to 380 microns), and sometimes a thin gold layer is deposited on the back of the wafer. |

Initially, the silicon chip forms part of a very thin (usually **650 microns**), round silicon slice: the raw wafer. Wafer diameters are typically **125, 150 or 200 mm** (5, 6 or 8 inches). However raw pure silicon has a main electrical property: it is an **isolating** material. So some of the features of silicon have to be altered, by means of well controlled processes. This is obtained by "doping" the silicon.

Dopants (or doping atoms) are purposely inserted in the silicon lattice, hence changing the features of the material in predefined areas: they are divided into "N" and "P" categories representing the **negative** and **positive** carriers they hold. Many different dopants are used to achieve these desired features: **Phosphorous, Arsenic** (N type) and **Boron** (P type) are the most frequently used ones. Semiconductors manufacturers purchase wafers predoped with N or P impurities to an impurity level of 1 ppm (one doping atom per ten million atoms of silicon).

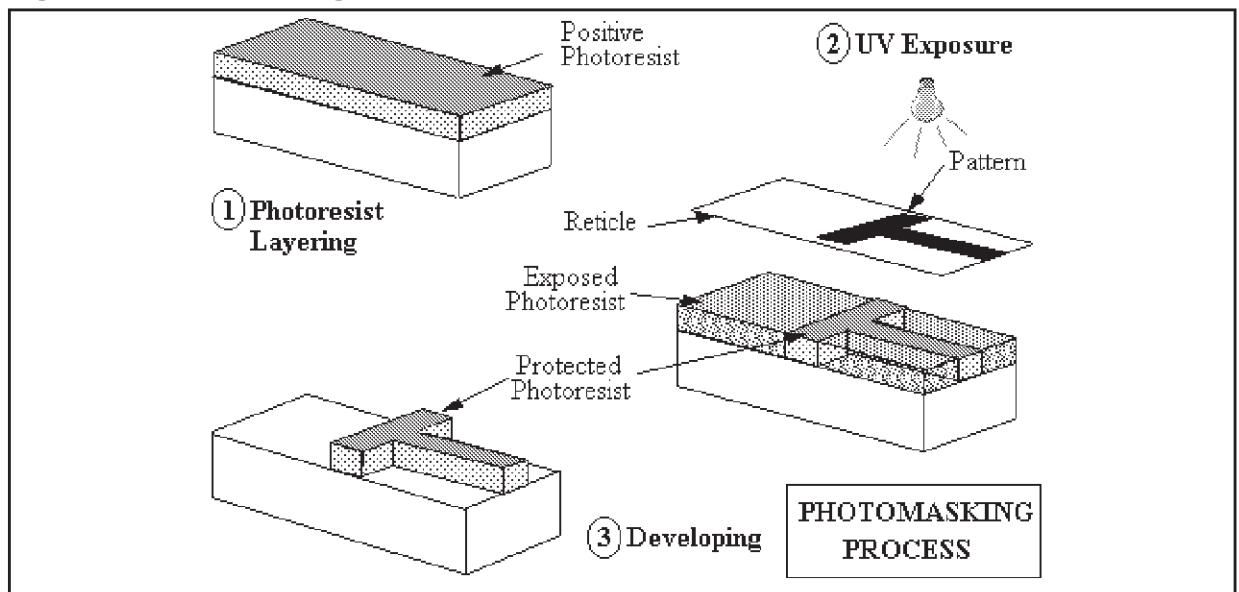
There are two ways to **dope** the silicon. The first one is to insert the wafer into a furnace. Doping gases are then introduced which impregnate the silicon surface. This is one part of the manufacturing process called **diffusion** (the other part being the oxide growth). The second way to dope the silicon is called **ionic implantation**. In this case, doping atoms are introduced inside the silicon using an electron beam. Unlike diffusion, ionic implantation allows to put atoms at a given depth inside the silicon and basically allows a better control of all the main parameters during the process. Ionic implantation process is simpler than diffusion process but more costly (ionic implanters are very expensive machines).

Figure 2. Diffusion and Ionic Implantation Processes



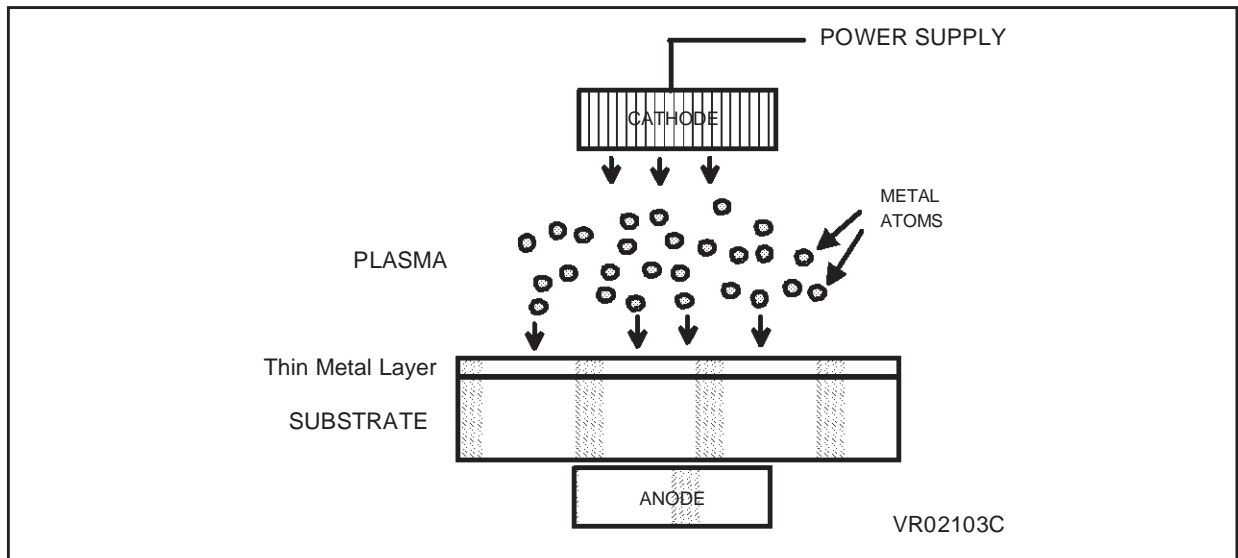
Photomasking (or masking) is an operation that is repeated many times during the process. This operation is described on the above graph. This step is called photomasking because the wafer is “masked” in some areas (using a specific pattern), in the same way one “masks out” or protects the windscreens of a car before painting the body. But even if the process is somewhat similar to the painting of a car body, in the case of a silicon chip the dimensions are measured in **tenth of microns**. The photoresist will replicate this pattern on the wafer. The exposed part of the photoresist is then rinsed off with a solvent (usually hydrofluoric or phosphoric acid).

Figure 3. Photomasking Process



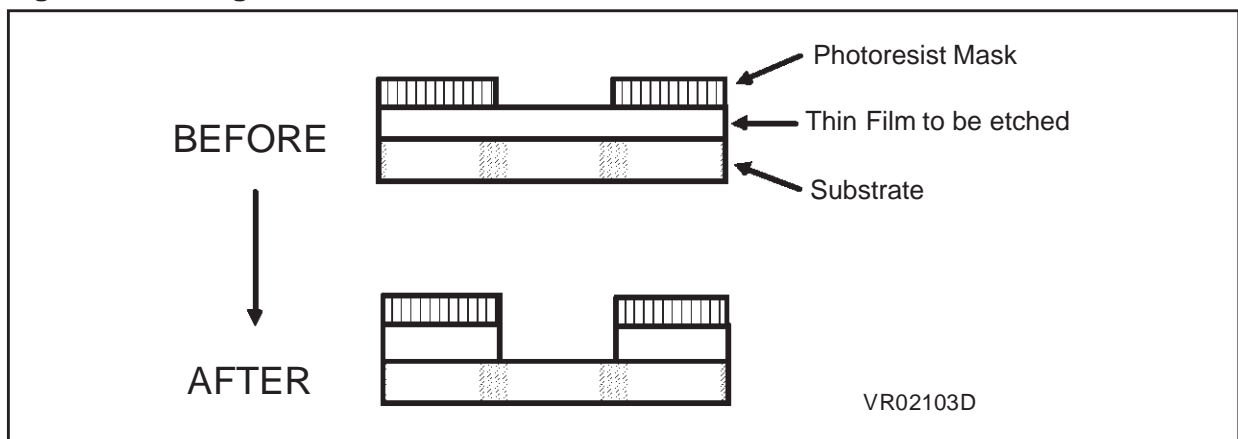
Metal deposition is used to put down a metal layer on the wafer surface. There are two ways to do that. The process shown on the graph below is called **sputtering**. It consists first in creating a plasma with argon ions. These ions bump into the target surface (composed of a metal, usually aluminium) and rip metal atoms from the target. Then, atoms are projected in all the directions and most of them condense on the substrate surface.

Figure 4. Metal Deposition Process



Etching process is used to etch into a specific layer the circuit pattern that has been defined during the photomasking process. Etching process usually occurs after deposition of the layer that has to be etched. For instance, the poly gates of a transistor are obtained by etching the poly layer. A second example are the aluminium connections obtained after etching of the aluminium layer.

Figure 5. Etching Process



Photomasking, ionic implantation, diffusion, metal deposition, and etching processes are repeated many times, using different materials and dopants at different temperatures in order to achieve all the operations needed to produce the requested characteristics of the silicon chip. The resolution limit (minimal line size inside the circuit) of current technology is **0.35 microns**. Achieving such results requires very sophisticated processes as well as superior quality levels.

Backlap is the final step of wafer fabrication. The wafer thickness is reduced from 650 microns to a minimum of 180 microns (for smartcard products).

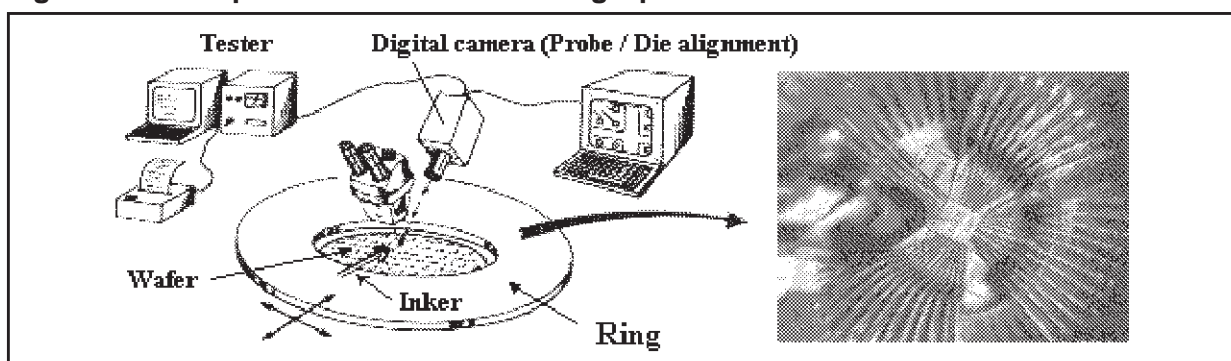
Wafer fabrication takes place in an extremely clean environment, where air cleanliness is **one million times better** than the air we normally breathe in a city, or some orders of magnitude better than the air in a heart transplant operating theatre. Photomasking, for example, takes place in rooms where there's maximum one particle whose diameter is superior to **0.5 micron** (and doesn't exceed 1 micron) inside **one cubic foot of air**.

All these processes are part of the **manufacturing phase** of the chip itself. Silicon chips are grouped on a silicon wafer (in the same way postage stamps are printed on a single sheet of paper) before being separated from each other at the beginning of the assembly phase.

Wafer Probing. This step takes place between wafer fabrication and assembly. It verifies the functionality of the device performing thousands of electrical tests, by means of special micro-probes (see graph on next page). Wafer probing is composed of two different tests:

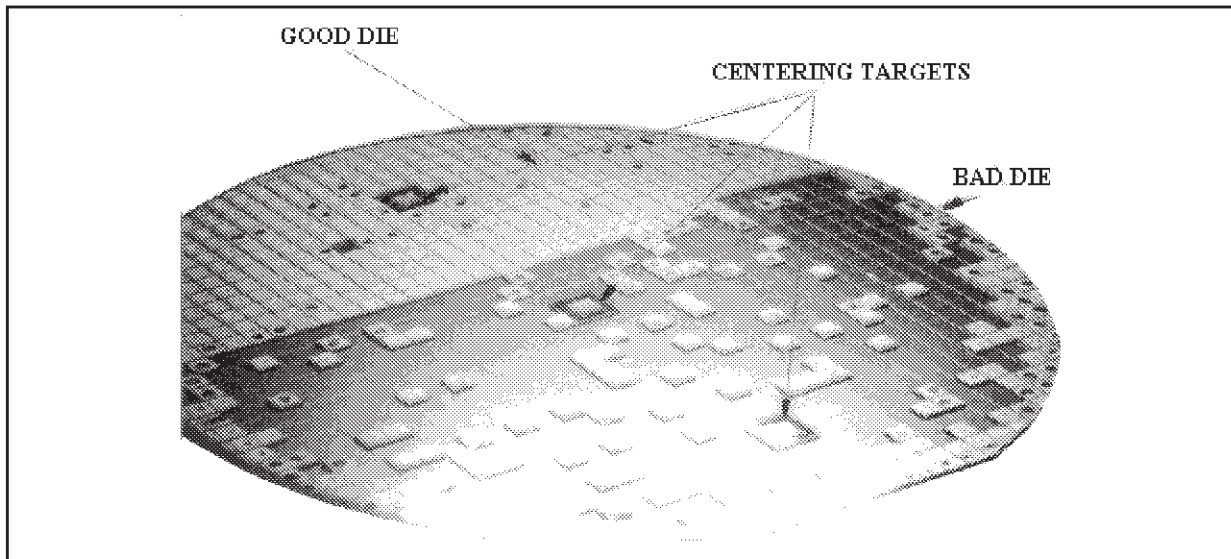
- 1. Process parametric test:** this test is performed on some test samples and checks the wafer fabrication process itself.
- 2. Full wafer probing test:** this test verifies the functionality of the finished product and is performed on all the dies.

Figure 6. Description of the Wafer Probing Operation



The bad die are automatically marked with a **black dot** so they can be separated from the good die after the wafer is cut. A record of what went wrong with the non-working die is closely examined by failure analysis engineers to determine where the problem occurred so that it may be corrected. The percentage of good die on an individual wafer is called its **yield**.

1.2 ASSEMBLY (BACK-END)

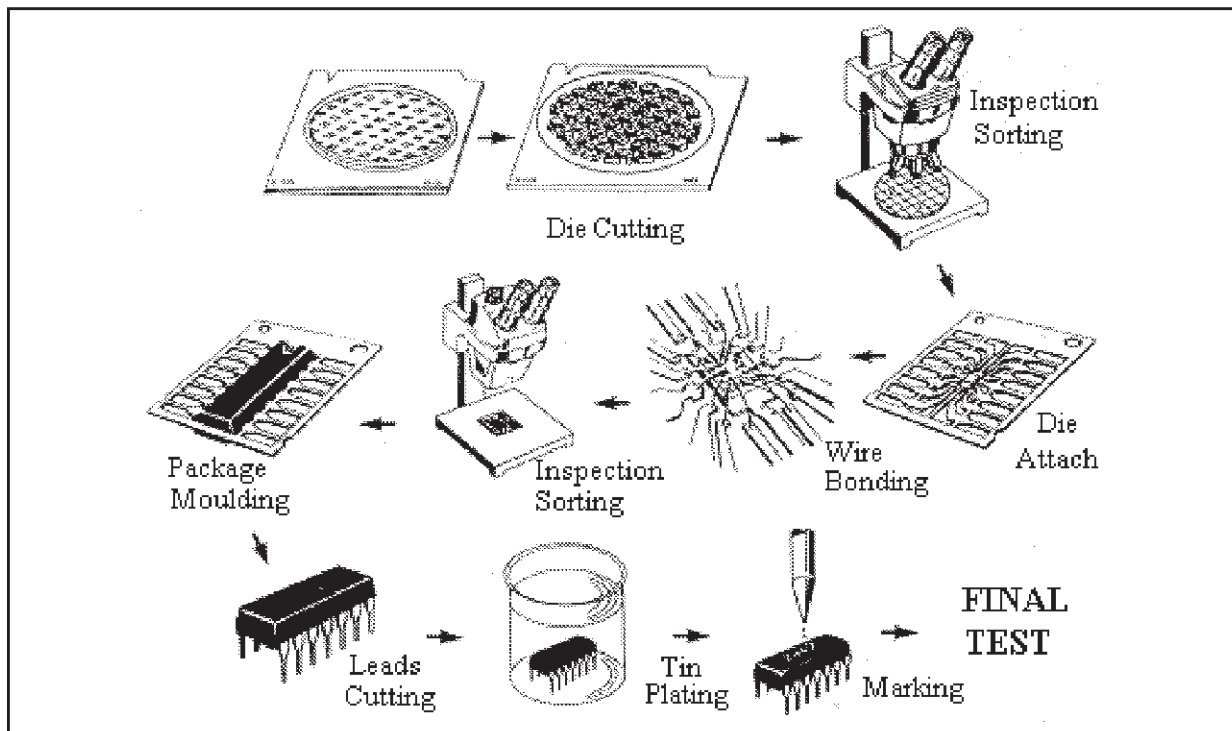


The first step of assembly is to separate the silicon chips: this step is called die cutting.

Then, the die are placed on a lead frame: the “leads” are the chip legs (which will be soldered or placed in a socket on a printed circuit board). On a surface smaller than a baby’s fingernail we now have thousands (or millions) of electronic components, all of them interconnected and capable of implementing a subset of a **complex electronic function**. At this stage the device is completely functional, but it would be impossible to use it without some sort of supporting system. Any scratch would alter its behaviour (or impact its reliability), any shock would cause failure.

Therefore, the die must be put into a ceramic or plastic package to be protected from the external world. A number of operations have to be made to realize this: they are described on the following graph.

Figure 7. Description of The Assembly Process



Wires thinner than a human hair (for microcontrollers the typical value is **33 microns**) are required to connect chips to the external world and enable electronic signals to be fed through the chip. The process of connecting these thin wires from the chip's bond pads to the package lead is called **wire bonding** (see also graph on next page for more details).

Figure 8. Wire Bonding

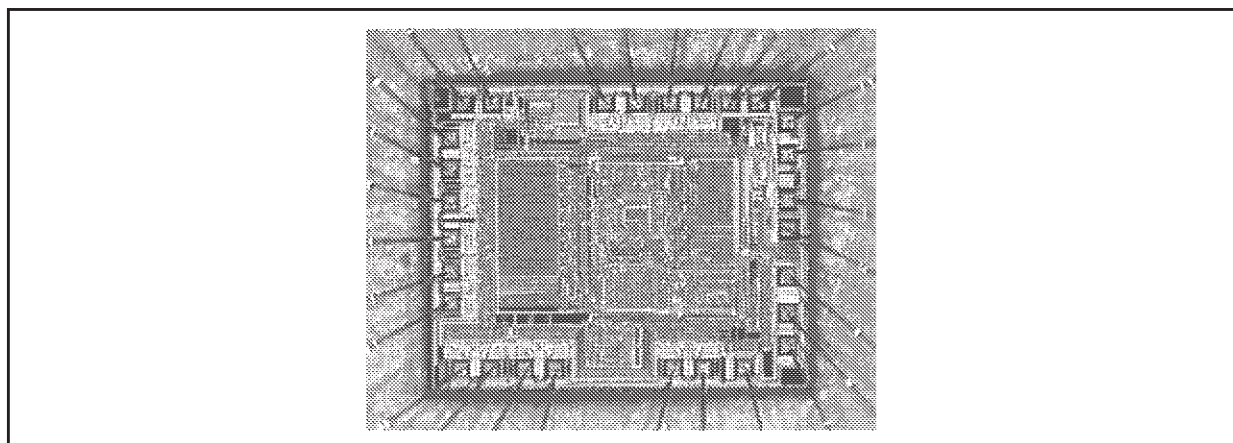
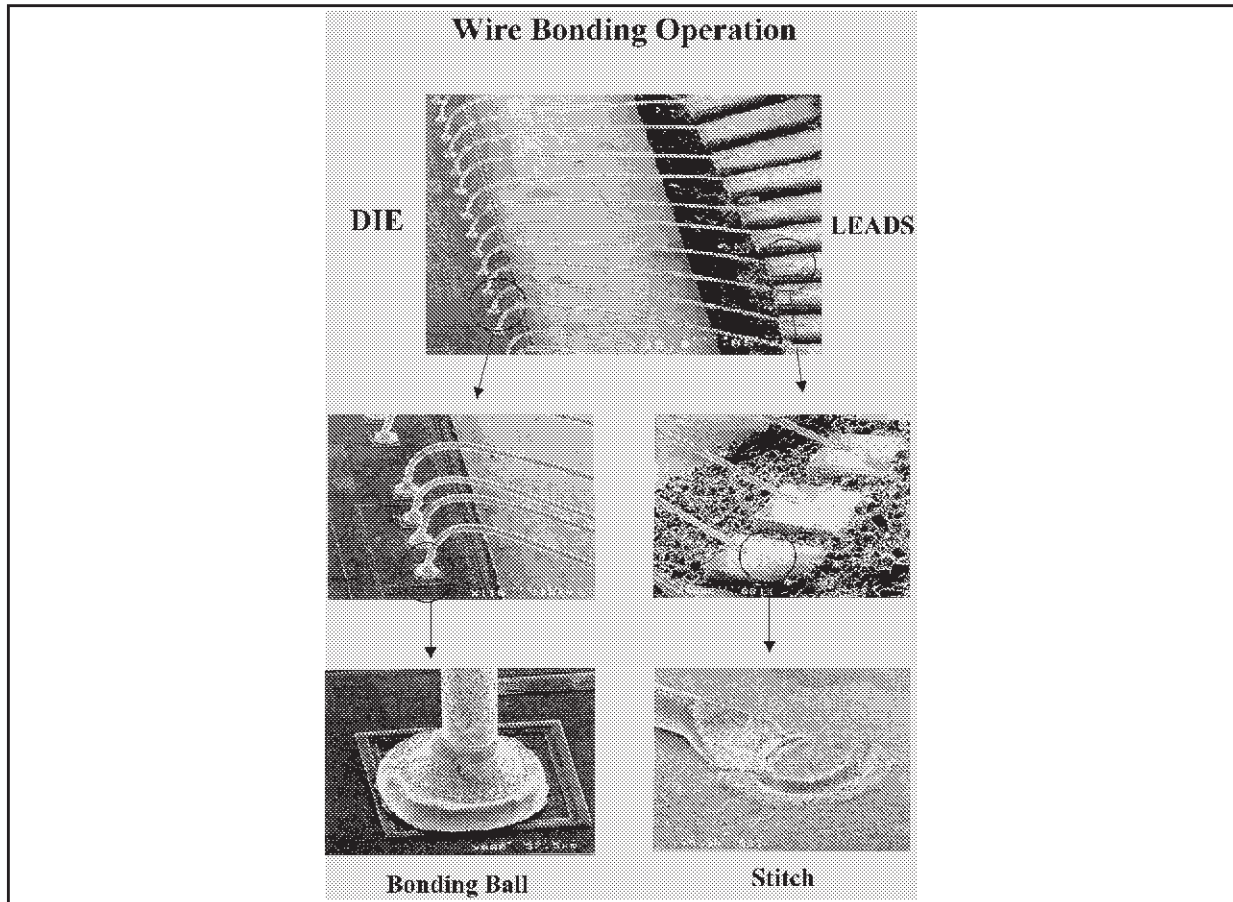
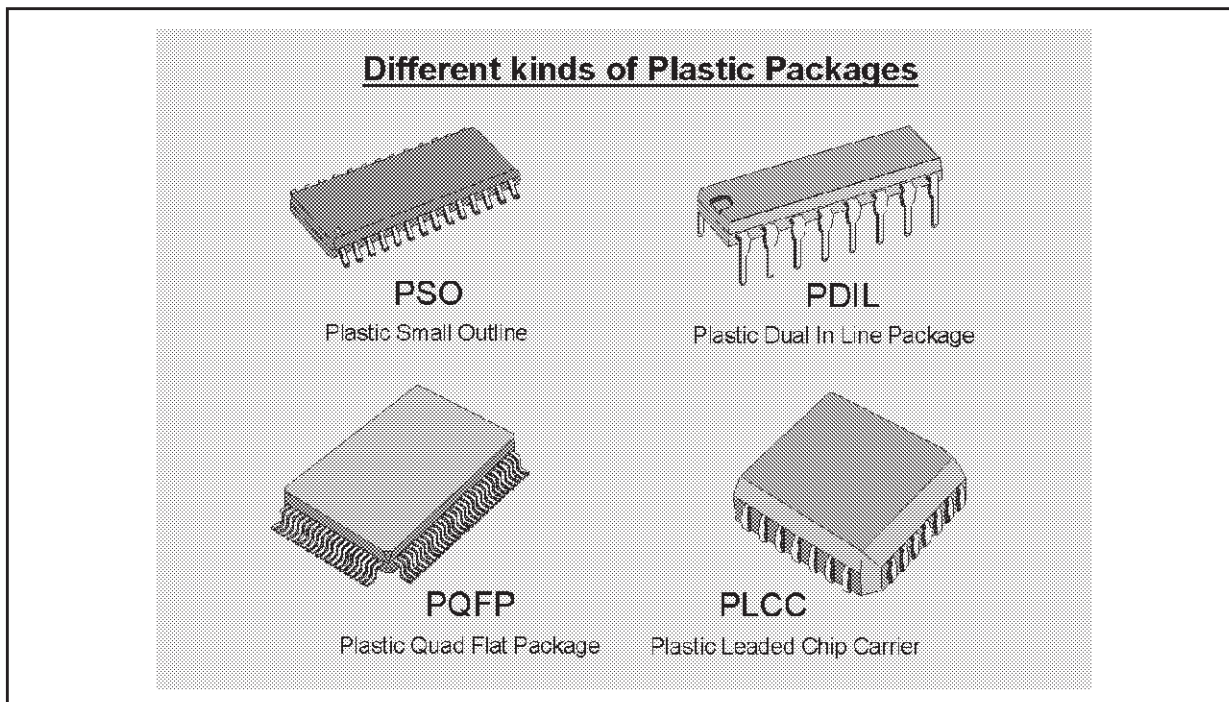


Figure 9. Wire Bonding Operation



The chip is then mounted in a **ceramic** or **plastic** package. The package not only protects the chip from external shocks, but also makes the whole device easier to handle. These packages come in a variety of shapes and sizes depending on the die itself and the application in which it will be used.

Figure 10. Different Kinds of Plastic Packages



Products are then marked with a **“traceability code”** which is used by the manufacturer and the user to identify the function of the device (and its date of fabrication). At the end of the assembly process, the integrated circuit is tested by automated test equipment. Only the integrated circuits that passed the tests will be packed and shipped to their final destination.

2 BASIC IC ELEMENT: THE TRANSISTOR

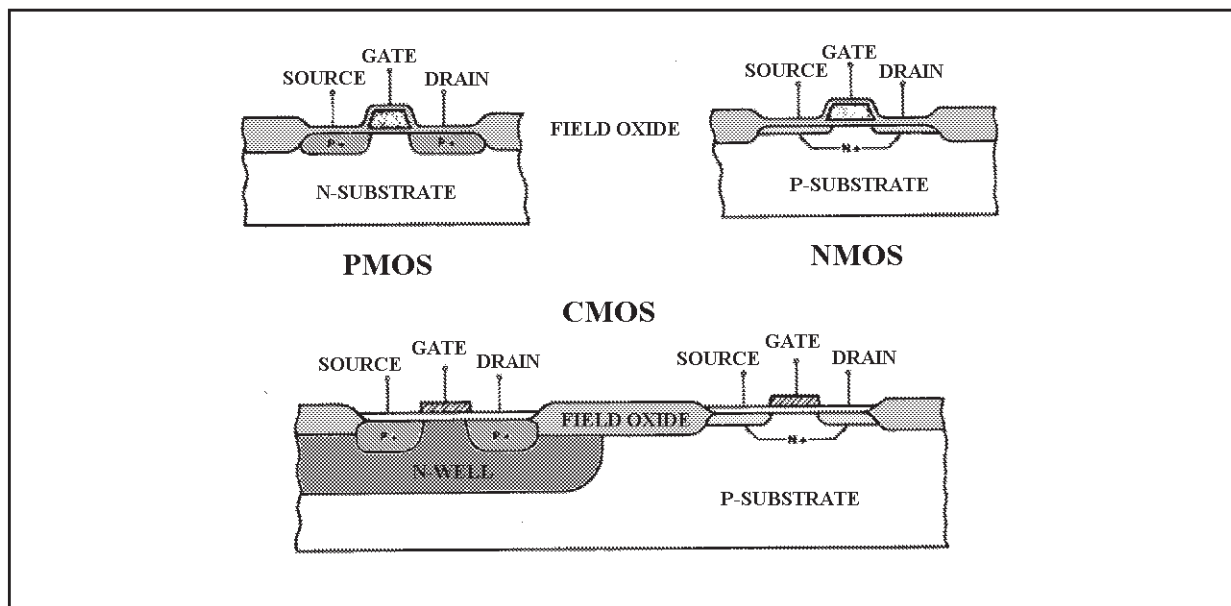
2.1 MOS TECHNOLOGY

We will examine first the basics of **MOS** (Metal Oxide Semiconductor) technologies as they are used for the majority of the integrated circuits manufactured at STMicroelectronics.

. There are three major MOS technology families: **PMOS**, **NMOS** and **CMOS**. They refer to the channel type of the MOS transistors made with the technology.

- **PMOS technologies** implement P-channel transistors by diffusing P-type dopants (usually Boron) into an N-type silicon substrate to form the source and the drain. P-channel is so named because the channel is composed of positively charged carriers.
- **NMOS technologies** are similar, but use N-type dopants (usually Phosphorus or Arsenic) to make N-channels transistors in P-type silicon substrate. N-channel is so named because the channel is composed of negatively charged carriers.
- **CMOS** (Complementary MOS) **technologies** combine both P-channel and N-channel devices on the same silicon. Either P or N-type silicon substrates can be used. However, deep areas of the opposite doping type (called wells) must be defined to allow fabrication of the complementary transistor type.

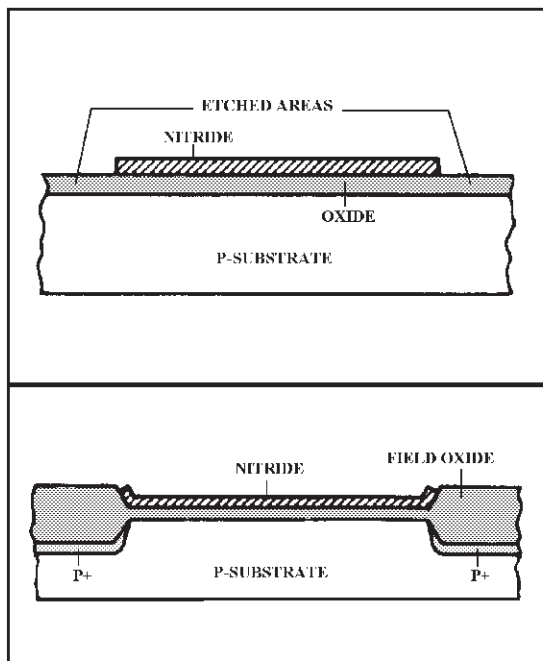
Figure 11. MOS Technologies



Most of the early semiconductor devices were made with PMOS technologies because it was easier to obtain stable manufacturing process with this technology. As higher speeds and greater densities were needed, new devices were implemented with NMOS. This was due to the higher speed of N-channel charge carriers (electrons) in silicon and also to the progress in the control of silicon doping. But CMOS technology has begun to see widespread commercial use in memory devices: it allowed the use of very low power devices. At the beginning, CMOS were slower than NMOS devices. Today, CMOS technology has been improved to produce higher speed devices.

2.2 FABRICATION OF A TRANSISTOR

The fabrication begins with a slice of single crystal silicon, uniformly doped P-type.

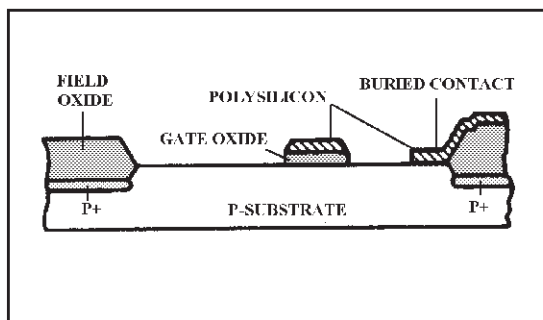


The wafer is oxidized in a furnace to grow a thin layer of **silicon dioxide** (SiO_2) on the surface. **Silicon nitride** is then deposited on the oxidized wafer in a gas phase chemical reactor. The wafer is now ready to receive the **first pattern** of what is to become a many layered complex circuit. The first pattern defines the **boundaries of the active regions** of the integrated circuit, where transistors, capacitors, diffused resistors and first level interconnects will be made.

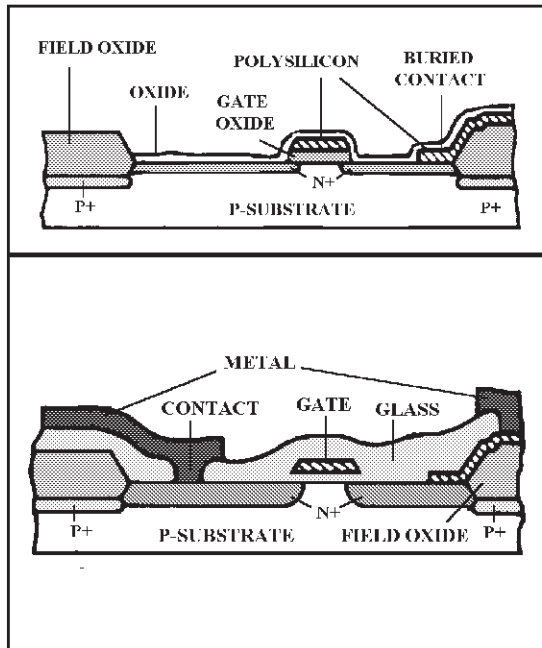
The patterned wafer is then implanted with boron atoms. **Boron** will only reach the etched zones of the silicon substrate, creating **P-type doped areas** that will electrically separate active areas. Wafer is oxidized again and the thick oxide only grows in the etched areas due to silicon nitride's properties as an oxidation barrier.

The remaining silicon nitride layer is removed. Now that the areas for active transistors have

been defined and isolated, the transistor types can be determined. The wafer is patterned and implanted with dopant atoms. The **energy** and **dose** at which the dopant atoms are implanted determines much of the **transistor's characteristics**.



The transistor types defined, the gate oxide of the active transistors are grown in a high temperature furnace. The gate oxide layer is then masked and holes are etched to provide direct access to buried contacts where needed. A **polycrystalline silicon layer** is deposited on the wafer. The gate layer is then patterned to define the actual transistor gates and interconnect paths.



Wafer is diffused with N-type dopants to form the **source** and **drain junction**. The transistor gate material acts as a barrier to the dopant providing an undiffused channel self-aligned to the two junctions. The wafer is then oxidized to **seal the junctions from contamination** with a layer of SiO_2 .

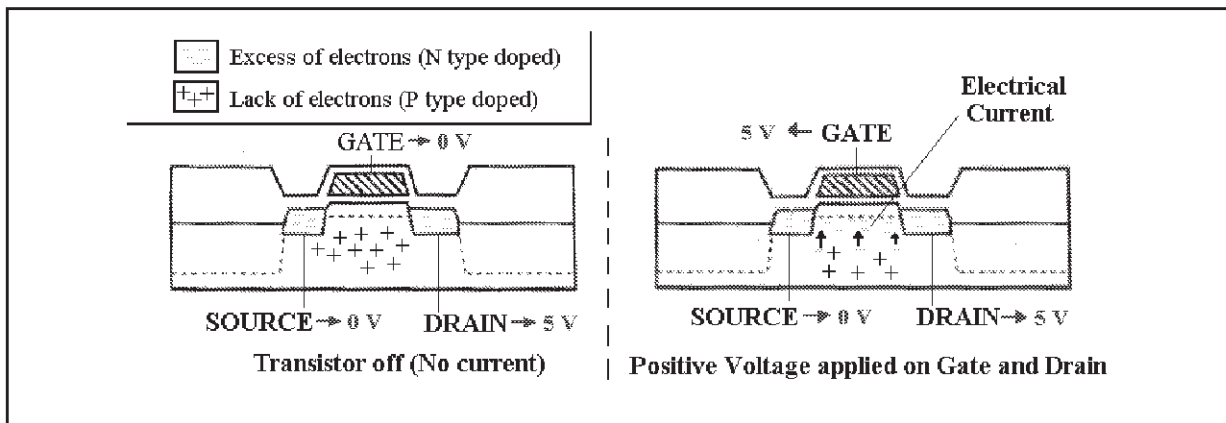
A thick glass layer is then deposited over the wafer (to provide better insulation), patterned with contact holes and placed in a high temperature furnace. Metal is deposited on the wafer and the interconnect patterns and external bonding pads are defined and etched. To prevent the device from contamination or moisture attack, wafers are sealed with a **passivation layer**. Patterning is done for the last time opening up windows only over the bond pads where external connections will be made.

This completes basic fabrication sequence for a **single poly and single metal layer** process.

2.3 HOW DOES A TRANSISTOR WORK?

Transistor is the basic element of an MCU device. There can be hundreds of thousands of them and the size of their gate can go down to 0.35 **microns**.

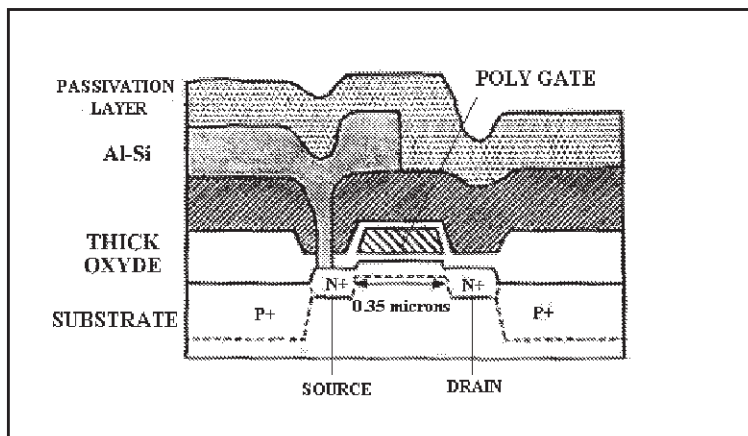
Let's explain the way a NMOS transistor operates. Basically, There's a lack of electrons between the Source (S) and the Drain (D) because this area has been implanted with a P-type dopant (Boron for instance). Therefore, when no voltage is applied, there's no current between the source and the drain (case of the **enhancement** transistor).



If we apply a positive voltage on the **gate** and the **drain**, then this will attract electrons in the channel existing between the source and the drain, therefore making it possible for an **electrical current** to flow between S and D.

There are two main types of transistor:

- **Enhancement Transistor:** channel is permanently **OFF**. It requires a positive applied gate voltage to turn on. Microcontrollers, for instance, mainly use this type of transistor.
- **Depletion Transistor:** channel is permanently **ON**. It requires a negative applied gate voltage to turn off.



This scheme is a cross section of a real transistor obtained after about **100 steps** of fabrication (see previous paragraph for the explanation of the different fabrication steps). The last layer is called a passivation layer and protects the transistor.

INTRODUCTION TO SEMICONDUCTOR TECHNOLOGY

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