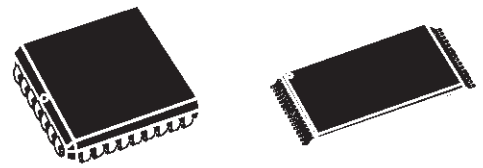
M29F040

4 Mbit (512Kb x8, Uniform Block) Single Supply Flash Memory

NOT FOR NEW DESIGN

- **M29F040 is replaced by the M29F040B**
- 5V ± 10% SUPPLY VOLTAGE for PROGRAM, ERASE and READ OPERATIONS
- FAST ACCESS TIME: 70ns
- BYTE PROGRAMMING TIME: 10µs typical
- ERASE TIME
  - Block: 1.0 sec typical
  - Chip: 2.5 sec typical
- PROGRAM/ERASE CONTROLLER (P/E.C.)
  - Program Byte-by-Byte
  - Data Polling and Toggle bits Protocol for P/E.C. Status
- MEMORY ERASE in BLOCKS
  - 8 Uniform Blocks of 64 KBytes each
  - Block Protection
  - Multiblock Erase
- ERASE SUSPEND and RESUME MODES
- LOW POWER CONSUMPTION
  - Read mode: 8mA typical (at 12MHz)
  - Stand-by mode: 25µA typical
  - Automatic Stand-by mode
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: E2h



PLCC32 (K)

TSOP32 (N)
8 x 20 mm

Figure 1. Logic Diagram

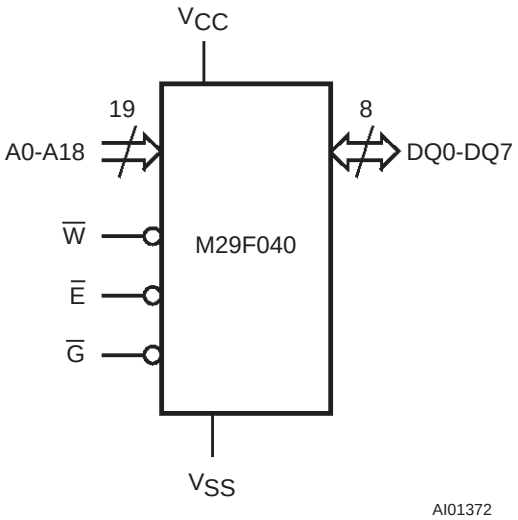


Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Input / Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Supply Voltage
V_{SS}	Ground

This is information on a product still in production but not recommended for new designs.

Figure 2A. LCC Pin Connections

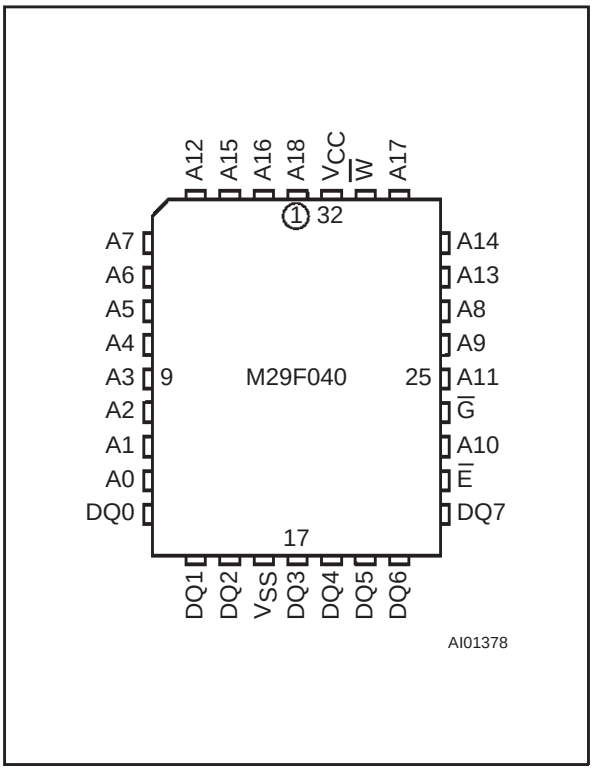


Figure 2B. TSOP Pin Connections

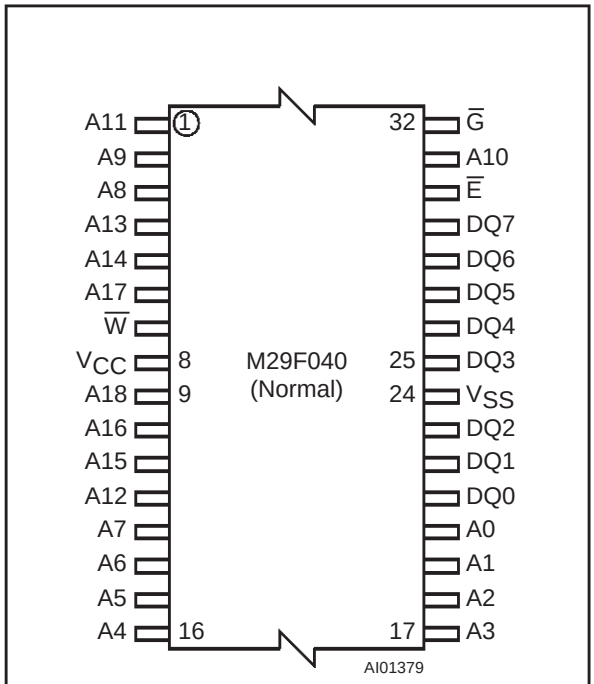
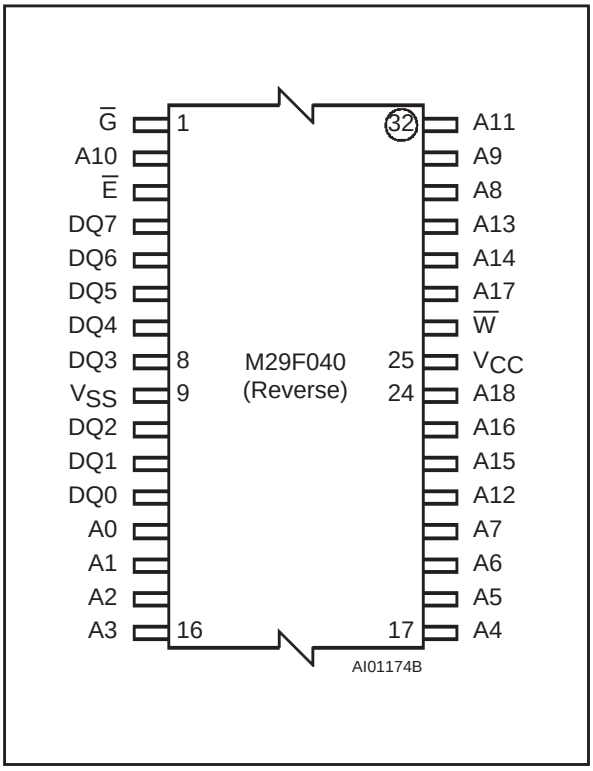


Figure 2C. TSOP Reverse Pin Connections



DESCRIPTION

The M29F040 is a non-volatile memory that may be erased electrically at the block level, and programmed Byte-by-Byte.

The interface is directly compatible with most microprocessors. PLCC32 and TSOP32 (8 x 20mm) packages are available. Both normal and reverse pin outs are available for the TSOP32 package.

Organisation

The Flash Memory organisation is 512K x8 bits with Address lines A0-A18 and Data Inputs/Outputs DQ0-DQ7. Memory control is provided by Chip Enable, Output Enable and Write Enable Inputs.

Erase and Program are performed through the internal Program/Erase Controller (P/E.C.).

Data Outputs bits DQ7 and DQ6 provide polling or toggle signals during Automatic Program or Erase to indicate the Ready/Busy state of the internal Program/Erase Controller.

Memory Blocks

Erasure of the memory is in blocks. There are 8 uniform blocks of 64 Kbytes each in the memory address space. Each block can be programmed and erased over 100,000 cycles. Each uniform block may separately be protected and unpro-

Table 2. Absolute Maximum Ratings (1)

Symbol	Parameter	Value	Unit
T_A	Ambient Operating Temperature (3)	–40 to 125	°C
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{IO} (2)	Input or Output Voltages	–0.6 to 7	V
V_{CC}	Supply Voltage	–0.6 to 7	V
V_{A9} (2)	A9 Voltage	–0.6 to 13.5	V

Notes: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.
2. Minimum Voltage may undershoot to –2V during transition and for less than 20ns.
3. Depends on range.

tected against program and erase. Block erasure may be suspended, while data is read from other blocks of the memory, and then resumed.

Bus Operations

Seven operations can be performed by the appropriate bus cycles, Read Array, Read Electronic Signature, Output Disable, Standby, Protect Block, Unprotect Block, and Write the Command of an Instruction.

Command Interface

Command Bytes can be written to a Command Interface (C.I.) latch to perform Reading (from the Array or Electronic Signature), Erasure or Programming. For added data protection, command execution starts after 4 or 6 command cycles. The first, second, fourth and fifth cycles are used to input a code sequence to the Command Interface (C.I.). This sequence is equal for all P/E.C. instructions. Command itself and its confirmation - if it applies - are given on the third and fourth or sixth cycles.

Instructions

Seven instructions are defined to perform Reset, Read Electronic Signature, Auto Program, Block Auto Erase, Chip Auto Erase, Block Erase Suspend and Block Erase Resume. The internal Program/Erase Controller (P/E.C.) handles all timing and verification of the Program and Erase instructions and provides Data Polling, Toggle, and Status data to indicate completion of Program and Erase Operations.

Instructions are composed of up to six cycles. The first two cycles input a code sequence to the Command Interface which is common to all P/E.C. instructions (see Table 7 for Command Descriptions). The third cycle inputs the instruction set up command instruction to the Command Interface. Subsequent cycles output Signature, Block Protection or the addressed data for Read operations. For added data protection, the instructions for program, and block or chip erase require further command inputs. For a Program instruction, the fourth command cycle inputs the address and data to be programmed. For an Erase instruction (block or chip), the fourth and fifth cycles input a further code sequence before the Erase confirm command on the sixth cycle. Byte programming takes typically 10µs while erase is performed in typically 1.0 second.

Erasure of a memory block may be suspended, in order to read data from another block, and then resumed. Data Polling, Toggle and Error data may be read at any time, including during the programming or erase cycles, to monitor the progress of the operation. When power is first applied or if V_{CC} falls below V_{LKO}, the command interface is reset to Read Array.

Table 3. Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0 - DQ7
Read	V_{IL}	V_{IL}	V_{IH}	Data Output
Write	V_{IL}	V_{IH}	V_{IL}	Data Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	Hi-Z
Standby	V_{IH}	X	X	Hi-Z

Note: X = V_{IL} or V_{IH}

Table 4. Electronic Signature

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A9	Other Addresses	DQ0 - DQ7
Manufact. Code	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	V_{ID}	Don't Care	20h
Device Code	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{ID}	Don't Care	E2h

Table 5. Block Protection Status

Code	$\overline{E}$	$\overline{G}$	$\overline{W}$	A0	A1	A6	A16	A17	A18	Other Addresses	DQ0 - DQ7
Protected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	01h
Unprotected Block	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	SA	SA	SA	Don't Care	00h

Note: SA = Address of block being checked

DEVICE OPERATION

Signal Descriptions

Address Inputs (A0-A18). The address inputs for the memory array are latched during a write operation. The A9 address input is used also for the Electronic Signature read and Block Protect verification. When A9 is raised to V_{ID}, either a Read Manufacturer Code, Read Device Code or Verify Block Protection is enabled depending on the combination of levels on A0, A1 and A6. When A0, A1 and A6 are Low, the Electronic Signature Manufacturer code is read, when A0 is High and A1 and A6 are Low, the Device code is read, and when A1 is High and A0 and A6 are low, the Block Protection Status is read for the block addressed by A16, A17, A18.

Data Input/Outputs (DQ0-DQ7). The data input is a byte to be programmed or a command written to the C.I. Both are latched when Chip Enable $\overline{E}$ and Write Enable $\overline{W}$ are active. The data output is from the memory Array, the Electronic Signature, the Data Polling bit (DQ7), the Toggle Bit (DQ6), the Error bit (DQ5) or the Erase Timer bit (DQ3). Ouputs are valid when Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled.

Chip Enable ($\overline{E}$). The Chip Enable activates the memory control logic, input buffers, decoders and sense amplifiers. $\overline{E}$ High deselects the memory and reduces the power consumption to the standby level. $\overline{E}$ can also be used to control writing to the command register and to the memory array, while $\overline{W}$ remains at a low level. Addresses are then latched on the falling edge of $\overline{E}$ while data is latched on the rising edge of $\overline{E}$. The Chip Enable must be forced to V_{ID} during Block Unprotect operations.

Output Enable ($\overline{G}$). The Output Enable gates the outputs through the data buffers during a read operation. $\overline{G}$ must be forced to V_{ID} level during Block Protect and Block Unprotect operations.

Write Enable ($\overline{W}$). This input controls writing to the Command Register and Address and Data latches. Addresses are latched on the falling edge of $\overline{W}$, and Data Inputs are latched on the rising edge of $\overline{W}$.

V_{CC} Supply Voltage. The power supply for all operations (Read, Program and Erase).

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

Table 6. Instructions (1,2)

Mne.	Instr.	Cyc.		1st Cyc.	2nd Cyc.	3rd Cyc.	4th Cyc.	5th Cyc.	6th Cyc.	7th Cyc.
RST (4,10)	Read Array/ Reset	1+	**Addr.** (3,7)	X	Read Memory Array until a new write cycle is initiated.					
			Data	F0h						
		3+	**Addr.** (3,7)	5555h	2AAAh	5555h	Read Memory Array until a new write cycle is initiated.			
			Data	AAh	55h	F0h				
RSIG (4)	Read Electronic Signature	3+	**Addr.** (3,7)	5555h	2AAAh	5555h	Read Electronic Signature until a new write cycle is initiated. See Note 5.			
			Data	AAh	55h	90h				
RBP (4)	Read Block Protection	3+	**Addr.** (3,7)	5555h	2AAAh	5555h	Read Block Protection until a new write cycle is initiated. See Note 6.			
			Data	AAh	55h	90h				
PG	Program	4	**Addr.** (3,7)	5555h	2AAAh	5555h	Program Address	Read Data Polling or Toggle Bit until Program completes.		
			Data	AAh	55h	A0h	Program Data			
BE	Block Erase	6	**Addr.** (3,7)	5555h	2AAAh	5555h	5555h	2AAAh	Block Address	Additional Block (8)
			Data	AAh	55h	80h	AAh	55h	30h	30h
CE	Chip Erase	6	**Addr.** (3,7)	5555h	2AAAh	5555h	5555h	2AAAh	5555h	Note 9
			Data	AAh	55h	80h	AAh	55h	10h	
ES	Erase Suspend	1	**Addr.** (3,7)	X	Read until Toggle stops, then read all the data needed from any uniform block(s) not being erased then Resume Erase.					
			Data	B0h						
ER	Erase Resume	1	**Addr.** (3,7)	X	Read Data Polling or Toggle Bit until Erase completes or Erase is suspended another time					
			Data	30h						

Notes: 1. Command not interpreted in this table will default to read array mode.
2. While writing any command or during RSG and RSP execution, the P/E.C. can be reset by writing the command 00h to the C.I.
3. X = Don't Care.
4. The first cycle of the RST, RBP or RSIG instruction is followed by read operations to read memory array, Status Register or Electronic Signature codes. Any number of read cycles can occur after one command cycle.
5. Signature Address bits A0, A1, A6 at V_{IL} will output Manufacturer code (20h). Address bits A0 at V_{IH} and A1, A6 at V_{IL} will output Device code.
6. Protection Address: A0, A6 at V_{IL}, A1 at V_{IH} and A16, A17, A18 within the uniform block to be checked, will output the Block Protection status.
7. Address bits A15-A18 are don't care for coded address inputs.
8. Optional, additional blocks addresses must be entered within a 80µs delay after last write entry, timeout status can be verified through DQ3 value. When full command is entered, read Data Polling or Toggle bit until Erase is completed or suspended.
9. Read Data Polling or Toggle bit until Erase completes.
10. A wait time of 5µs is necessary after a Reset command, if the memory is in a Block Erase status, before starting any operation.

Memory Blocks

The memory blocks of the M29F040 are shown in Figure 3. The memory array is divided in 8 uniform blocks of 64 Kbytes. Each block can be erased separately or any combination of blocks can be erased simultaneously. The Block Erase operation is managed automatically by the P/E.C. The operation can be suspended in order to read from any other block, and then resumed.

Block Protection provides additional data security. Each uniform block can be separately protected or unprotected against Program or Erase. Bringing A9 and $\overline{G}$ to V_{ID} initiates protection, while bringing A9, $\overline{G}$ and $\overline{E}$ to V_{ID} cancels the protection. The block affected during protection is addressed by the inputs on A16, A17, and A18. Unprotect operation affects all blocks.

Operations

Operations are defined as specific bus cycles and signals which allow Memory Read, Command Write, Output Disable, Standby, Read Status Bits, Block Protect/Unprotect, Block Protection Check and Electronic Signature Read. They are shown in Tables 3, 4, 5.

Read. Read operations are used to output the contents of the Memory Array, the Status Register or the Electronic Signature. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be low in order to read the output of the memory. The Chip Enable input also provides power control and should be used for device selection. Output Enable should be used to gate data onto the output independent of the device selection. The data read depends on the previous command written to the memory (see instructions RST and RSIG, and Status Bits).

Write. Write operations are used to give Instruction Commands to the memory or to latch input data to be programmed. A write operation is initiated when Chip Enable $\overline{E}$ is Low and Write Enable $\overline{W}$ is Low with Output Enable $\overline{G}$ High. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ whichever occurs last. Commands and Input Data are latched on the rising edge of $\overline{W}$ or $\overline{E}$ whichever occurs first.

Output Disable. The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

Standby. The memory is in standby when Chip Enable $\overline{E}$ is High and Program/Erase Controller P/E.C. is Idle. The power consumption is reduced to the standby level and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

Automatic Standby. After 150ns of inactivity and when CMOS levels are driving the addresses, the chip automatically enters a pseudo standby mode where consumption is reduced to the CMOS standby value, while outputs are still driving the bus.

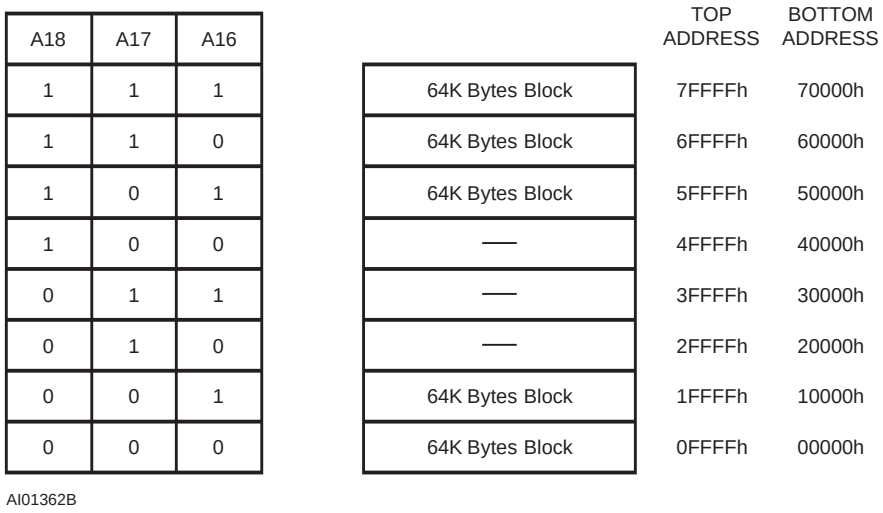
Electronic Signature. Two codes identifying the manufacturer and the device can be read from the memory, the manufacturer'scode for STMicroelectronics is 20h, and the device code is E2h for the M29F040. These codes allow programming equipment or applications to automatically match their interface to the characteristics of the particular manufacturer's product. The Electronic Signature is output by a Read operation when the voltage applied to A9 is at V_{ID} and address inputs A1 and A6 are at Low. The manufacturer code is output when the Address input A0 is Low and the device code when this input is High. Other Address inputs are ignored. The codes are output on DQ0-DQ7. This is shown in Table 4.

The Electronic Signature can also be read, without raising A9 to V_{ID} by giving the memory the instruction RSIG (see below).

Block Protection. Each uniform block can be separately protected against Program or Erase. Block Protection provides additional data security, as it disables all program or erase operations. This mode is activated when both A9 and $\overline{G}$ are set to V_{ID} and the block address is applied on A16-A18. Block Protection is programmed using a Presto F program like algorithm. Protection is initiated on the edge of $\overline{W}$ falling to V_{IL}. Then after a delay of 100µs, the edge of $\overline{W}$ rising to V_{IH} ends the protection operation. Protection verify is achieved by bringing $\overline{G}$, $\overline{E}$ and A6 to V_{IL} while $\overline{W}$ is at V_{IH} and A9 at V_{ID}. Under these conditions, reading the data output will yield 01h if the block defined by the inputs on A16-A18 is protected. Any attempt to program or erase a protected block will be ignored by the device.

Any protected block can be unprotected to allow updating of bit contents. All blocks must be protected before an unprotect operation. Block Unprotect is activated when A9, $\overline{G}$ and $\overline{E}$ are at V_{ID}. The addresses inputs A6, A12, A16 must be maintained at V_{IH}. Block Unprotect is performed through a Presto F Erase like algorithm. Unprotect is initiated by the edge of $\overline{W}$ falling to V_{IL}. After a delay of 10ms, the edge of $\overline{W}$ rising to V_{IH} will end the unprotection operation. Unprotect verify is achieved by bringing $\overline{G}$ and $\overline{E}$ to V_{IL} while A6 and $\overline{W}$ are at V_{IH} and A9 at V_{ID}. In these conditions, reading the output data will yield 00h if the block defined by the inputs on A16-A18 has been successfully unprotected. All combinations of A16-A18 must be addressed in order to ensure that all of the 8 uniform blocks have been unprotected. Block Protection Status is shown in Table 5.

Figure 3. Memory Map and Block Address Table



Instructions and Commands

The Command Interface (C.I.) latches commands written to the memory. Instructions are made up from one or more commands to perform Read Array/Reset, Read Electronic Signature, Block Erase, Chip Erase, Program, Block Erase Suspend and Erase Resume. Commands are made of address and data sequences. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ and data is latched on the rising of $\overline{W}$ or $\overline{E}$. The instructions require from 1 to 6 cycles, the first or first three of which are always write operations used to initiate the command. They are followed by either further write cycles to confirm the first command or execute the command immediately. Command sequencing must be followed exactly. Any invalid combination of commands will reset the device to Read Array. The increased number of cycles has been chosen to assure maximum data security. Commands are initialised by two preceding coded cycles which unlock the Command Interface. In addition, for Erase, command confirmation is again preceeded by the two coded cycles.

P/E.C. status is indicated during command execution by Data Polling on DQ7, detection of Toggle on DQ6, or Error on DQ5 and Erase Timer DQ3 bits. Any read attempt during Program or Erase command execution will automatically output those four bits. The P/E.C. automatically sets bits DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1, DQ2 and DQ4) are reserved for future use and should be masked.

Table 7. Commands

Hex Code	Command
00h	Read
10h	Chip Erase Confirm
30h	Block Erase Resume/Confirm
80h	Set-up Erase
90h	Read Electronic Signature/ Block Protection Status
A0h	Program
B0h	Erase Suspend
F0h	Read Array/Reset

Table 8. Status Register

DQ	Name	Logic Level	Definition	Note
7	Data Polling	'1'	Erase Complete	Indicates the P/E.C. status, check during Program or Erase, and on completion before checking bits DQ5 for Program or Erase Success.
		'0'	Erase on Going	
		DQ	Program Complete	
		$\overline{DQ}$	Program on Going	
6	Toggle Bit	'-1-0-1-0-1-0-1-'	Erase or Program on Going	Successive read output complementary data on DQ6 while Programming or Erase operations are going on. DQ6 remain at constant level when P/E.C. operations are completed or Erase Suspend is acknowledged.
		'-0-0-0-0-0-0-0-'	Program ('0' on DQ6) Complete	
		'-1-1-1-1-1-1-1-'	Erase or Program ('1' on DQ6) Complete	
5	Error Bit	'1'	Program or Erase Error	This bit is set to '1' if P/E.C. has exceded the specified time limits.
		'0'	Program or Erase on Going	
4		'1'		
		'0'		
3	Erase Time Bit	'1'	Erase Timeout Period Expired	P/E.C. Erase operation has started. Only possible command entry is Erase Suspend (ES). An additional block to be erased in parallel can be entered to the P/E.C.
		'0'	Erase Timeout Period on Going	
2	Reserved			
1	Reserved			
0	Reserved			

Note: Logic level '1' is High, '0' is Low. -0-1-0-0-0-1-1-1-0- represent bit value in successive Read operations.

Data Polling bit (DQ7). When Programming operations are in progress, this bit outputs the complement of the bit being programmed on DQ7. During Erase operation, it outputs a '0'. After completion of the operation, DQ7 will output the bit last programmed or a '1' after erasing. Data Polling is valid only effective during P/E.C. operation, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. It must be performed at the address being programmed or at an address within the block being erased. If the byte to be programmed belongs to a protected block the command is ignored. If all the blocks selected for erasure are protected, DQ7 will set to '0' for about 100µs, and then return to previous addressed memory data. See Figure 9 for the Data Polling flowchart and Figure 10 for the Data Polling waveforms.

Toggle bit (DQ6). When Programming operations are in progress, successive attempts to read DQ6 will output complementary data. DQ6 will toggle following toggling of either $\overline{G}$ or $\overline{E}$ when $\overline{G}$ is low. The operation is completed when two successive reads yield the same output data. The next read will output the bit last programmed or a '1' after erasing. The toggle bit is valid only effective during P/E.C. operations, that is after the fourth $\overline{W}$ pulse for programming or after the sixth $\overline{W}$ pulse for Erase. If the byte to be programmed belongs to a protected block the command will be ignored. If the blocks selected for erasure are protected, DQ6 will toggle for about 100µs and then return back to Read. See Figure 11 for Toggle Bit flowchart and Figure 12 for Toggle Bit waveforms.

Error bit (DQ5). This bit is set to '1' by the P/E.C when there is a failure of byte programming, block erase, or chip erase that results in invalid data being programmed in the memory block. In case of error in block erase or byte program, the block in which the error occured or to which the programmed byte belongs, must be discarded. Other blocks may still be used. Error bit resets after Reset (RST) instruction. In case of success, the error bit will set to '0' during Program or Erase and to valid data after write operation is completed.

Table 9. AC Measurement Conditions

	High Speed	Standard
Input Rise and Fall Times	≤ 10ns	≤ 10ns
Input Pulse Voltages	0 to 3V	0.45V to 2.4V
Input and Output Timing Ref. Voltages	1.5V	0.8V and 2V

Figure 4. AC Testing Input Output Waveform

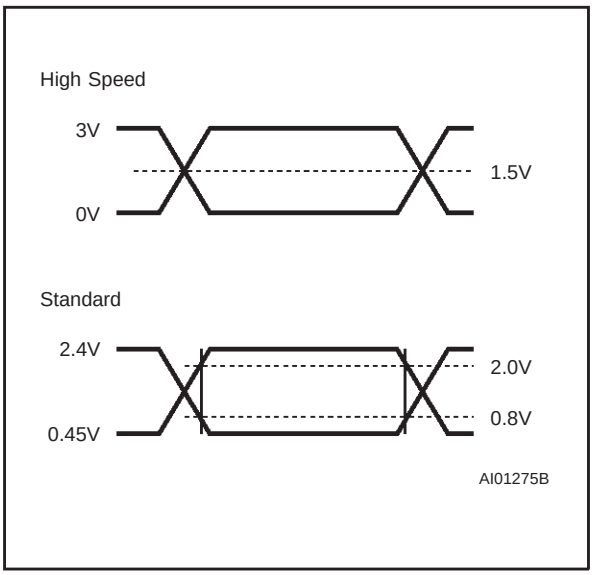


Figure 5. AC Testing Load Circuit

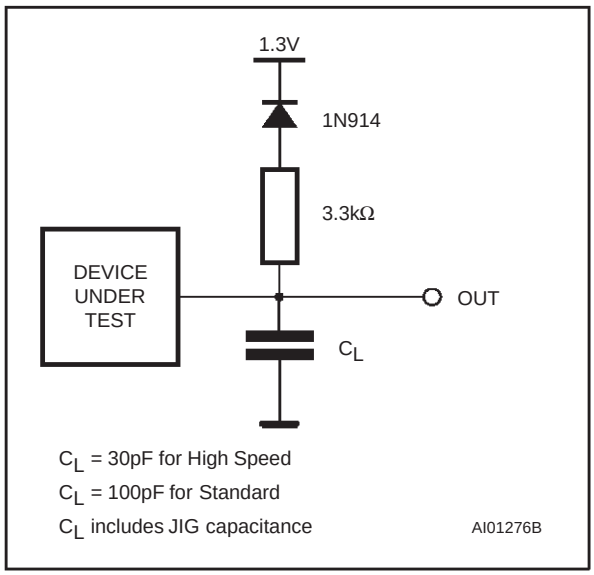


Table 10. Capacitance (1) (T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: 1. Sampled only, not 100% tested.

Erase Timer bit (DQ3). This bit is set to '0' by the P/E.C. when the last Block Erase command has been entered to the Command Interface and it is awaiting the Erase start. When the wait period is finished, after 80 to 120µs, DQ3 returns back to '1'.

Coded Cycles. The two coded cycles unlock the Command Interface. They are followed by a command input or a comand confirmation. The coded cycles consist of writing the data AAh at address 5555h during the first cycle and data 55h at address 2AAAh during the second cycle. Addresses are latched on the falling edge of $\overline{W}$ or $\overline{E}$ while data is latched on the rising edge of $\overline{W}$ or $\overline{E}$. The coded cycles happen on first and second cycles of the command write or on the fourth and fifth cycles.

Read Array/Reset (RST) instruction. The Reset instruction consists of one write operation giving the command F0h. It can be optionally preceded by the two coded cycles. A wait state of 5µs before read operations is necessary if the Reset command is applied during an Erase operation.

Read Electronic Signature (RSIG) instruction. This instruction uses the two coded cycles followed by one write cycle giving the command 90h to address 5555h for command setup. A subsequent read will output the manufacturer code, the device code or the Block Protection status depending on the levels of A0, A1, A6, A16, A17 and A18. The manufacturer code, 20h, is output when the addresses lines A0, A1 and A6 are Low, the device code, E2h is output when A0 is High with A1 and A6 Low.

Table 11. DC Characteristics
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C; V_{CC} = 5V ± 10%)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		15	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		1	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$		50	µA
I_{CC4}	Supply Current (Program or Erase)	Byte Program, Block Erase		20	mA
I_{CC5}	Supply Current	Chip Erase in progress		40	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 10mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4		V
		I_{OH} = –2.5mA	0.85 V_{CC}		V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	12.5	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		50	µA
V_{LKO}	Supply Voltage (Erase and Program lock-out)		3.2	4.2	V

Read Block Protection (RBP) instruction. The use of Read Electronic Signature (RSIG) command also allows access to the Block Protection status verify. After giving the RSIG command, A0 and A6 are set to V_{IL} with A1 at V_{IH}, while A16, A17 and A18 define the block of the block to be verified. A read in these conditions will output a 01h if block is protected and a 00h if block is not protected.

This Read Block Protection is the only valid way to check the protection status of a block. Nevertheless, it must not be used during the Block Protection phase as a method to verify the block protection. Please refer to Block Protection paragraph.

Chip Erase (CE) instruction. This instruction uses six write cycles. The Erase Set-up command 80h is written to address 5555h on third cycle after the two coded cycles. The Chip Erase Confirm command 10h is written at address 5555h on sixth cycle after another two coded cycles. If the second command given is not an erase confirm or if the coded cycles are wrong, the instruction aborts and the device is reset to Read Array. It is not necessary to program the array with 00h first as the P/E.C. will automatically do this before erasing to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register bits. During the execution of the erase by the P/E.C. the memory accepts only the Reset (RST) command. Read of Data Polling bit DQ7 returns '0', then '1' on completion. The Toggle Bit DQ6 toggles during erase operation and stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because the erasure has not been verified even after the maximum number of erase cycles have been executed.

Table 12A. Read AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)(3)

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-70		-90		
				V_{CC} = 5V ± 5%		V_{CC} = 5V ± 10%		
				Standard Interface		Standard Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	70		90		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		70		90	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		70		90	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		30		35	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		20		20	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		20		20	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	20		20		ns

Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.
3. The temperature range –40 to 125°C is guaranteed at 70ns with High Speed Interface test condition and V_{CC} = 5V ± 5%.

Block Erase (BE) instruction. This instruction uses a minimum of six write cycles. The Erase Set-up command 80h is written to address 5555h on third cycle after the two coded cycles. The Block Erase Confirm command 30h is written on sixth cycle after another two coded cycles. During the input of the second command an address within the block to be erased is given and latched into the memory. Additional Block Erase confirm commands and block addresses can be written subsequently to erase other blocks in parallel, without further coded cycles. The erase will start after an Erase timeout period of about 100µs. Thus, additional Block Erase commands must be given within this delay. The input of a new Block Erase command will restart the timeout period. The status of the internal timer can be monitored through the level of DQ3, if DQ3 is '0' the Block Erase Command has been given and the timeout is running, if DQ3 is '1', the timeout has expired and the P/E.C is erasing the block(s). Before and during Erase timeout, any command different from 30h will abort the instruction and reset the device to read array mode. It is not necessary to program the block with 00h as the P/E.C. will do this automatically before erasing to FFh. Read operations after the sixth rising edge of $\overline{W}$ or $\overline{E}$ output the status register bits.

During the execution of the erase by the P/E.C., the memory accepts only the ES (Erase Suspend) and RST (Reset) instructions. Data Polling bit DQ7 returns '0' while the erasure is in progress and '1' when it has completed. The Toggle Bit DQ6 toggles during the erase operation. It stops when erase is completed. After completion the Status Register bit DQ5 returns '1' if there has been an Erase Failure because erasure has not completed even after the maximum number of erase cycles have been executed. In this case, it will be necessary to input a Reset (RST) to the command interface in order to reset the P/E.C.

Table 12B. Read AC Characteristics
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)

Symbol	Alt	Parameter	Test Condition	M29F040				Unit
				-120		-150		
				V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
				Standard Interface		Standard Interface		
				Min	Max	Min	Max	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	120		150		ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}		120		150	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{ELQV} (2)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G}$ = V_{IL}		120		150	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	$\overline{E}$ = V_{IL}		50		55	ns
t_{EHQX}	t_{OH}	Chip Enable High to Output Transition	$\overline{G}$ = V_{IL}	0		0		ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}$ = V_{IL}		30		35	ns
t_{GHQX}	t_{OH}	Output Enable High to Output Transition	$\overline{E}$ = V_{IL}	0		0		ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}$ = V_{IL}		30		35	ns
t_{AXQX}	t_{OH}	Address Transition to Output Transition	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IL}	20		20		ns

Notes: 1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Program (PG) instruction. The memory can be programmed Byte-by-Byte. This instruction uses four write cycles. The Program command A0h is written on the third cycle after two coded cycles. A fourth write operation latches the Address on the falling edge of $\overline{W}$ or $\overline{E}$ and the Data to be written on its rising edge and starts the P/E.C. During the execution of the program by the P/E.C., the memory will not accept any instruction. Read operations output the status bits after the programming has started. The status bits DQ5, DQ6 and DQ7 allow a check of the status of the programming operation. Memory programming is made only by writing '0' in place of '1' in a Byte.

Erase Suspend (ES) instruction. The Block Erase operation may be suspended by this instruction which consists of writing the command 0B0h without any specific address code. No coded cycles are required. It allows reading of data from another block while erase is in progress. Erase suspend is accepted only during the Block Erase instruction execution and defaults to read array mode. Writing this command during Erase timeout will, in addition to suspending the erase, terminate the timeout. The Toggle Bit DQ6 stops toggling when the P/E.C. is suspended. Toggle Bit status must be monitored at an address out of the block being erased. Toggle Bit will stop toggling between 0.1µs and 15µs after the Erase Suspend (ES) command has been written.

The M29F040 will then automatically set to Read Memory Array mode. When erase is suspended, Read from blocks being erased will output invalid data, Read from block not being erased is valid. During the suspension the memory will respond only to Erase Resume (ER) and Reset (RST) instructions. RST command will definitively abort erasure and result in the invalid data in the blocks being erased.

Figure 6. Read Mode AC Waveforms

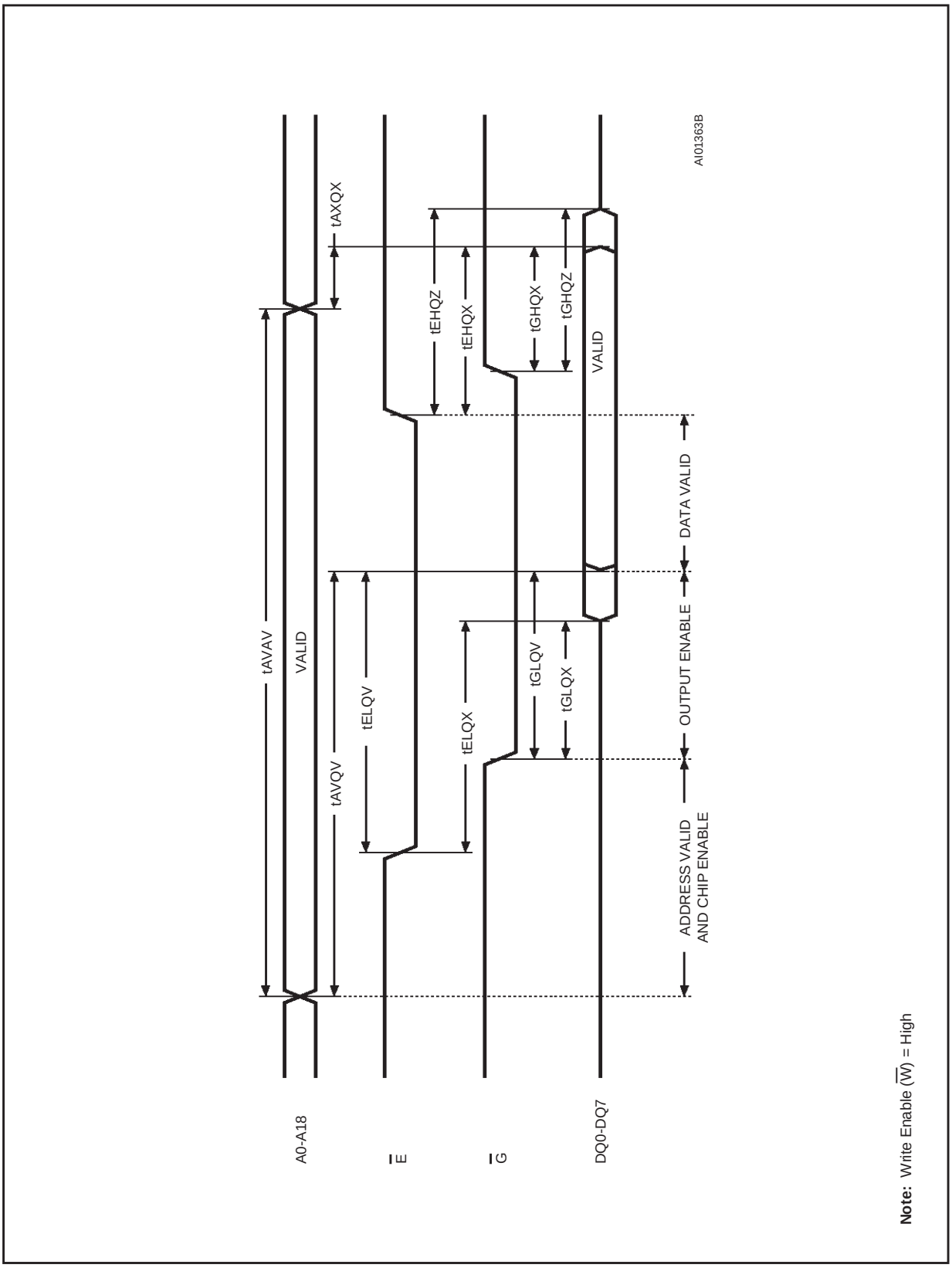


Table 13A. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)(2)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			Standard Interface		Standard Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	35		45		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	30		45		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	45		45		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$
2. The temperature range –40 to 125°C is guaranteed at 70ns with High Speed Interface test condition and V_{CC} = 5V ± 5%.

Erase Resume (ER) instruction. If an Erase Suspend instruction was previously executed, the erase operation may be resumed by giving the command 30h, at any address, and without any coded cycles.

Power Up

The memory Command Interface is reset on power up to Read Array. Either $\overline{E}$ or $\overline{W}$ must be tied to V_{IH} during Power-up to allow maximum security and the possibility to write a command on the first rising adge of $\overline{E}$ or $\overline{W}$. Any write cycle initiation is blocked when V_{CC} is below V_{LKO}.

Supply Rails

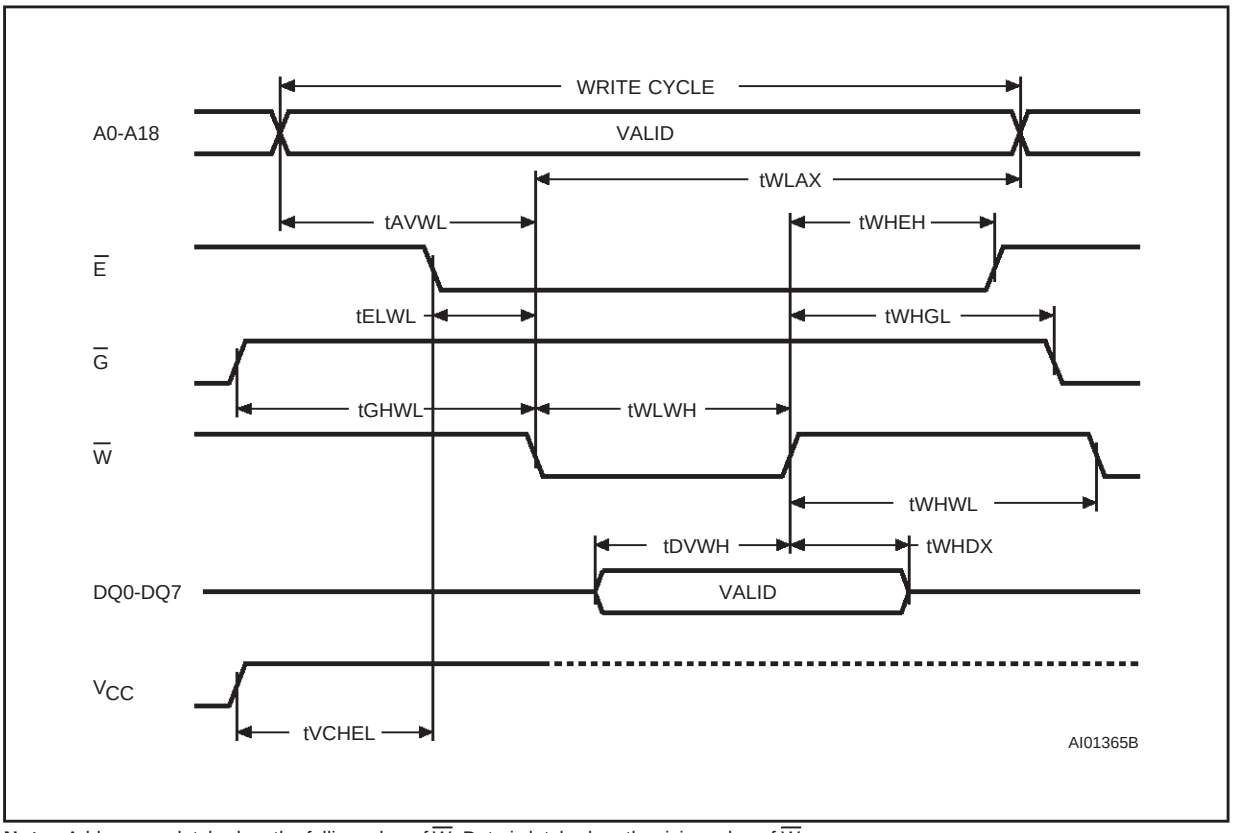
Normal precautions must be taken for supply voltage decoupling, each device in a system should have the V_{CC} rail decoupled with a 1.0µF capacitor close to the V_{CC} and V_{SS} pins. The PCB trace widths should be sufficient to carry the V_{CC} program and erase currents required.

Table 13B. Write AC Characteristics, Write Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			Standard Interface		Standard Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	0		0		ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	50		50		ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	50		50		ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	0		0		ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	0		0		ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	20		20		ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	0		0		ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	50		50		ns
t_{GHWL}		Output Enable High to Write Enable Low	0		0		ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	50		50		µs
t_{WHQV1} (1)		Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2} (1)		Write Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$

Figure 7. Write AC Waveforms, $\overline{W}$ Controlled



Note: Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.

Table 14A. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)(2)

Symbol	Alt	Parameter	M29F040				Unit
			-70		-90		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			Standard Interface		Standard Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	70		90		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	35		45		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	30		45		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	45		45		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

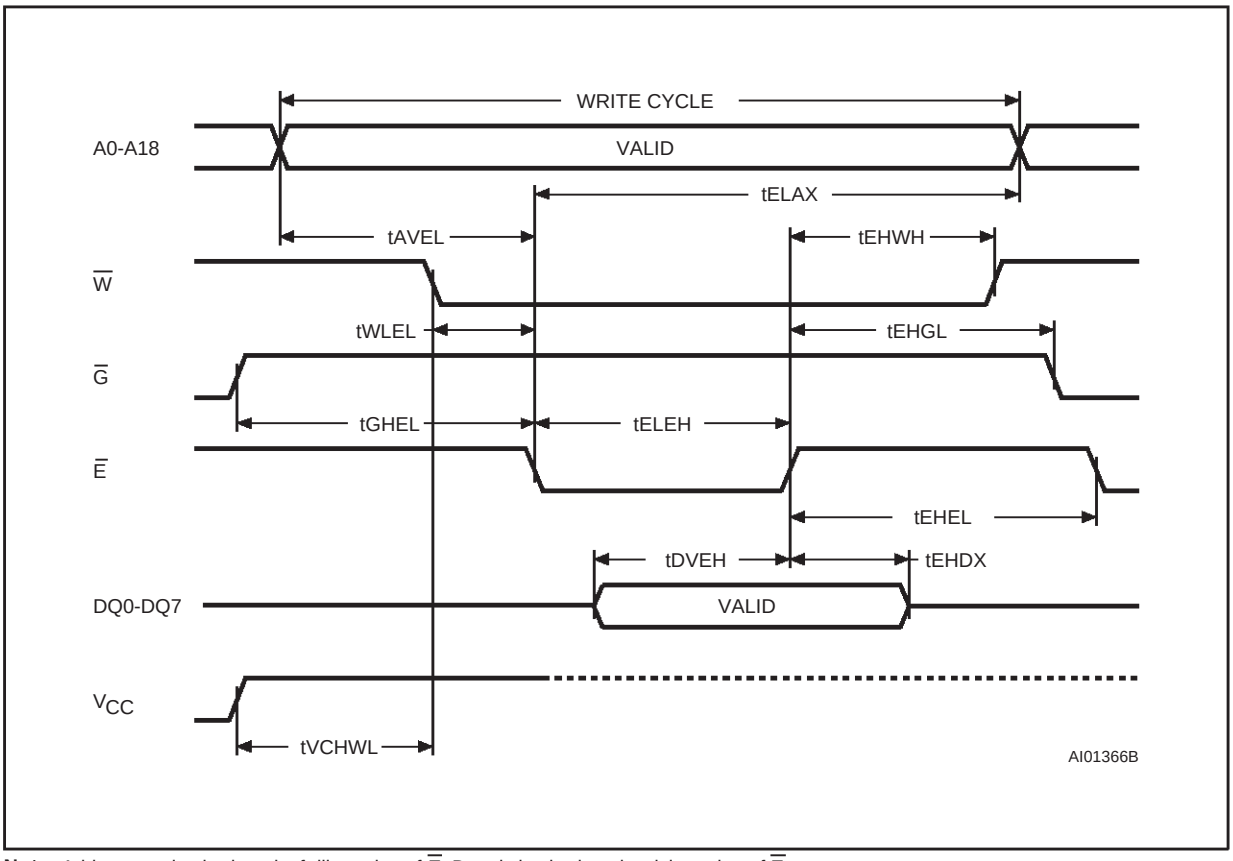
Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.
2. The temperature range –40 to 125°C is guaranteed at 70ns with High Speed Interface test condition and V_{CC} = 5V ± 5%.

Table 14B. Write AC Characteristics, Chip Enable Controlled
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)

Symbol	Alt	Parameter	M29F040				Unit
			-120		-150		
			V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
			Standard Interface		Standard Interface		
			Min	Max	Min	Max	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	120		150		ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	0		0		ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	50		50		ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	50		50		ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	0		0		ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	0		0		ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	20		20		ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	0		0		ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	50		50		ns
t_{GHEL}		Output Enable High Chip Enable Low	0		0		ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	50		50		µs
t_{EHQV1} (1)		Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2} (1)		Chip Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	0		0		ns

Note: 1. Time is measured to Data Polling or Toggle Bit, $t_{WHQV} = t_{WHQ7V} + t_{Q7VQV}$.

Figure 8. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

Table 15A. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)(3)

Symbol	Parameter	M29F040				Unit
		-70		-90		
		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
		Standard Interface		Standard Interface		
		Min	Max	Min	Max	
t_{WHQ7V1} (2)	Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10		10		µs
t_{WHQ7V2} (2)	Write Enable High to DQ7 Valid (Block Erase, $\overline{W}$ Controlled)	1.0	30	1.0	30	sec
t_{EHQ7V1} (2)	Chip Enable High to DQ7 Valid (Program, $\overline{E}$ Controlled)	10		10		µs
t_{EHQ7V2} (2)	Chip Enable High to DQ7 Valid (Block Erase, $\overline{E}$ Controlled)	1.0	30	1.0	30	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		30		35	ns
t_{WHQV1}	Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2}	Write Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec
t_{EHQV1}	Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2}	Chip Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec

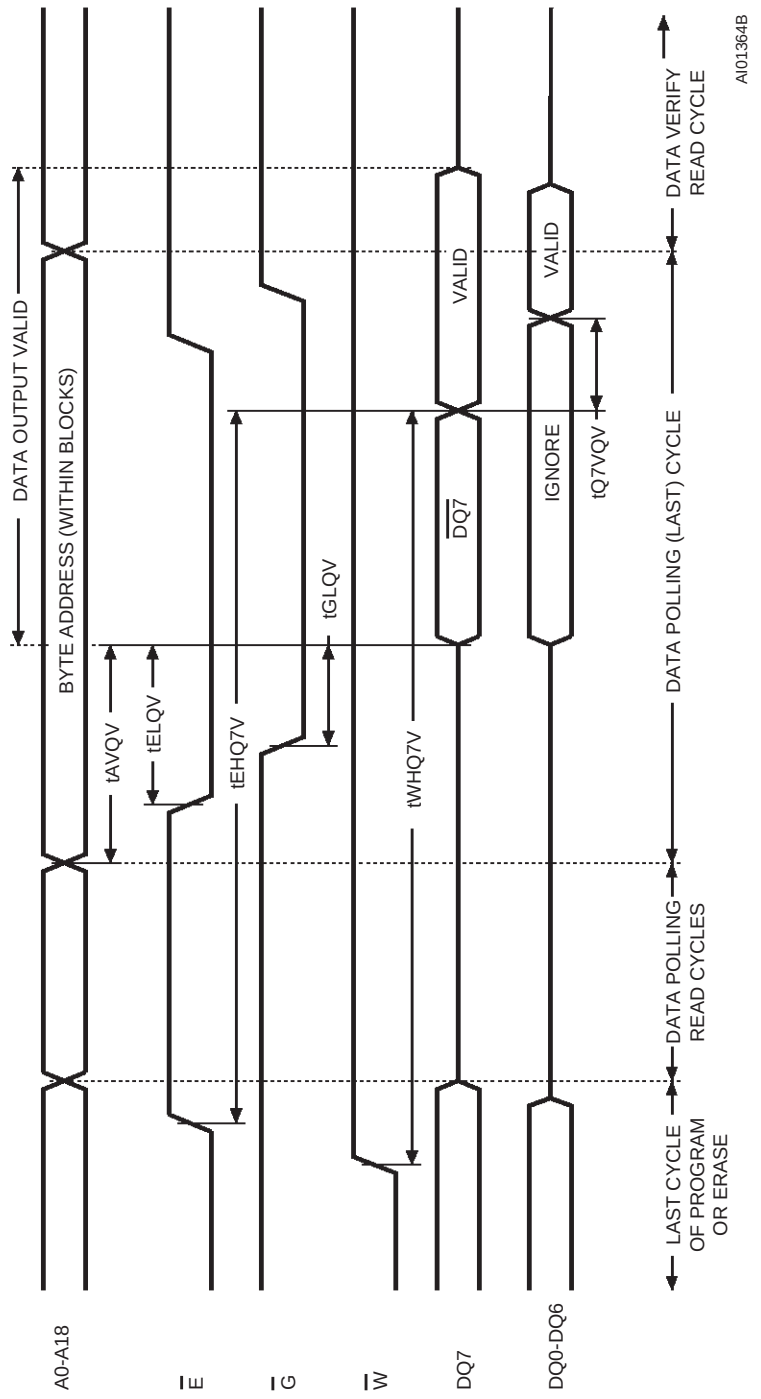
Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.
3. The temperature range –40 to 125°C is guaranteed at 70ns with High Speed Interface test condition and V_{CC} = 5V ± 5%.

Table 15B. Data Polling and Toggle Bit AC Characteristics (1)
(T_A = 0 to 70°C, –20 to 85°C, –40 to 85°C or –40 to 125°C)

Symbol	Parameter	M29F040				Unit
		-120		150		
		V_{CC} = 5V ± 10%		V_{CC} = 5V ± 10%		
		Standard Interface		Standard Interface		
		Min	Max	Min	Max	
t_{WHQ7V1} (2)	Write Enable High to DQ7 Valid (Program, $\overline{W}$ Controlled)	10		10		µs
t_{WHQ7V2} (2)	Write Enable High to DQ7 Valid (Block Erase, $\overline{W}$ Controlled)	1.0	30	1.0	30	sec
t_{EHQ7V1} (2)	Chip Enable High to DQ7 Valid (Program, $\overline{E}$ Controlled)	10		10		µs
t_{EHQ7V2} (2)	Chip Enable High to DQ7 Valid (Block Erase, $\overline{E}$ Controlled)	1.0	30	1.0	30	sec
t_{Q7VQV}	Q7 Valid to Output Valid (Data Polling)		50		55	ns
t_{WHQV1}	Write Enable High to Output Valid (Program)	10		10		µs
t_{WHQV2}	Write Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec
t_{EHQV1}	Chip Enable High to Output Valid (Program)	10		10		µs
t_{EHQV2}	Chip Enable High to Output Valid (Block Erase)	1.0	30	1.0	30	sec

Notes: 1. All other timings are defined in Read AC Characteristics table.
2. t_{WHQ7V} is the Program or Erase time.

Figure 9. Data Polling DQ7 AC Waveforms



Notes: 1. All other timings are as a normal Read cycle.
2. DQ7 and DQ0-DQ6 can transmit to valid at any point during the data output valid period.
3. tWHQ7V is the Program or Erase time.
4. During erasing operation Byte address must be within Block being erased.

Figure 10. Data Polling Flowchart

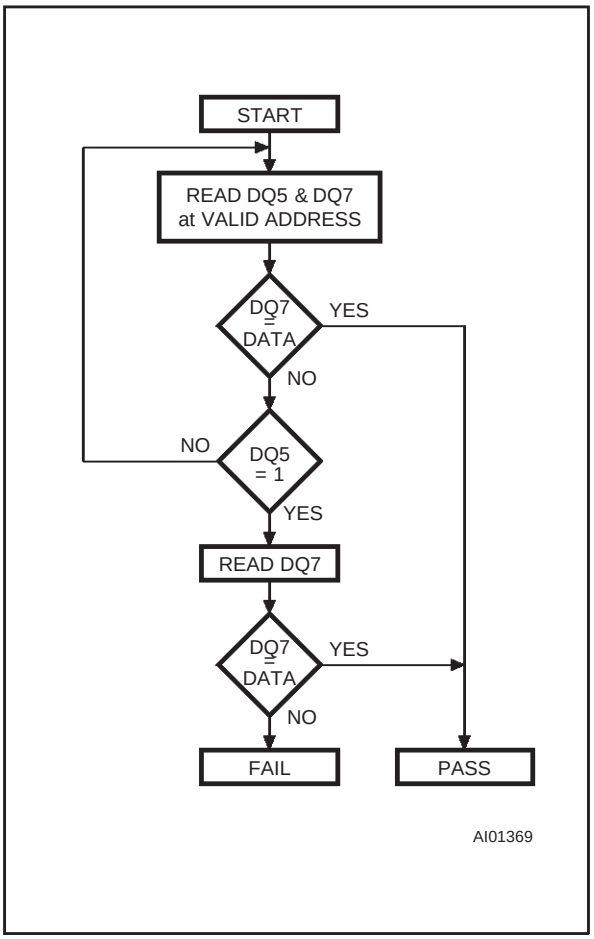


Figure 11. Data Toggle Flowchart

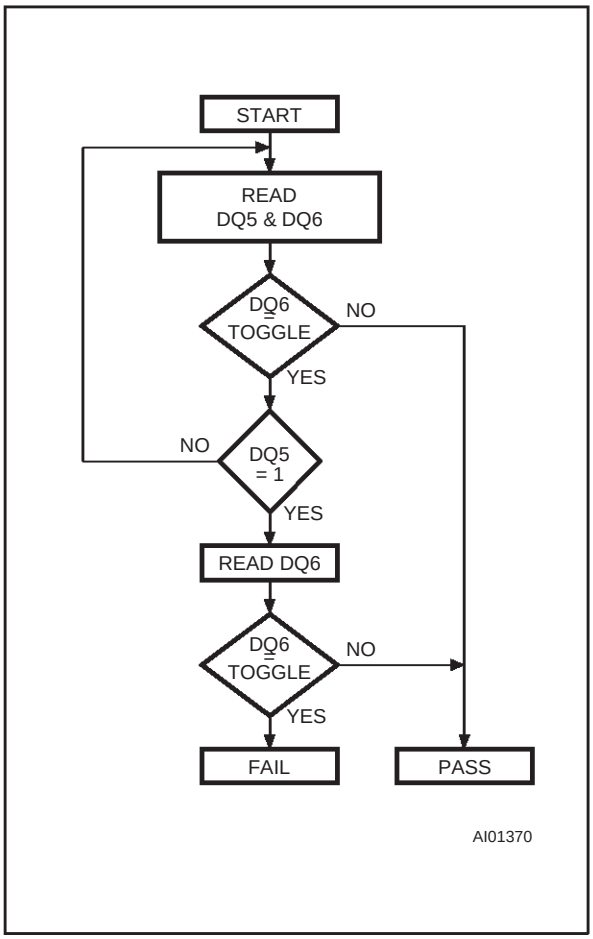
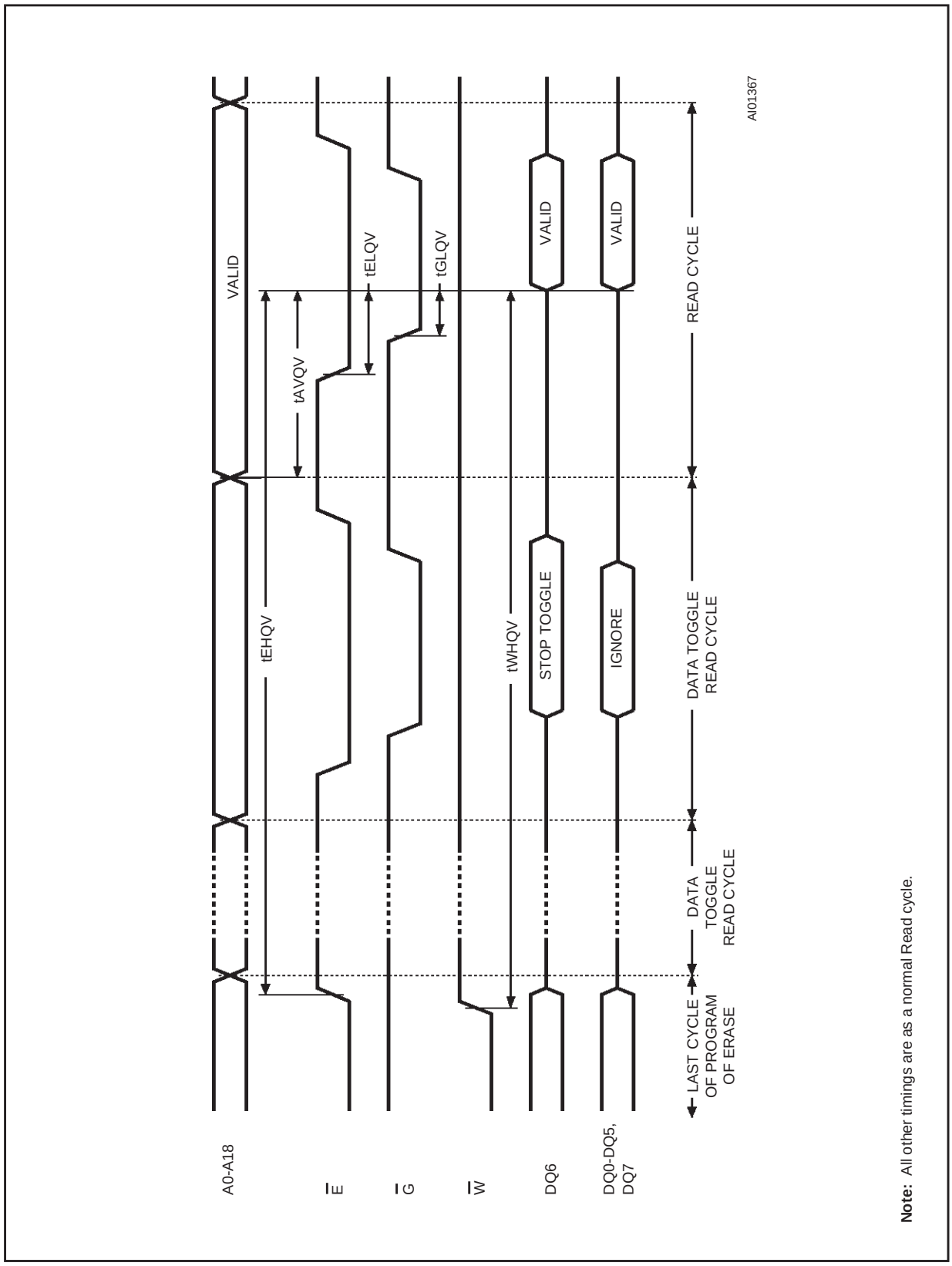


Table 16. Program, Erase Times and Program, Erase Endurance Cycles
(T_A = 0 to 70°C; V_{CC} = 5V ± 10% or 5V ± 5%)

Parameter	M29F040			Unit
	Min	Typ	Max	
Chip Program (Byte)		6		sec
Chip Erase (Preprogrammed)		2.5	30	sec
Chip Erase		8.5		sec
Block Erase (Preprogrammed)		1	30	sec
Block Erase		1.5		sec
Byte Program	10		1500	µs
Program/Erase Cycles (per Block)	100,000			cycles

Figure 12. Data Toggle DQ6 AC Waveforms



Note: All other timings are as a normal Read cycle.

Figure 13. Block Protection Flowchart

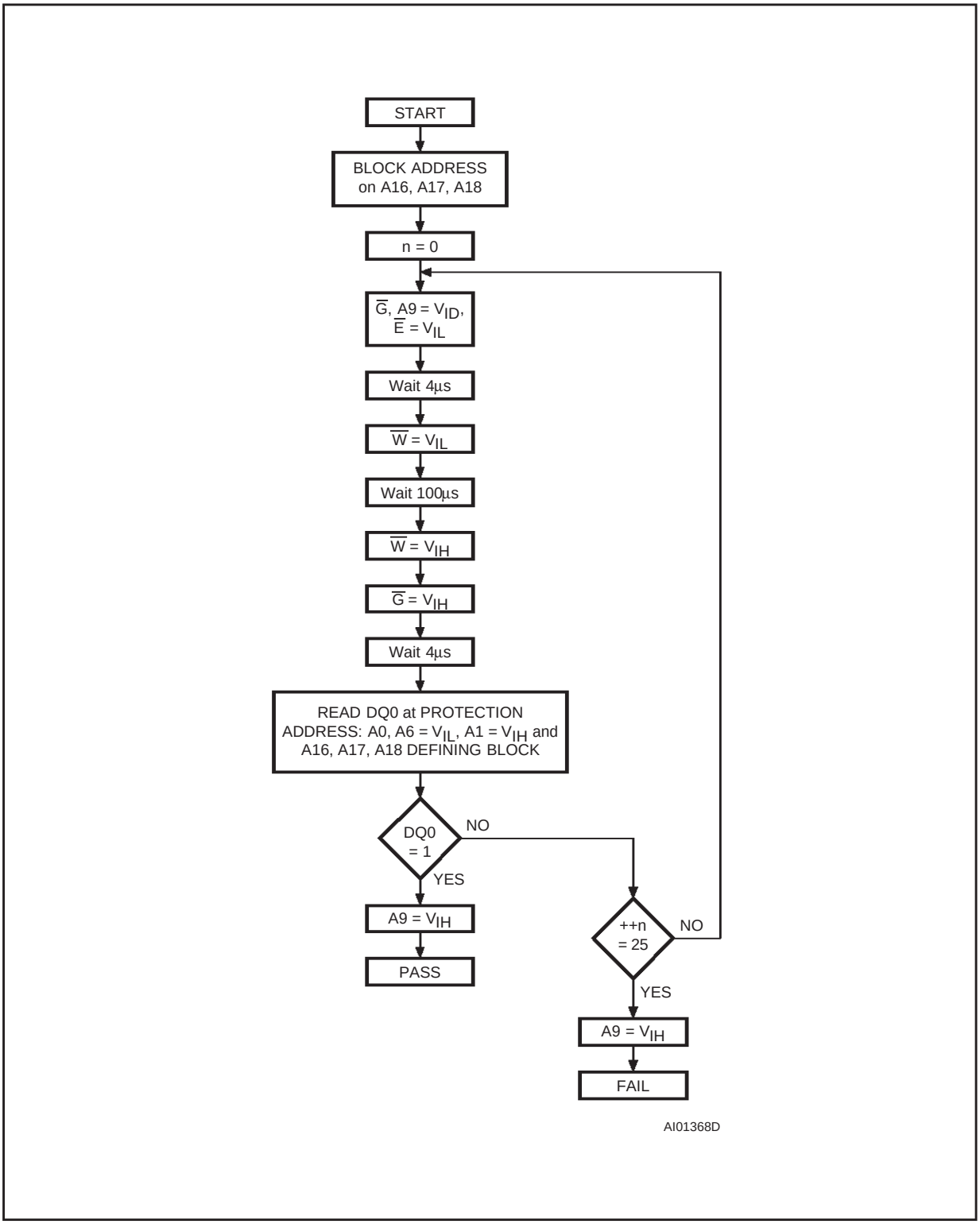
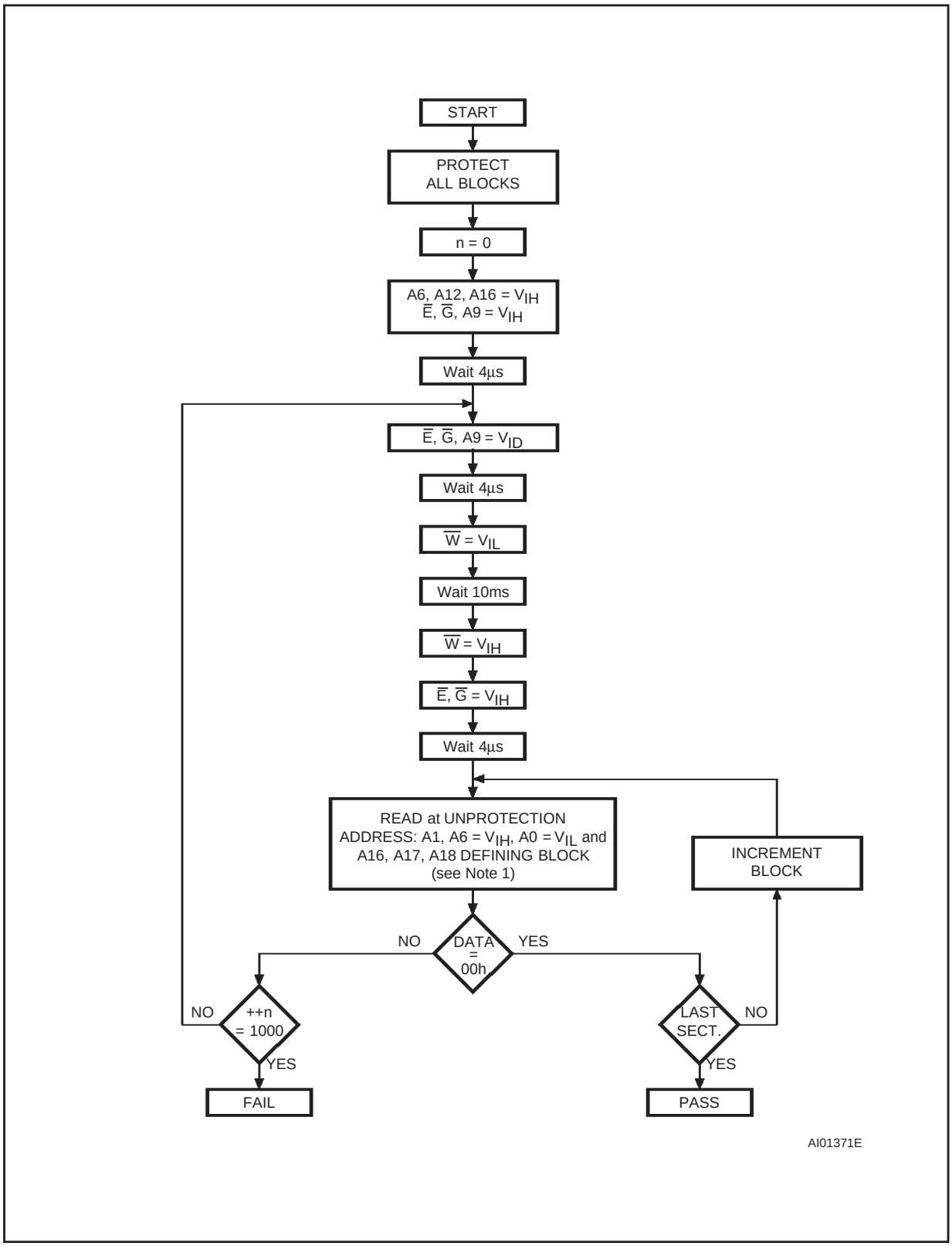
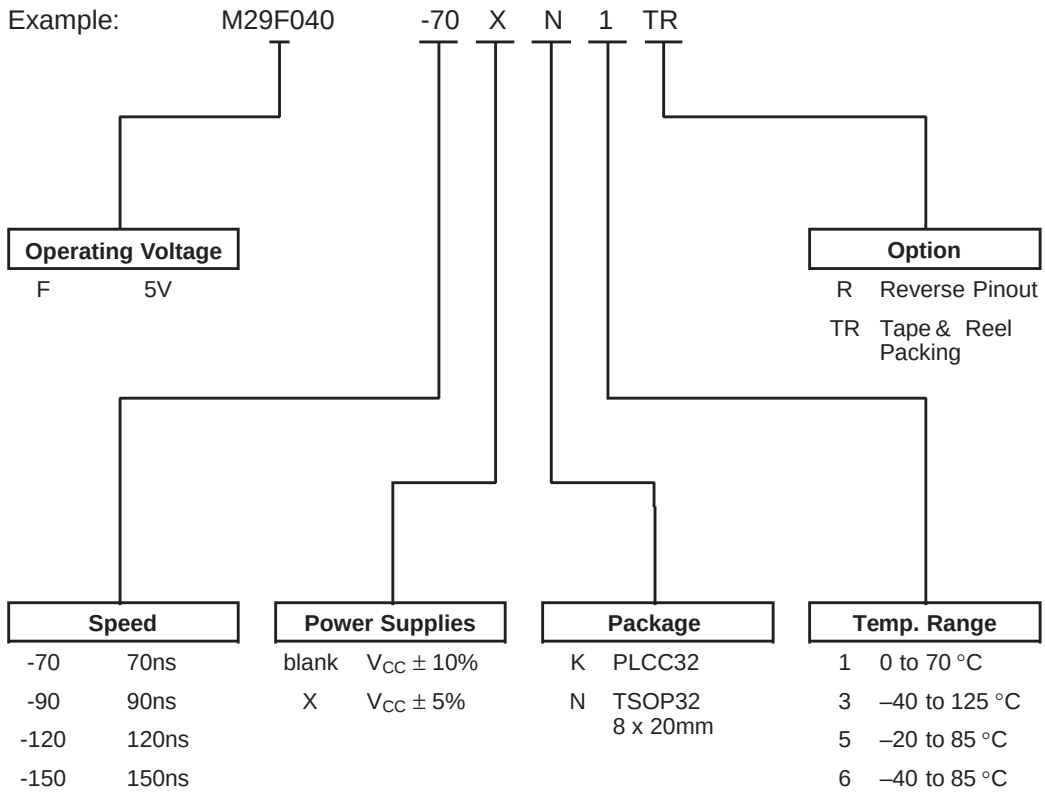


Figure 14. Block Unprotecting Flowchart



Note: 1. A6 is kept at V_{IH} during unprotection algorithm in order to secure best unprotection verification. During all other protection status reads, A6 must be kept at V_{IL}.

ORDERING INFORMATION SCHEME



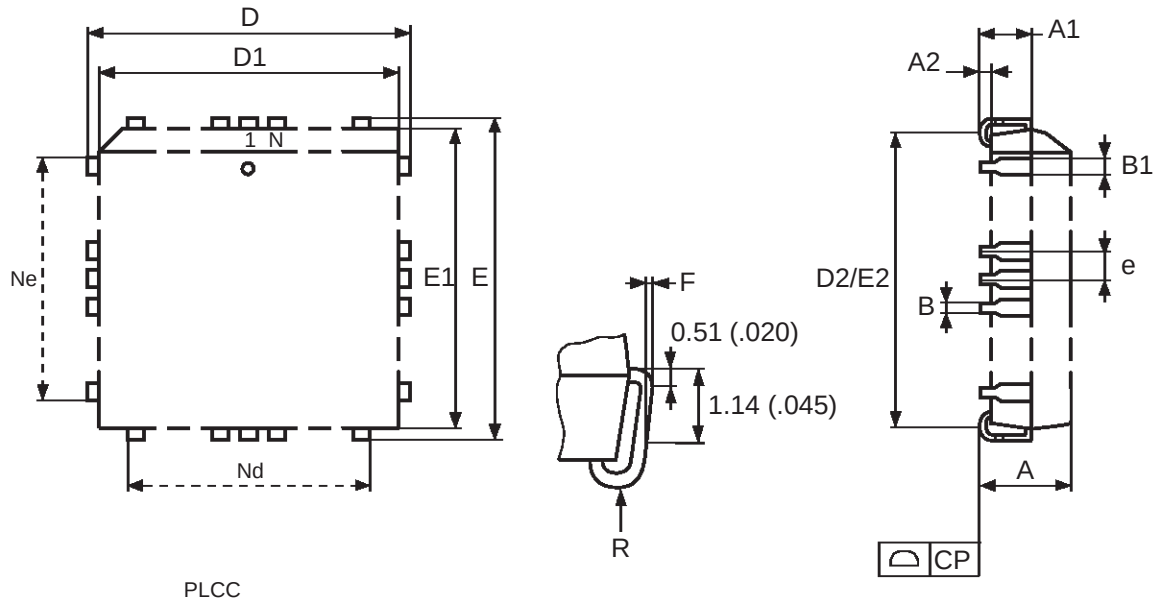
M29F040 is replaced by the new version M29F040B

Device are shipped from the factory with the memory content erased (to FFh).

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the STMicroelectronics Sales Office nearest to you.

PLCC32 - 32 lead Plastic Leaded Chip Carrier, rectangular

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		2.54	3.56		0.100	0.140
A1		1.52	2.41		0.060	0.095
A2		–	0.38		–	0.015
B		0.33	0.53		0.013	0.021
B1		0.66	0.81		0.026	0.032
D		12.32	12.57		0.485	0.495
D1		11.35	11.56		0.447	0.455
D2		9.91	10.92		0.390	0.430
E		14.86	15.11		0.585	0.595
E1		13.89	14.10		0.547	0.555
E2		12.45	13.46		0.490	0.530
e	1.27	–	–	0.050	–	–
F		0.00	0.25		0.000	0.010
R	0.89	–	–	0.035	–	–
N	32			32		
Nd	7			7		
Ne	9			9		
CP			0.10			0.004

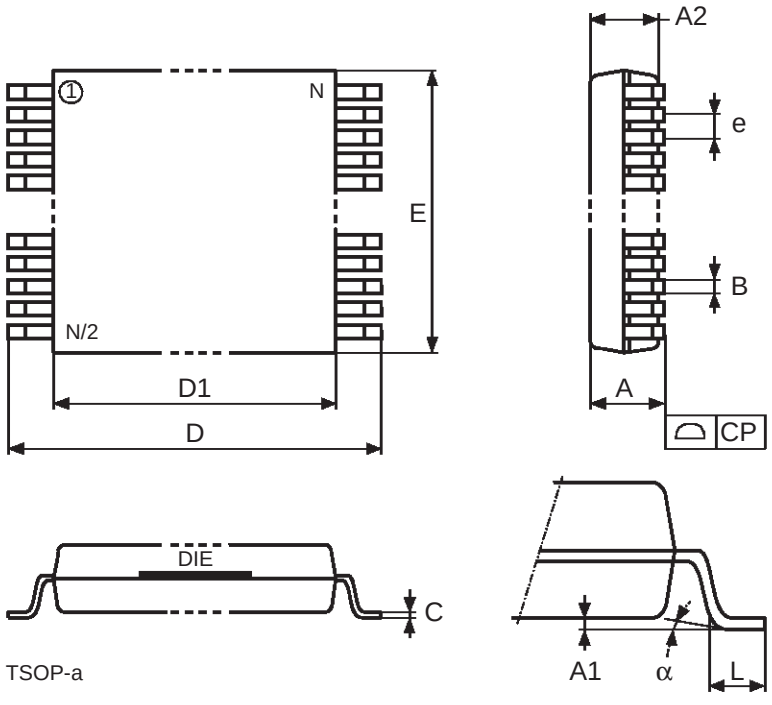


PLCC

Drawing is not to scale.

TSOP32 Normal Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.15		0.002	0.007
A2		0.95	1.05		0.037	0.041
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	-	-	0.020	-	-
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004

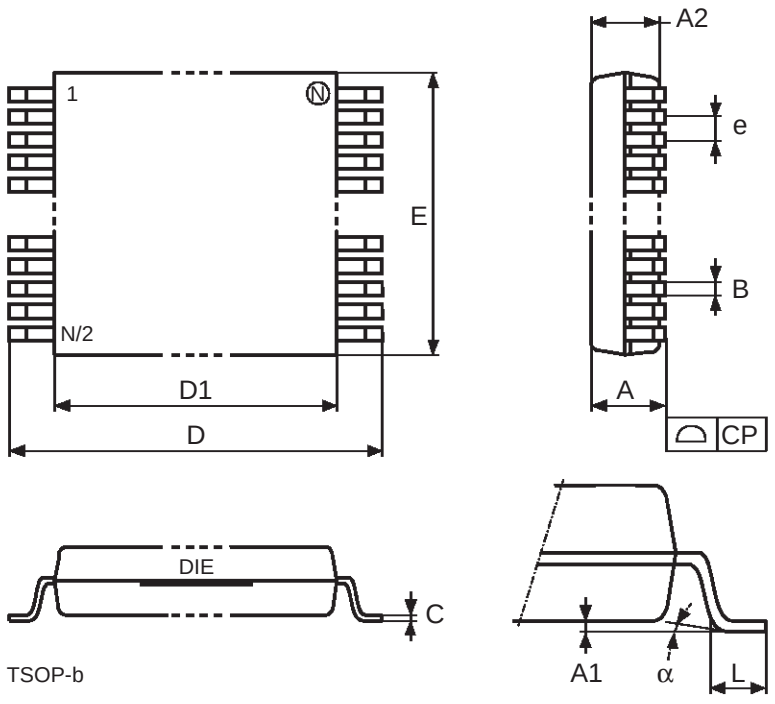


TSOP-a

Drawing is not to scale.

TSOP32 Reverse Pinout - 32 lead Plastic Thin Small Outline, 8 x 20mm

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1		0.05	0.17		0.002	0.006
A2		0.95	1.05		0.037	0.041
B		0.15	0.27		0.006	0.011
C		0.10	0.21		0.004	0.008
D		19.80	20.20		0.780	0.795
D1		18.30	18.50		0.720	0.728
E		7.90	8.10		0.311	0.319
e	0.50	–	–	0.020	–	–
L		0.50	0.70		0.020	0.028
α		0°	5°		0°	5°
N	32			32		
CP			0.10			0.004



TSOP-b

Drawing is not to scale.