SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

QUALITY AND RELIABILITY INFORMATION

by the Micro Divisions

INTRODUCTION

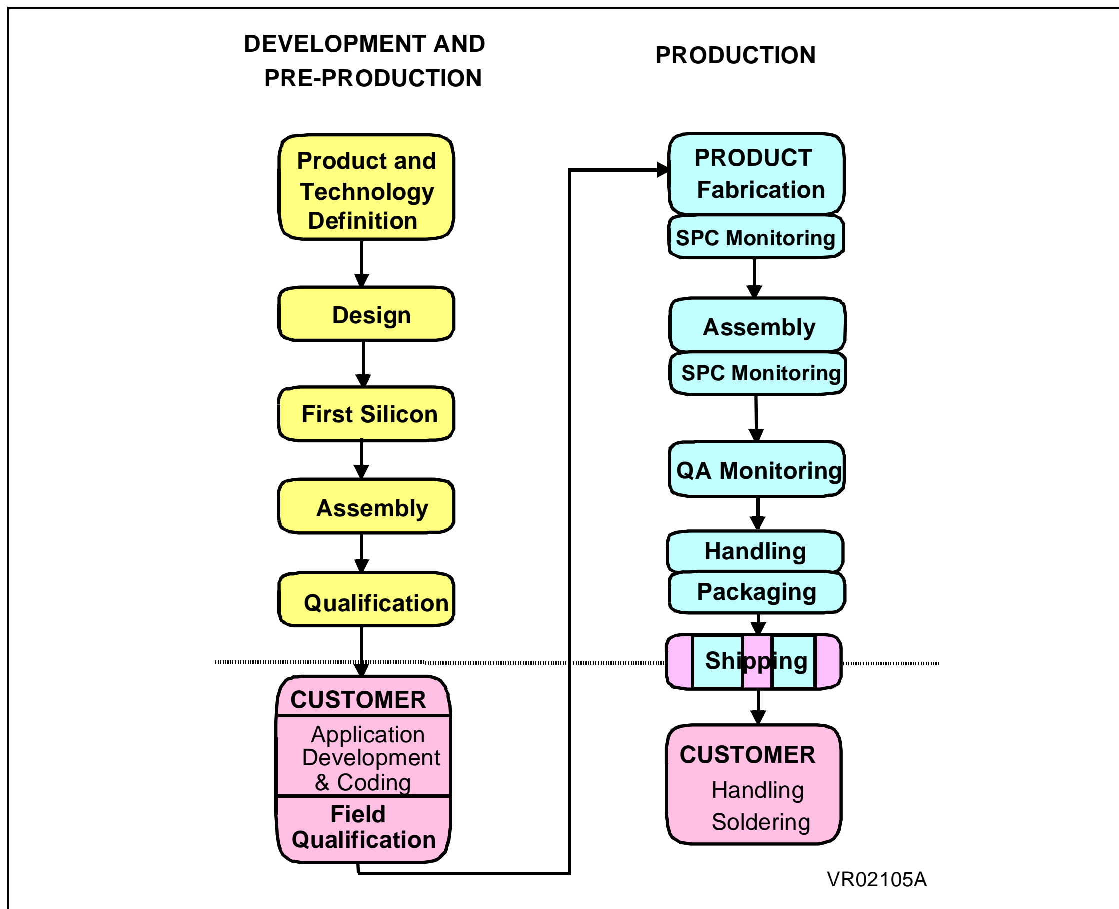
We think that maintaining an optimal quality level is very important but we also believe that our customers contribute to the quality chain when they handle or program our MCU devices This application note describes all the stages an SGS-THOMSON's product need to get over to be qualified, passing the various reliability tests.

1 QUALITY ASSURANCE

1.1 THE QUALITY CHAIN

The main steps of a product life cycle are summarized on the graph below. Quality is involved at each step but it is important to notice that the customer also has a major role in quality assurance

Figure 1. Main Steps of the Quality Chain

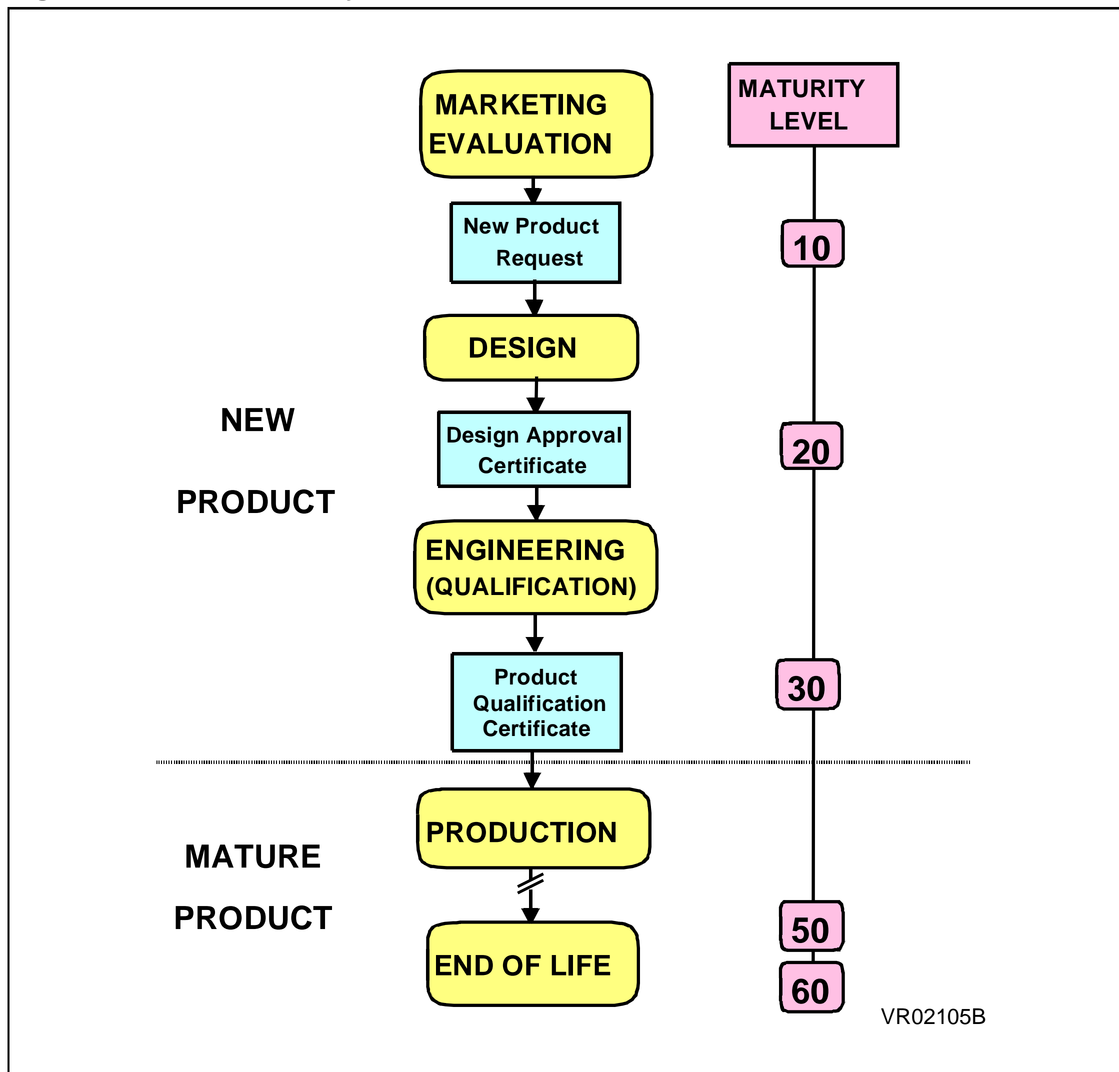


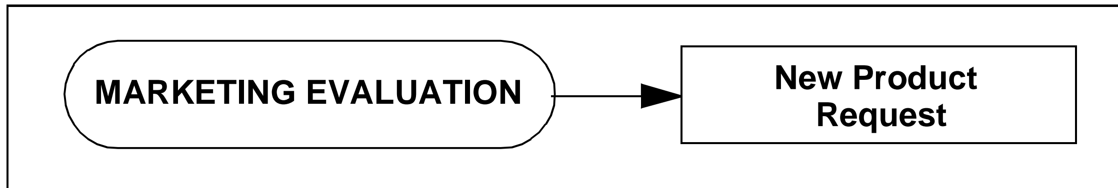
1.2 QUALITY SYSTEM AT SGS-THOMSON

A maturity number is attributed to each step of the development of a MCU device (design, industrialization or volume production). **Maturity** is an attribute assigned to each product that shows the status of knowledge reached on it and allows to follow its life cycle internally.

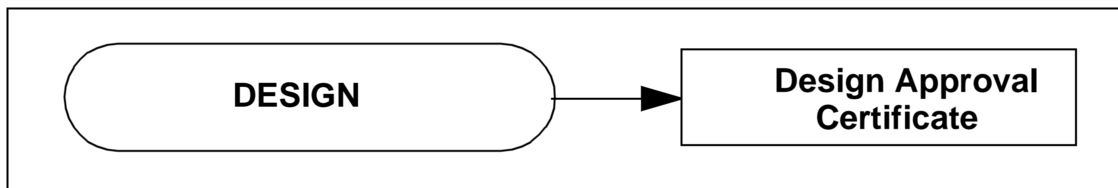
There are four main steps in a new product development: **marketing evaluation**, **design**, **engineering** and **production**. The table on page 4 gives a list of the requirements for each development level. The following procedure is for internal qualification and is applied to new generic semi-conductors products manufactured with a qualified wafer fabrication and assembly process.

Figure 2. Product Life Cycle

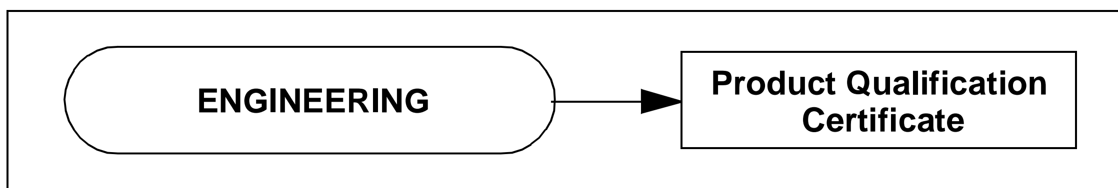




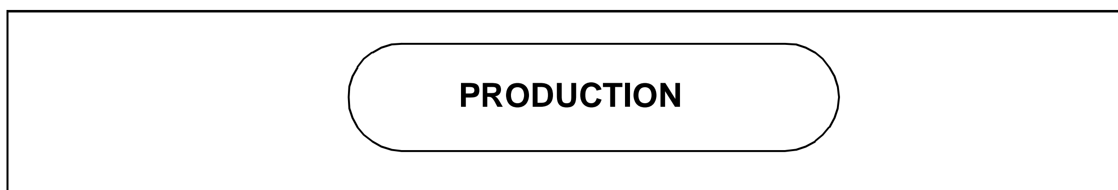
The reasons to develop a new MCU are market trends and specified requirements from our customers. They will be translated into a specification after additional technical and economical evaluation. To eventually start a new product development with this specification, SGS-THOMSON constitutes a development council to decide about the realization. The result will be fixed in the target specification, which contains the device functions, technology, and parameters as well as the **targets** for **quality and reliability**.



Design by CAD (Computer Aided Design) plays an important role in generating design quality for a new product. Since the introduction of CAD for the automation of design and its verification, the influence of computer based methods has reduced the amount of time required for a product design. In order to increase the level of performance, design methods are usually standardized.



Once a design successfully passes its review, a trial run takes place in which the product's electrical and mechanical characteristics, quality and reliability are evaluated. Additional runs are performed in which process conditions are varied deliberately, causing characteristic factors to change in mass production. These samples are evaluated to determine the best combination of process conditions but also to check the product behaviour inside the full specification range. Reliability tests are then conducted to check the new product's electrical and mechanical stress resistance. If no problems are found at this stage, the product is qualified and approved for mass production.



The standards for production and control steps are continuously re-examined for possible improvement, even after mass production has started. Quality controls and reliability monitoring are also performed.

Maturity Level	Project Details	Samples and Data	Ordering Parts
10	New product is designed to get full specifications samples	Free samples are delivered to selected customers	No orders can be entered
20	Product is characterised Reliability is measured	Samples to customers (not for qualification)	Order confirmation is not allowed. In device list with “Not to be Sold”
30	Product is manufactured and monitored to meet corporate standard	Process parameters stabilised and under company limits	The product is available through regular commercial system
50	Notification of the decision to stop the product to the customer		Order confirmation for limited period and controlled quantity
60	Product termination is completed Production of remaining orders		Order confirmation forbidden

1.3 STATISTICAL PROCESS CONTROL (SPC)

One of the most efficient tools implemented throughout the production of integrated circuits to control product quality and process stability is **SPC**. The goal of SPC is to bring each critical parameter to “6 Sigma” capability. In a typical wafer processing line, more than 200 variables may be controlled for SPC. Data is gathered and analysed by on-line computers and provides on-line control charts. The critical process steps are defined by FMEA (Failure Mode and Effects Analysis).

FMEA is a disciplined methodology to anticipate and evaluate potential failure modes and to define preventive actions that can be incorporated during development of a product or process. Thus costly field failures and redesigns can be easily avoided.

A selection of the most important SPC steps is regularly available and can help customers to avoid the costly qualification of new products when the products come from a qualified manufacturing process that is demonstrated to be under control.

1.4 FAILURE ANALYSIS

Failure Analysis Request (FAR) is a request made by a customer for the analysis of components delivered by the company that are claimed to have failed during customer usage. In order to allow SGS-THOMSON to quickly analyse the possible failure cause, the following elements must be included for each Failure Analysis Request:

– The detailed description of the symptoms for **each device**.

– The conditions and the step of occurrence:

° Incoming inspection

° Programming stage

° Manufacturing stage

° Field

° Reliability trials

° Engineering trials

– The **failure rate**.

– A sample of MCU devices affected by the problem. For OTP devices, a good part must also be shipped with the bad ones to allow comparison (code,...).

Parts are then analysed and an analysis report is issued. The failure analysis cycle time from FAR to the final date of report issued by quality organization in charge of FAR processing is detailed on the following graph.

Figure 3. FAR Information Flow

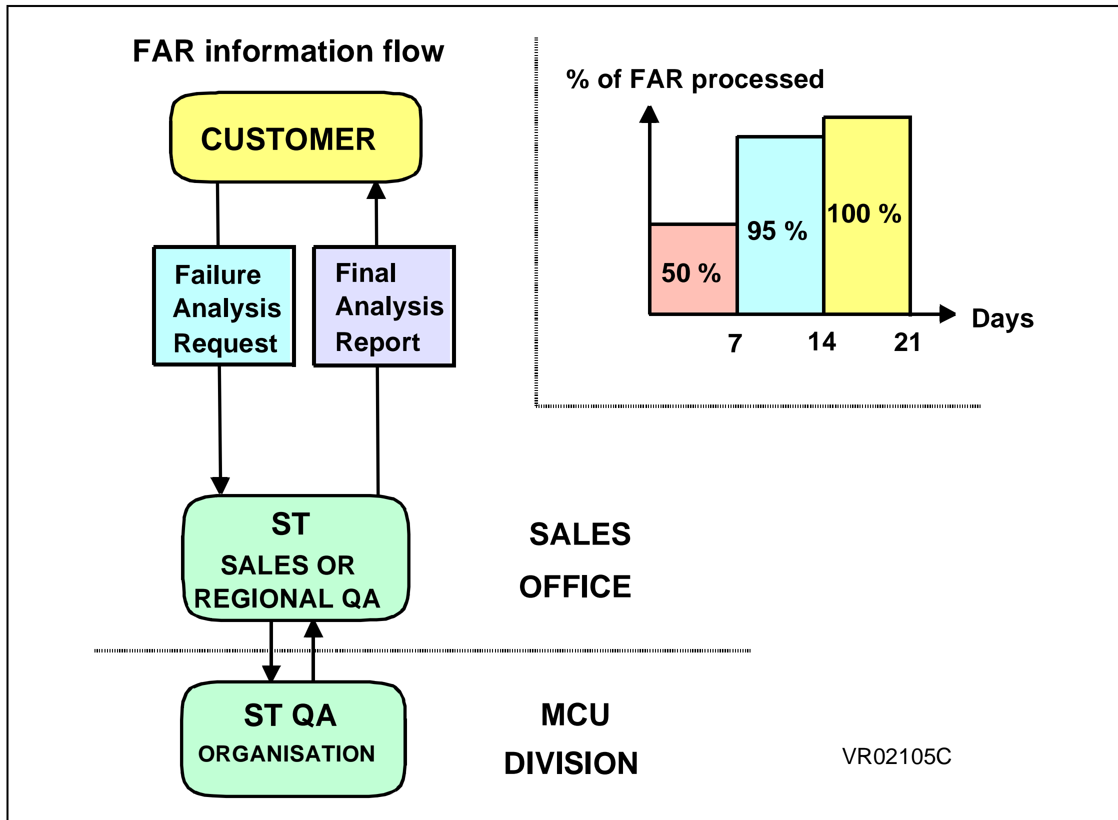
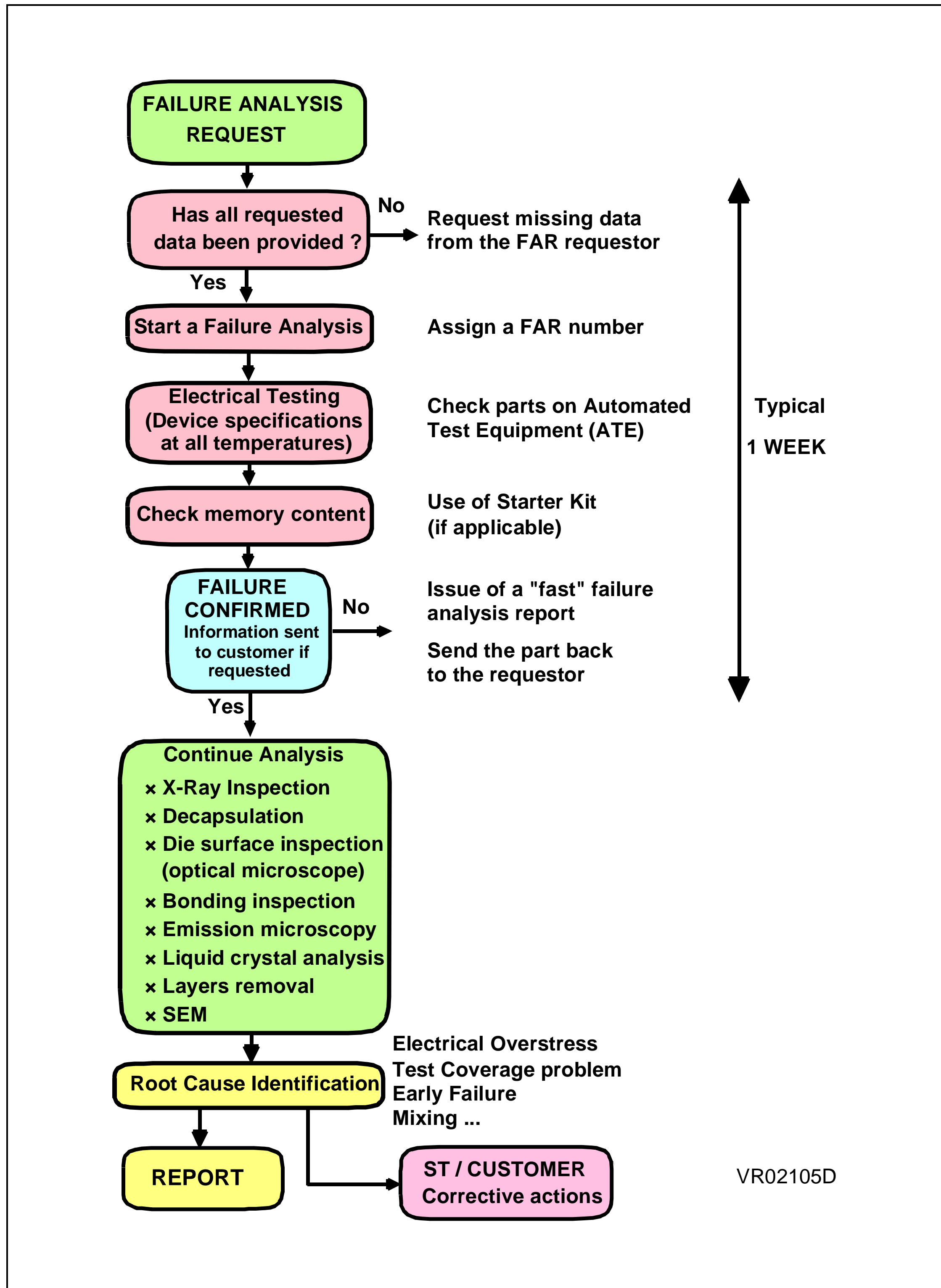


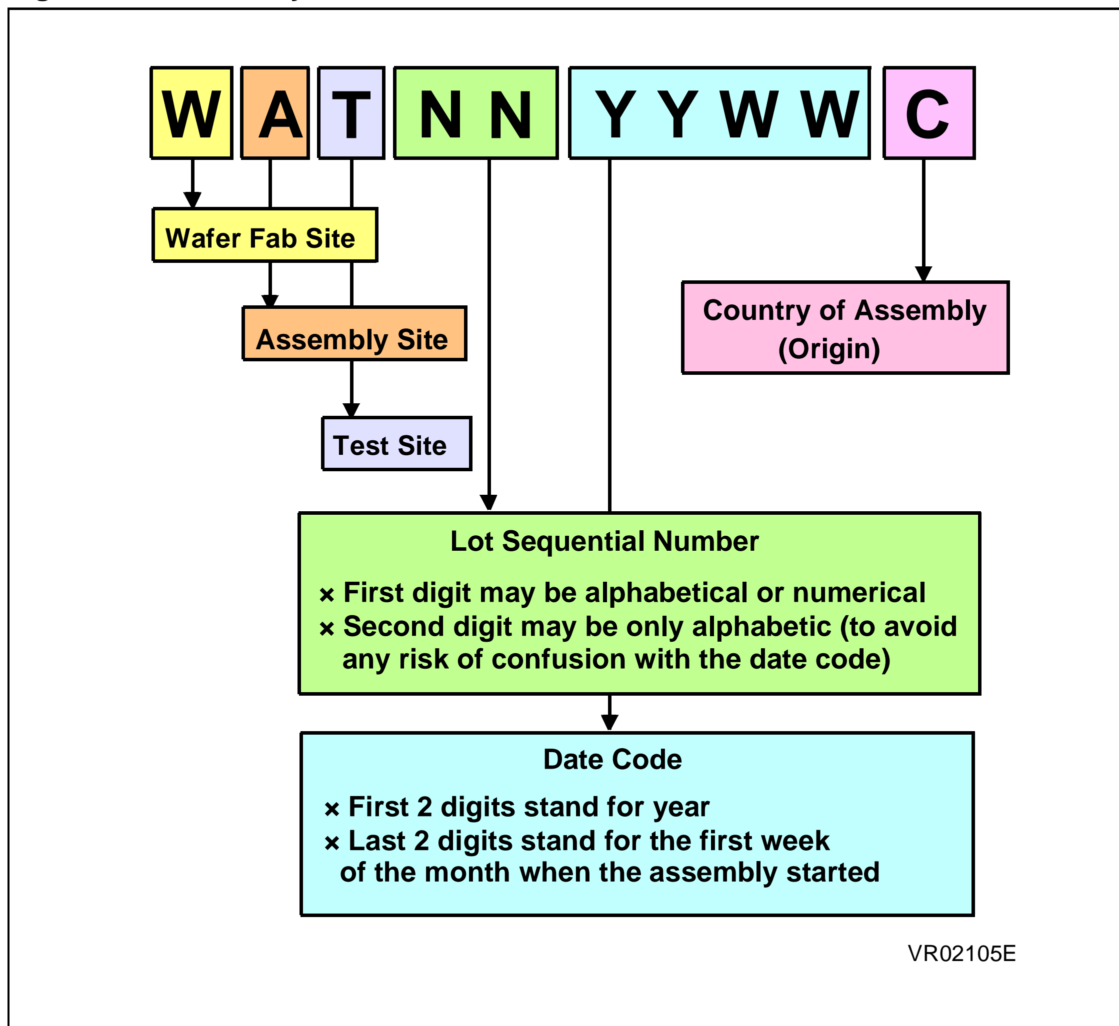
Figure 4. FAR Processing Flow



1.5 TRACEABILITY

At the end of the assembly stage, each component is marked with a traceability code. Traceability is a method enabling to reconstruct the individual history of any component manufactured in company plants. Traceability records are maintained to trace back the component's history. Details on technology, technical and electrical data, quality performance, key dates and sites where operations are performed are therefore recorded using traceability codes.

Figure 5. Traceability Code



The first nine digits are printed on the inner box label, with a space to emphasis the date code for clarity: **WATNN YYWW**.

Data records provide, as a minimum, 5 years traceability for each product after the last shipment.

Here are the tables for the first three digits (these lists are just an extract for 8 bits MCU products taken from the full lists. Contents are also subject to change without notice):

WAFER SITES CODES (FIRST DIGIT)				
CODE	**Location**	**Country**	**Wafer Dimension**	**Company**
G	Rousset	France	5 “	SGS-THOMSON
H	Carrolton	U.S.A.	6 "	
W	Ang Mo Kio	Singapore	5 “	
4.00	Rousset	France	6 “	
V	Agrate	Italy	6 “	

ASSEMBLY SITES CODES (SECOND DIGIT)			
CODE	**Location**	**Country**	**Company**
2.00	Kirkop	Malta	SGS-THOMSON
5.00	Hong-Kong	Hong-Kong	ASAT
9.00	Muar	Malaysia	SGS-THOMSON
B	Manila	Philippines	ANAM
P	Seoul	Korea	ANAM
N	Nancy	France	ASAT
A	Taipeh	Taiwan	ASE

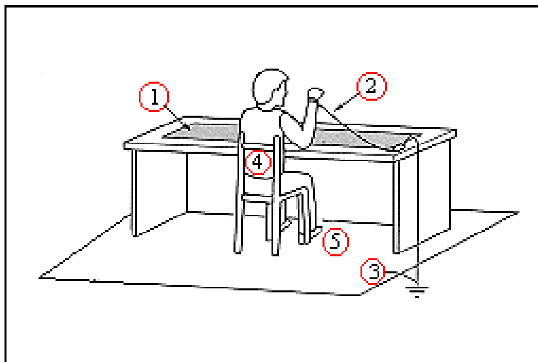
TEST SITES CODES (THIRD DIGIT)			
CODE	**Location**	**Country**	**Company**
2.00	Kirkop	Malta	SGS-THOMSON
9.00	Muar	Malaysia	SGS-THOMSON
E	Rousset	France	SGS-THOMSON

1.6 ELECTROSTATIC DISCHARGE PROTECTION AND HANDLING PRECAUTIONS

Electronic components have to be protected from the hazard of **static electricity** from the manufacturing stage down to where they are utilized. MOS devices are typically voltage and electrical field sensitive: the thin oxide layers can be **destroyed** by an electrical field. This happens mostly because a charged conductor, typically a person, is rapidly discharged through the device. A specific no-compromise strategy is implemented at SGS-THOMSON for all ESD sensitive products.

From the wafer level to the shipping of finished goods, each workstation and processing step is guaranteed. For final packing SGS-THOMSON uses anti-static tubes. This solution assures full ESD protection of devices. However, the supplier's greatest efforts are in vain if the **end user** does not provide the **same level of protection and care** in application.

A relative humidity of **50% to 65%** will be the best to prevent electrostatic problems (the lower the relative humidity, the higher the electrostatic voltage). Nevertheless, the person handling the semiconductors as well as the equipment will be charged to a certain level. The work environment is very important to protect devices against static electricity.



Anti-static electricity measures during work

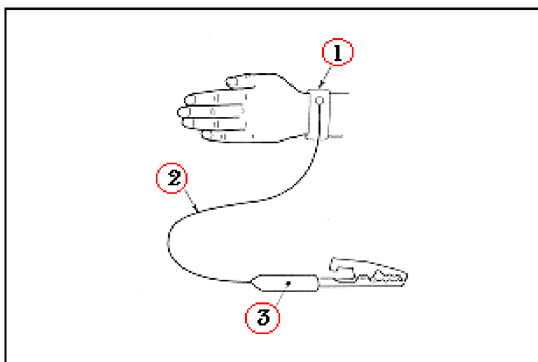
(1) Conductive mat

(2) Wrist strap

(3) Conductive floor mat

(4) Work suit with anti-static measure

(5) Conductive shoes Grounding the human body



Grounding the Human Body

(1) Wrist ring

(2) Grounding wire: threaded copper wire, vinyl covered, about 1 meter

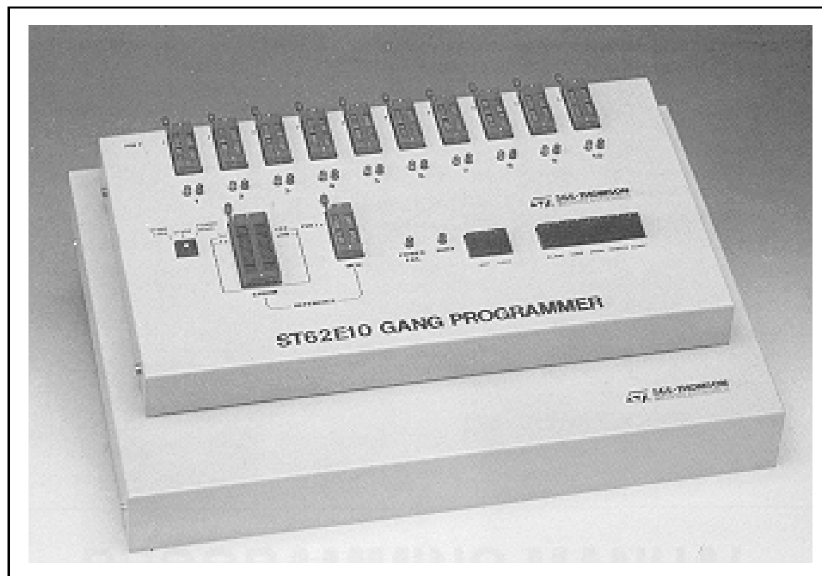
(3) 250 KΩ to 1 MΩ resistance is built in

The following are the basic static control protection rules:

	ANTI-STATIC MEASURES
DEVICE HANDLING	Static control wrist straps, used and connected properly, must be worn. All tools, persons, testing machines, which could come in contact with device leads, must be conductive and grounded. Each table top must be protected with a conductive mat, properly grounded. Use static control shoe strap. Use vacuum pipes.
STORAGE BOX	Keep parts in the original packing bags up to the very last moment of the production line. If bigger containers are used for in-plant transport of devices or PC boards, they must be electrically conductive like the carbon loaded types. Avoid use of high dielectric materials (like polystyrene) for sub-assembly construction, storing, transportation.
EQUIPMENT AND TOOLS	Use Ionized air blowers to neutralize static charges of non-conductive materials. Use only the grounded tip variety of soldering iron. Use proper power supply systems in testing and application. Supply voltage should be applied before and removed after input signals. Insertion and removal from sockets should be carried out with no power applied. Filtration, noise suppression, slow voltage surges should be guaranteed on the supply lines. An open (floating) pin is a potential hazard to the circuit. Each pin should be grounded or connected to V_{DD} through a resistance whenever possible.

1.7 PROPER USE OF GANG PROGRAMMERS

Gang programmers are designed for programming up to 10 EPROM or OTP devices at a time. It can run either in standalone or remote mode under control of a DOS compatible PC.



Gang programmers are used to program thousands of EPROM or OTP devices every day. Great care has to be taken when handling and removing programmed devices. The following precautions must also be taken to decrease OTP failures rates:

	PRECAUTIONS
POWER SUPPLY	Power supply must be grounded. A power regulator or an AC filter must be used to regulate the incoming voltage.
DUST PROTECTION	Clean sockets every day. Use covers at the end of the day to protect sockets from dust.
MISC	Respect a maximum number of 10 000 insertions / socket before changing sockets.

2 RELIABILITY TESTS

2.1 DEFINITION

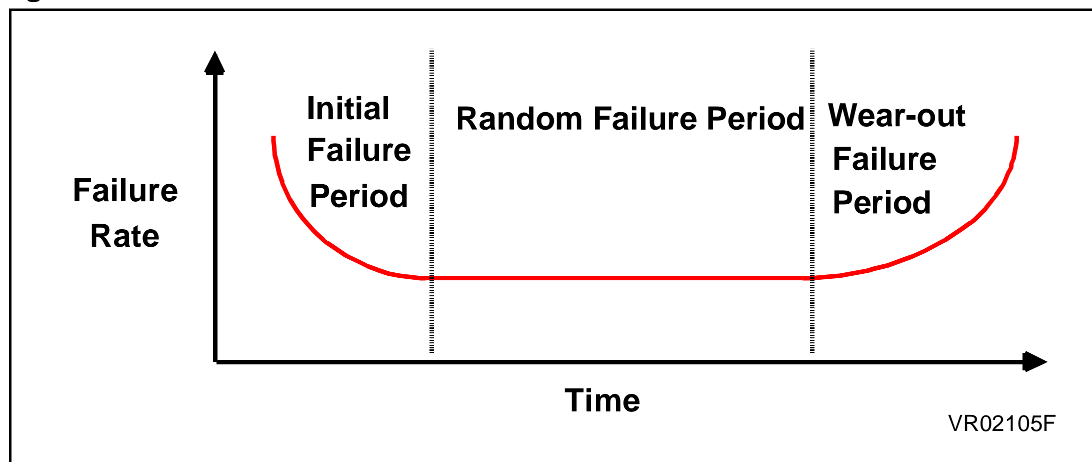
Reliability is the probability of a system or circuit performing its predefined function adequately under specific conditions for a given period of time. Thus, the reliability of a microcircuit is a function of both stress conditions and the time of operation.

The **failure rate** is the rate at which failures occur on units surviving to a specific number of hours of operation. Failure rates per component-hours (i.e. number of hours of operation multiplied by the number of components) would generally be very small. To avoid reporting such small numbers, failure rates have been defined for greater component-hours. The unit used to define failure rate is called **FIT**, and it represents the **absolute failures per billion component-hours**. A failure rate of 0.1% / 1 000 000 component hours and 1 FIT are equivalent numbers.

Failure rate over time: the bathtub curve

The generic representational graph of failure rate vs. time takes the shape of a bathtub curve. The **early failure rate** (infant mortality) period starts from initial operation and decreases as time goes on. The next phase of the curve is a very long period of time where failure rate is nearly constant and very low. After this long period, the failure rate starts to increase slowly. This last phase is known as the **wear-out period**.

Figure 6. Failure Rate over Time



Temperature dependency

In order to access reliability in a reasonable time, it is necessary to accelerate the incidence of the failure modes. Higher environmental stress levels than those encountered under normal conditions are needed. The most employed accelerating parameter is temperature, although voltage and humidity, for example, are also used. This is also done to simulate the behaviour of the component during its use under various conditions.

The **reliability tests** are conducted on samples picked up from the current production. They are also performed to validate some major changes in the process related to the design, the wafer fabrication or the assembly. In addition, new products introduction is always evaluated by several reliability tests which stress the devices to be sure that the production will be safe. Real Time Control tests are performed by our assembly sites to check that there are no deviations in their production. If a deviation occurs this kind of tests allows to react immediately and to take corrective actions.

2.2 DIE ORIENTED TESTS

HIGH TEMPERATURE OPERATING LIFE TEST (HTOL)

This test is the most die oriented test because it simulates the operation of the device inside its application. The aim of this test is to check the ability of the die to be fully functional for a very long period (i.e. more than 9 years). The life cycle of the device has to be long enough and the only way to check it efficiently (i.e. within a reasonable time frame for both supplier and customer) is by realizing this kind of accelerated test.

HTOL is the **most generally accepted** accelerated life test because high temperature is known to accelerate many physical and chemical reactions, leading to accelerated device failure. Devices are loaded on burn-in boards designed to exercise the device circuit and placed in a chamber at elevated temperature.

TEST CONDITIONS	
Power Supply	Supply Voltage + 20%
Oven Temperature	140 ° C
Duration	504 hours

RETENTION BAKE

This is an accelerated test aimed to evaluate the ability of the memory cells to retain the programmed data. Non volatile memory is programmed and devices are loaded in a chamber at high temperature without any bias. High temperature will give the charges enough energy to move from the floating gate, therefore leading to a retention failure.

TEST CONDITIONS	
Power Supply	No Bias
Oven Temperature	150 ° C
Duration	1008 hours

ELECTRICAL CYCLING ENDURANCE

This test is aimed to verify the Erase / Write capability of the EEPROM memory. Erase / Write cycles are performed at room temperature and are followed by a retention bake at 150 °C.

TEST CONDITIONS / PROCEDURE
300 000 cycles of Erase / Write
Retest of the EEPROM functionality and programmation
168 hours of retention bake at 150 ° C
Verification of the EEPROM contents

ELECTROSTATIC DISCHARGE (ESD) TEST

CMOS devices are very sensitive to electro-static discharges. All components are designed to withstand normal amounts of electrostatic discharge during assembly, test and handling by the customer. Two ESD standards are used: the human body model and the machine model.

Each trial consists of 3 positive pulses and 3 negative pulses separated by 1 second and is performed on three parts for each of the following configurations:

– Electrical pulse between all pins referenced to all grounds

– Electrical pulse between all pins referenced to all power supplies

– Electrical pulse between each pin (except power supplies and grounds) referenced to all other pins connected together

HUMAN BODY MODEL	MACHINE MODEL
R = 1.5 KΩ and C = 100 pF	R = 0 Ω and C = 200 pF
3 positive pulses + 3 negative pulses separated by 1 second	
Device has to pass 2000 V	Device has to pass 300 V

LATCH-UP TEST

Latch-up is caused by turning on the parasitic PNPN structure in CMOS circuits, due to a noise pulse, junction breakdown, or power supply transient overshoot. This will cause the circuit to malfunction temporarily or go into a destructive mode. There are 3 main tests, and each test is given a class letter (A, B or C) depending of the obtained result (A for the best result and C for the worst).

Overvoltage on power supplies: this test simulates an user induced situation where a transient over voltage is applied on power supply.

Current injection: this test simulates an user or application induced situation where either applied voltage on any pin is greater than V_{DD} or where severe overshoot occurs on inputs.

Power supply sequence: this test simulates an user induced situation where a hazardous power supply sequence is applied to the component (board plug-in application when power supply is on).

The final class for the device is the worst class among these three tests.

2.3 PACKAGE ORIENTED TESTS

THERMAL CYCLING

This test is made to determine the resistance of devices to exposure at temperature extremes, and especially to alternating extremes. This is also a worst case simulation of systems like cars, where the chip is exposed at very low temperatures during night and to high temperature when the car engine is running. Temperature cycling failures are mainly caused by problems due to different thermal expansion coefficients between: die, die attach, lead frame or mould compound.

AIR TO AIR TEMPERATURE CYCLING	
Maximum Temperature	+ 150 ° C
Minimum Temperature	- 40 ° C
Cycle Time	30 minutes
Duration	1000 cycles

THERMAL SHOCK

Thermal shock is the most extreme case of temperature transition: this accelerates any stress related failures with the rapidly changing gradient. That test is very close to thermal cycling, the main difference being the short temperature transition time obtained by dipping the devices in liquid. This test is specially aimed at ceramic packages.

LIQUID TO LIQUID CYCLING	
Maximum Temperature	+ 125 ° C
Minimum Temperature	- 55 ° C
Transfer Time	10 seconds maximum
Duration	100 shocks

TEMPERATURE AND HUMIDITY TEST

The temperature and humidity test is generally accepted throughout the industry as the standard test for plastic package integrity, especially pertaining to moisture penetration. In this test, devices are loaded on boards designed to bias the device with minimum power dissipation (to minimize the drying effect) in a chamber at high temperature and humidity.

TEST CONDITIONS	
Power Supply	Supply Voltage + 10%
Oven Temperature	85 ° C
Relative Humidity	85%
Duration	1008 hours

PRESSURE POT

Pressure pot test determines the survival capability of devices in moulded plastic packages to a hot, humid environment. The test exposes unbiased, plastic packaged devices to saturated steam at 121 ° C and 2 ATM gauge pressure. Pressure and the 240 hours of testing allow moisture to penetrate into the die. Chemical corrosion of the die metallization may occur if contaminants are present due to passivation layer damage.

TEST CONDITIONS	
Oven Temperature	121 ° C
Relative Humidity	100%
Oven Pressure	2 ATM
Duration	240 hours

RESISTANCE TO SURFACE MOUNTING

The purpose of this test is to determine the resistance of devices to new techniques of surface-mount technology for assembling integrated circuits on printed boards. Pop-corn effect is the cracking of the package during the soldering cycle which can compromise the integrity of surface-mount packages like SOP, PLCC or PQFP. Cracks may occur in the moulding compound, depending on the absorbed moisture level, soldering temperature and time, die size, package structure and moulding compound characteristics.

TEST CONDITIONS / PROCEDURE
(1) Temperature and Humidity Test
85 ° C No Bias
85% RH 96 hours
5.5 V
(2) Solder dipping
T = 215 ° C, 120 s
(T = 260 ° C, 10 s for SO packages)
85 ° C
(3) Visual inspection for cracks on body
Electrical Test
85%
(4) Pressure Pot Test
(121 ° C / 2 ATM / 96 hours)
1000 hours
(5) Electrical Test

SOLDERABILITY

The purpose of this test is to verify the solderability behaviour of the products (i.e. the ability of the tin leads to be soldered on the customer's board).

TEST CONDITIONS
(1) Aging
16 hours / 155 ° C in dry air for SMD
8 hours steam aging for other plastic packages
5.5 V
(2) Solder dipping
T = 215 ° C (+/- 3 ° C), 3 s for SMD
T = 245 ° C (+/- 5 ° C), 5 s for other plastic packages
85 ° C
Inspection criteria: 95% coverage minimum

GLOSSARY

EOS	**E**lectrical **O**ver**S**tress. This expression summarizes all defects generated by the application of electrical conditions which are at least for one parameter out of specification. The main failure modes observed are damaged, melted, or burned out wires.
ESD	**E**lectro**S**tatic **D**ischarge. The discharge of two differently charged elements might result in a discharge process when the elements are touching each other or electric fields influence the charge. Due to the high charge voltages, semi-conductor structures can be damaged or destroyed along the path of discharge. Main failure modes observed are increased leakage currents of input circuits and damaged input buffer structures.
Failure Analysis	A post mortem examination of failed devices for the purpose of verifying the reported failure and identifying the mode or mechanism of the failure.
FIT	**F**ailure **I**n **T**ime. It is the unit of the failure rate. One fit is equal to one defect within one billion device hours.
PPM	**P**arts **P**er **M**illion, also defects per million. It is used as a unit to define a defect rate.
Screening	100% testing of a device, as opposed to sampling.
SPC	**S**tatistical **P**rocess **C**ontrol. Used to control the quality of the mass production process by statistical methods when process capability studies have been successful (based on pre-production data).

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