SGS-THOMSON MICROELECTRONICS

APPLICATION NOTE

STV0196 - DIGITAL SATELLITE RECEIVER LINK I.C.

CONTENTS **Page**

I - INTRODUCTION

This note is mainly focused on the carrier and timing loops hardware and software implementation. Limited mentions are given about the forward error correction (FEC), as this section is widely frozen by the structure of the STV0196 circuit.

This note is relevant to STV0196, STV0196B, STV0196C

II - STV0196 IN A SATELLITE RECEIVER FRONT-END

In a satellite receiver application, the STV0196 is implemented between the tuner and the MPEG2 demultiplexer (Transport IC) (see Figure 1).

Since the STV0196 is a fully digital integrated circuit an analog to digital conversion is required between the tuner and the STV0196. Due to the structure of the STV0196 the A/D conversion is run at twice the symbol rate Fs. The recommanded converter is STV0190 (conversion speed till 60Mbps, and supply voltage : 3.3V).

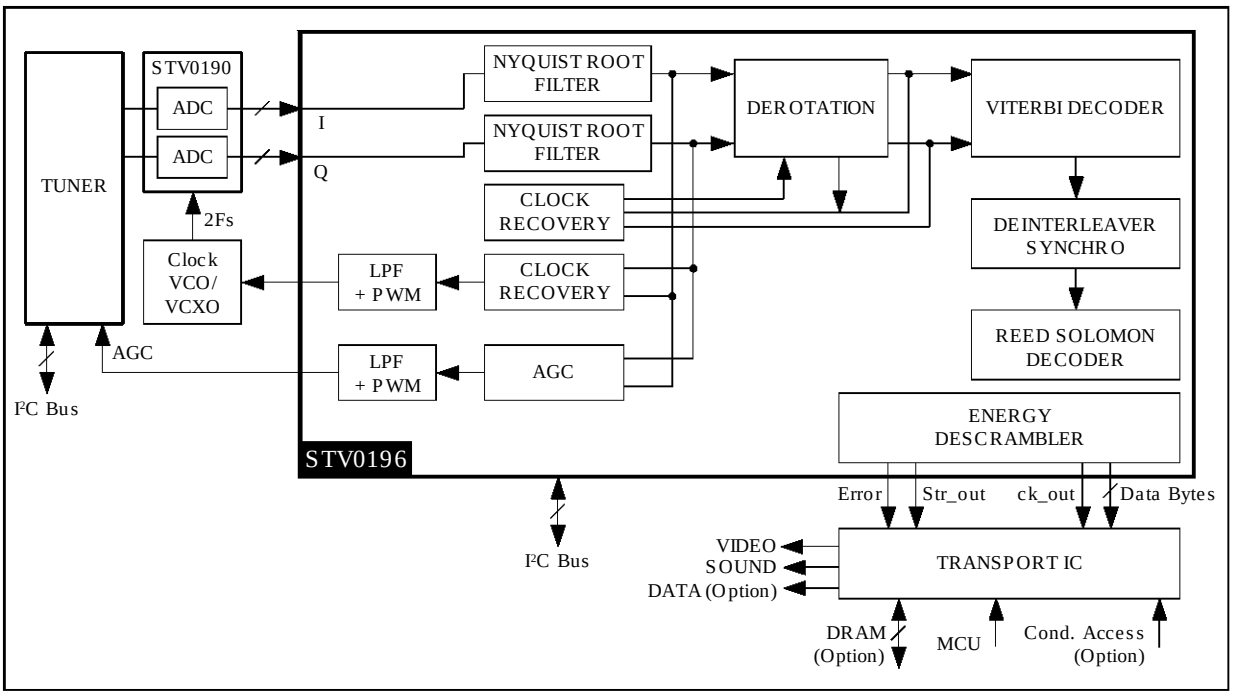
The STV0196 realises all the required channel demodulation and correction functions defined in the digital satellite broadcast systems :

- Root Nyquist filtering
- Carrier and timing recovery
- QPSK demodulation
- C/N estimation (option of the STV0196B and STV0196C)
- Forward error correction :
  - Viterbi decoding with puncture rate recognition
  - De-interleaver
  - Synchronization word recognition
  - Reed-Solomon decoding
  - Energy descrambling

Interface with the demultiplexer :
The output data are corrected bytes (of 8 bits), additionnaly the STV0196 supplies all required control signals for the demultiplexer :

- Error flag : Error
- Packet clock : D/P
- Synchro byte clock : STR_OUT
- Energy descrambler : CK_OUT

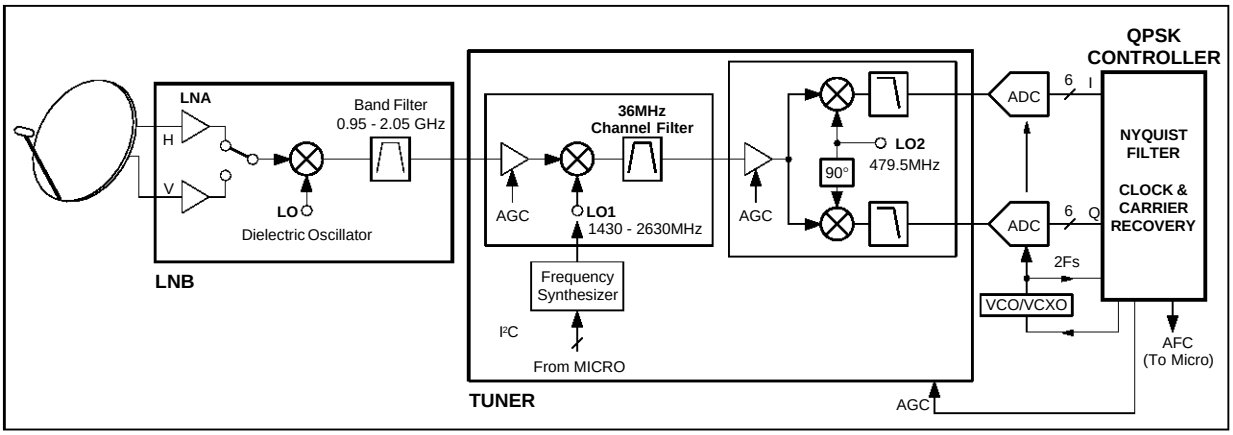
Figure 1 : STV0196 in a Sattelite Receiver Front-end



II - STV0196 IN A SATELLITE RECEIVER FRONT-END (continued)

More details about the timing and carrier recovery : The Figure 2 gives the complete structure of the front-end part of a satellite receiver from the LNB till the FEC.

Figure 2 : Front-end Block Diagram



The main components and signals are :

1 The RF Signal

The RF signal is broadcasted in the C or Ku bands.

The modulation is QPSK. This signal is mainly characterized by a low Carrier to Noise ratio (C/N).

The energy per bit Eb compared to the noise density No (Eb/No) can be in the 4 to 5dB range.

2 LNB (outdoors unit)

- The signal polarization selection (Horizontal/ Vertical ...)
- Low noise amplification and band pass filtering
- A frequency down-conversion, for each RF signal, the down converted frequency f_{CH} is :

  $f_{CH} = f_{RF} - f_{LO}$

  f_{LO} : LNB local oscillator frequency (typ. values : 9.75 or 10.75GHz).

Remark : The local oscillator frequency is subject to dispersions and drifts (wide ambiant operating temperature range). So that the total offset is about ± 3 to ± 5MHz.

3 Tuner

- Individual channel selection (mixing with a PLL controlled oscillator LO1)
- Channel filtering with selective SAW filter centered on a 479.5MHz intermediate frequency (2 SAW filters may be required to accomodate a wide range of channel bandwidth).
- I/Q splitting : I and Q demodulation is done with a second oscillator LO2 which is not frequency and phase controlled.
- Gain control : to accomodate a wide RF power range (typically : -65dBm till -20dBm). To automatically control the amplitude of the I/Q analog signals, this gain control is combined with the STV0196 AGC function to realize a closed loop.

4 A/D Conversion

The analog I and Q signals delivered by the tuner are converted into 6 bits words. The conversion frequency is 2Fs. The sampling clock is generated by a VCXO (fixed rate applications) or a VCO (multirate applications) which is controlled by the timing recovery function of the STV0196.

II - STV0196 IN A SATELLITE RECEIVER FRONT-END (continued)

5 Clock and Carrier Recovery Functions

Those functions are embedded in the STV0196. In addition to the explanations and descriptions given in the STV0196 specification, this section gives further characterisitics which explain how the STV0196 can retreive the data even in the worst conditions :

- ***AGC Function :***

  This function is combined with gain control of the tuner to realize a closed loop.

  More precisely the AGC function calulates the modulus of the constellation vector (taking into account the I and Q digital words produced by the A/D converter) ; compares this modulus to a reference (selectable by a I^2C register).The AGC function outputs a pulse width modulated signal which is converted into a DC control voltage by an external low pass filter. The DC voltage controls the gain control function of the tuner. The error signal of this loop (depending on the actual power of the RF signal) can be known by the Reg Hex 12.

  Interesting characteristics :

  The AGC function of the STV0196 produces reliable results even in the following condtions :

  - low C/N conditions (Eb/No ≥ 2dB)
  - wide LNB frequency offset (≥ ± 5MHz)
  - unlocked timing loop

    (even when (f_{VCO} -2Fs) ≥ several MHz)

  Due to its high robustness, the AGC function can reliably used in the first steps of the carrier and data search software.

- ***Timing Recovery :***

  This function is based on a phase lock loop (PLL) in which the error detector and the loop filter are integrated in the STV0196 while the oscillator is external (VCO or VCXO). This PLL is a second order whose damping factor and natural frequency are programmable Reg Hex 0C. Additionnaly the PLL can be opened (Reg Hex 0C= 00) and the drive signal of the external oscillator can be arbitrarily forced with Reg Hex 0D.

  Interesting characteristics :

  The experiments have shown that : as long as the frequency difference between the oscillator and the targeted value 2Fs is lower than 500ppm, the timing loop can lock on to 2Fs, even in the following conditions :

  - Low C/N conditions (Eb/ No ≥ 2.5dB)
  - wide LNB frequency offset (≥ ±5MHz)

- ***Carrier Offset Evaluator :***

  The purpose of this function is to evaluate the position of the weighted center of the channel spectrum ; ideally this function is used to select in which direction the carrier search has to be done.

  Interesting characteristics :

  The carrier offset evaluator function does operate under the following conditions :

  - Low C/N conditions (Eb/No ≥ 2dB)
  - wide LNB frequency offset (up to ±Fs/2)
  - unlocked timing loop

  Remark : since this function is equivalent to an estimation of the location of the weighted center of the carrier, this function is sensitive to the SWR (stationnary wave ratio) which may exist in the coaxial cable.

  For this reason, this function is used to satistically reduce the search time (choosing a first search direction), however in case of unsucessful search the opposite direction will be also evaluated.

- ***Frequency Derotator :***

  This function is the last stage before FEC. The purpose of this function is to compensate the remaining frequency offsets (ex : due to the discrete aspect of the tuner frequency (62.5 or 125kHz steps). This function is equivalent to a PLL whose damping factor and natural frequency are programmable (Reg Hex 0E).

  Additionnaly the static frequency of this PLL can be forced (writing in Reg Hex 0F).

  Interesting characterisitcs :

  - reliably works only when timing loop is locked on to 2Fs
  - static frequency range ± f_S/16

III - MULTIRATE APPLICATION

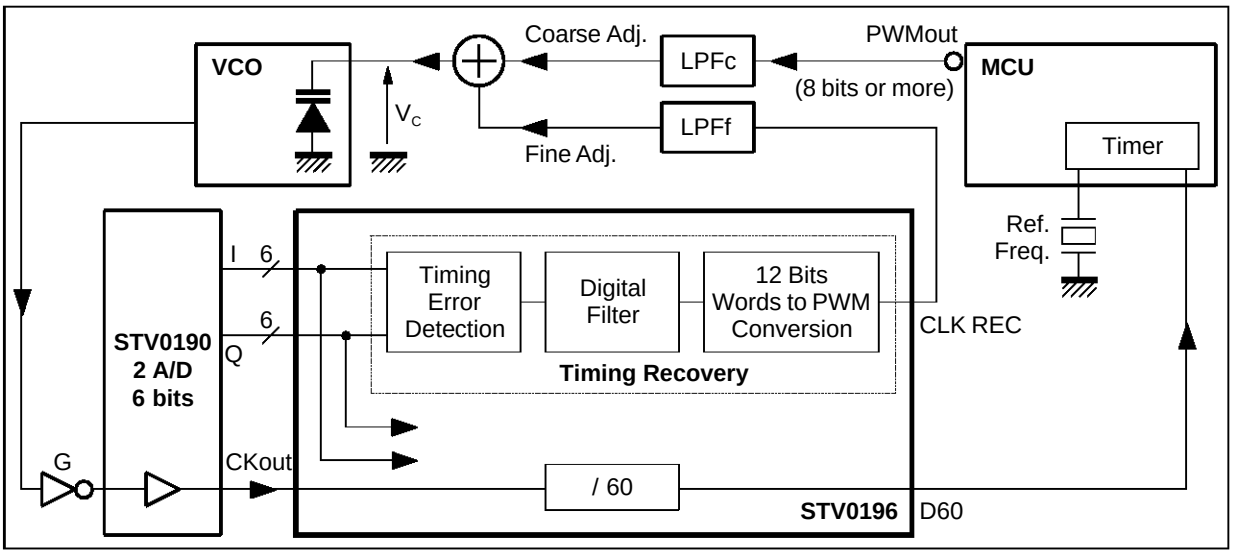
Preliminary : in this note "multirate " means application in which the symbol frequency Fs may take any value between 20 Mbauds and 30 Mbauds.

III.1 - Timing Loop : Hardware Description

III.1.1 - General Description

See block diagram in Figure 3.

Figure 3 : Multirate Application, Timing Loop Block Diagram



Taking into account that the timing oscillator runs at 2Fs, the operating frequency ranges from 40MHz to 60MHz. To cover such a range a solution implementing a Voltage Controlled Oscillator (VCO) is used.

As in any conventional VCO, a DC voltage V_C is used to control the capacitance of variable capacitance diodes (Varicaps : D1, D2). To both cover a wide range (40 to 60MHz) and to precisely control the timing frequency, the control signal Vc of the varicap diodes is the sum of two control signals : COARSE and FINE adjust.

An inverter gate G (1/6 of 74F04) is used to turn the VCO output waveform (pseudo-sinewave) into a conventional square waveform (remark : to save space, power consumption and to reduce the cost of this function, monogate circuit can be used (ex : TC74SH04F supplied by TOSHIBA/Japan or TEXAS Instruments)).

The clock signal is supplied to the A/D converter and bufferised into the CLOCK_OUT signal on which are synchronized with the two 6 bits output words. The CLOCK_OUT signal is the MASTER_CLK signal of the STV0196.

Whatever the operating mode and conditions of the STV0196, the D/60 pin of the STV0196 delivers a clock signal which frequency is 60 times lower than MASTER_CLK (VCO frequency).

In the complete system, the D/60 signal is supplied to the system control (MCU) to measure the VCO frequency and to compare it to a well known and stable reference frequency (derived from a crystal). With the results of the comparaison the MCU delivers a PWM (pulse width modulated) signal which is converted into a DC control : COARSE adjust. In doing so, a coarse adjustment loop is realized.

III - MULTIRATE APPLICATION (continued)

III.1.2 - Voltage Controlled Oscillator (VCO)

In the application, simple VCO structure can be used. Evaluation boards and typical application diagrams show standart COLPPITS oscillator (see Figure 4).

The oscillation frequency can be roughtly estimated as follows :

$$f_{VCO} = \frac{1}{2\pi\sqrt{L_2 \cdot C_{eq}}} \quad (1)$$

$$C_{eq} \approx C + \frac{C29 \cdot C26}{C29 + C26} \quad (2)$$

$$C = C_v + C_{parasitic} \quad (3)$$

$$C_V = \frac{C_{varicap} \cdot C30}{C_{varicap} + C30} ; C_{varicap} = f(V_C) \quad (4)$$

With reference to Figure 4 :

$$V_C = \frac{\frac{V_{COARSE}}{R25 + R26} + \frac{V_{FINE}}{R27}}{\frac{1}{R25 + R26} + \frac{1}{R27}} \quad (5)$$

- For a safe operation, the transistor Q1 must feature $f_T \geq$ 500MHz @ V_{CE} = 5V.
- In order to get the lowest jitter as possible in the VCO operation two main cares have to be taken :
  - to filter the transistor power supply voltage (R24,C27,C28)
  - to pay some attention in the PCB layout so that the control voltage V_C is not polluted (see PCB layout recommandations).

Remark : for components supply reason, the demoboards and diagrams show two varicaps (D1 and D2). Naturally it exists diodes references which would have produced similar results with only one component.

III.1.3 - Fine Timing Loop, and LPFf (Figure 3)

The fine timing loop is used to lock the VCO on the symbol rate of the received signal (actually f_{VCO} = 2Fs).

As described in the specification, the timing loop of the STV0196 (corresponding to the fine timing loop) can be modelised as a second order phase lock loop (PLL). The oscillator of this PLL is the external VCO.

Remark : in this structure the external low pass filter (LPFf) is not dominant in the characteristics of this PLL, this filter is mainly used to convert the signal generated at Pin CLK/REC into a (DC+Low frequencies) signal which is used to drive the VCO.

The closed loop frequency response of this PLL is : (assuming that the roll-off frequency of the external Low pass filter LPFf is high enough)

$$f(p) = \frac{N(p)}{p^2 + 2\xi\omega_n + \omega_n} \quad (6)$$

p : Laplace operator in the frequency field.

The natural frequency of this loop is :

$$f_n = \frac{\omega_n}{2\pi} = 19.2 \cdot 10^{-6} \cdot m\,Fs \cdot \sqrt{\Delta f \times 2^{beta\_tmg}} \quad (7)$$

m : decimal value of the AGC reference level (Reg Hex 11 b0 to b5)

beta_tmg : programmable coefficient (Reg Hex 0C b0 to b3)

Δf : half of the total relative fine timing range ; can be estimated as :

$$\Delta f = \frac{1}{2} \cdot \frac{1}{2Fs} \cdot \frac{V_{DD} \cdot \left(1 + \frac{R30}{R31}\right)}{1 + \frac{R27}{R25 + R26}} \cdot K_{VCO} \quad (8)$$

K_{VCO} = VCO slope

$\Delta f = 3.1 \times 10^{-3}$ in the typical application.

The damping factor of this loop is :

$$\xi = \frac{0.247 \cdot m \cdot \sqrt{\Delta f} \cdot 2^{alpha\_tmg}}{\sqrt{2^{beta\_tmg}}} \quad (9)$$

alpha_tmg :programmable coefficient (Reg Hex 0C b4 to b6)

Ex : In the typical application software, the register 06hex = 64hex and the reference level of the AGC is m = 20dec.
- the natural frequency ≈ 3.3kHz @ Fs = 20Mbauds
- the damping factor ≈ 4.4kHz @ Fs = 20Mbauds

LPFf Dimensions *(see Figure 5)*

There are 3 conditions to dimension the external low pass filter :
- The DC gain of the filter directly influences the pull range of the fine tuning loop (Δf), the DC gain is :

$$LPFf_{DCgain} = \frac{1 + \frac{R30}{R31}}{1 + \frac{R27}{R25 + R26}} \quad (10)$$

  The gain can be selected by R30, R31, R27.
- The roll-off frequency of the filter is a compromise between a too low frequency which would modify the characteristics of the PLL of the timing and a too high frequency which would not provide enough attenuation of the PWM signal generated at Pin CLKREC. Roll-off frequency ≈ 20kHz.

$$V_{OUT} = V_{IN} \cdot \frac{1}{(R36C36)p + 1} \cdot (1 + \frac{R30}{R31}) \cdot A(p) \quad (11)$$

A dominant pole is given by R36 and C36, f_{POLE} ≈ 19.4kHz

III - MULTIRATE APPLICATION (continued)

Figure 4 : VCO Detailed Schematic

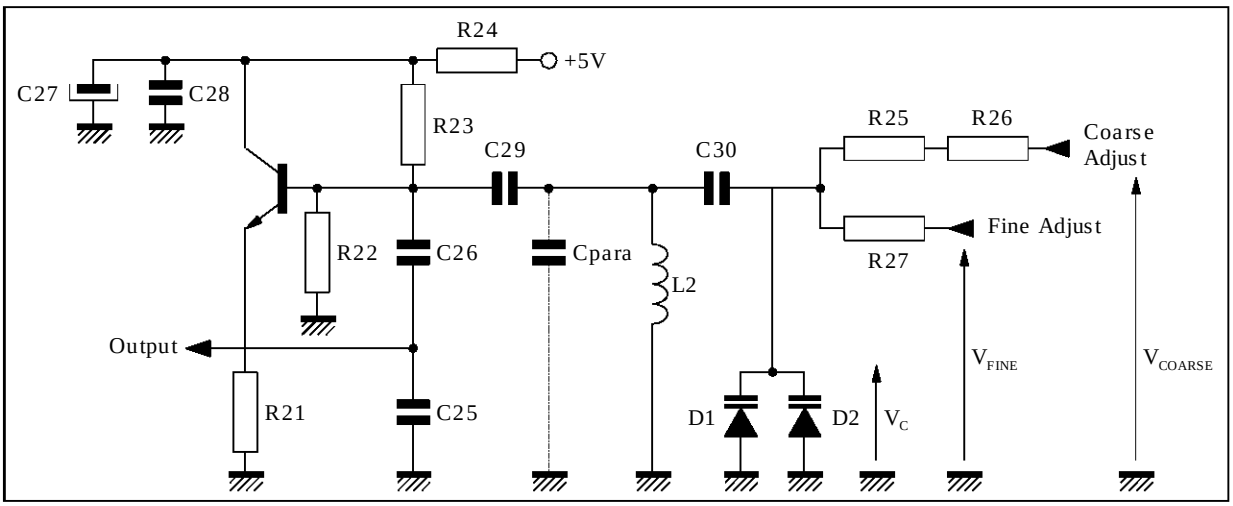
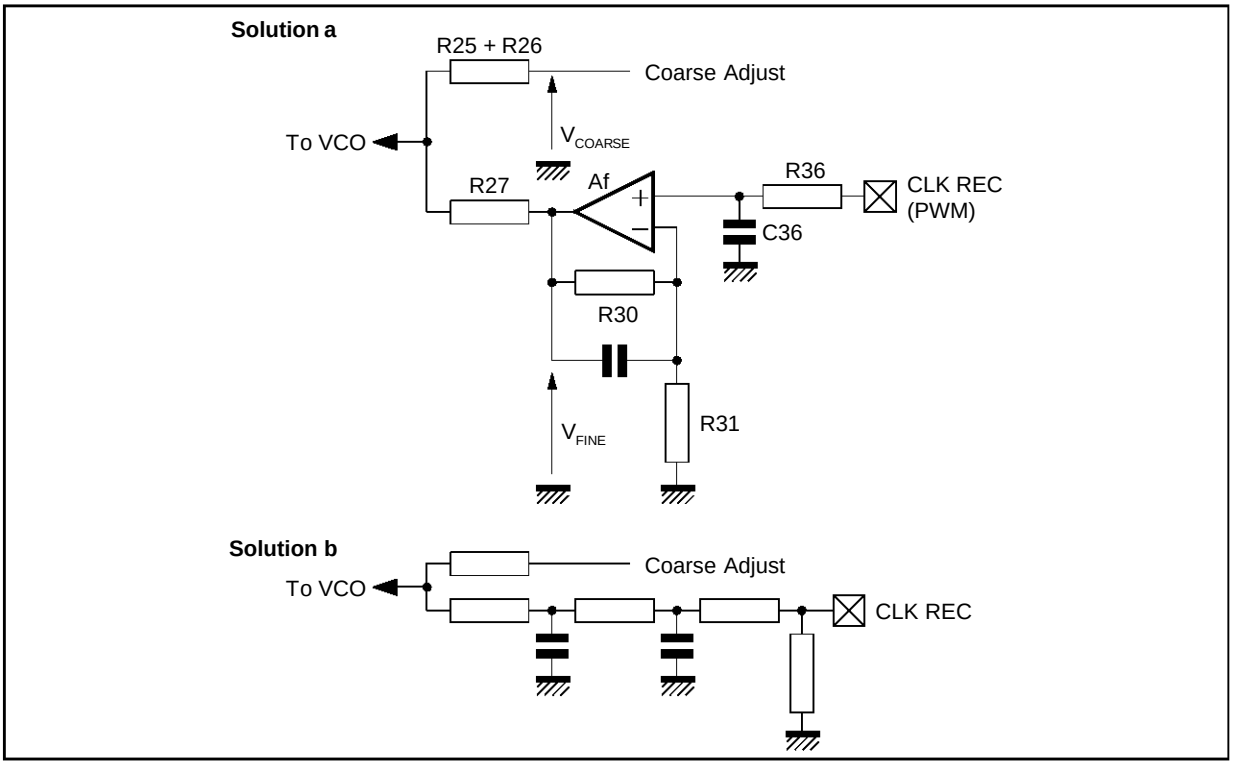


Figure 5 : Fine Timing Loop ; External Low Pass Filter LPFf



Note : Solutions a) and b) lead to similar results. On demoboards, the a) solution has been used to drive either a VCO (multirate application) or a VCXO (fixed rate application) with an unique PCB layout.

III - MULTIRATE APPLICATION (continued)

III.1.4 - Coarse Timing Loop and LPFc

The principle of the coarse adjust timing loop is : By software, to measure and compare the actual frequency of the VCO with a stable and precise frequency reference. Then the result of the comparaison is used to adjust the PWM signal which is turned into the coarse drive signal ; this is a closed loop. The VCO frequency (divided by 60) is measured at Pin D/60 (Figure 3).

In this loop the lowpass filter LPFc transforms the PWM signal into a quasi DC signal. To avoid some undesired effects, the two following cautions have to be taken in the application (Figure 6).

- It is recommanded to use an interface between the PWM output of the MCU and the low pass filter itself. This interface may either be a buffer or an inverting gate G1. With this care, the conversion of the PWM signal into a DC control can be done very close to the VCO and then reduces the disturbances due to the PCB layout (long connections, coupling with other signals...).
- Additionnaly, it is recommanded to supply this interfacing gate with a stable, noise free power supply. Reason : the DC level V_{DC} generated from a PWM signal is directly depends on the amplitude V_{AMP}. of the pulses of the PWM signal :

$$V_{DC} = \frac{t_{ON}}{T} \cdot V_{AMP} \qquad (12)$$

$\frac{t_{ON}}{T}$: duty cycle of the PWM signal.

If the interfacing gate is connected to a stable supply voltage, the V_{AMP} parameter is stable and consequently V_{DC}.

LPFc Dimensions

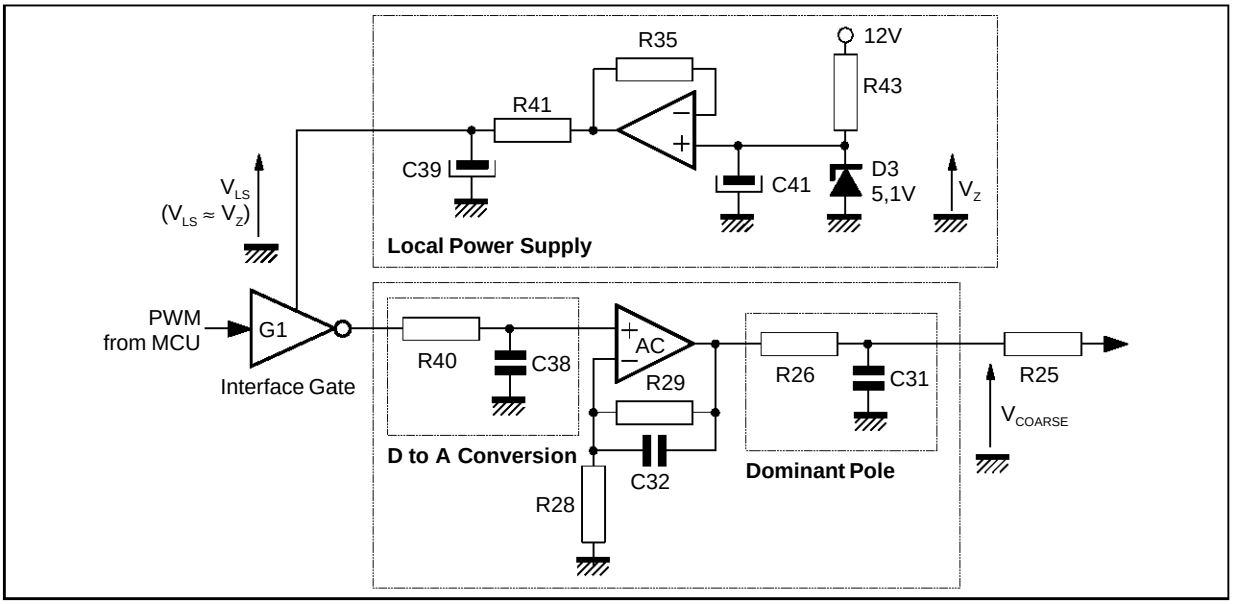
The main purpose of this filter is to attenuate, in the highest extent as possible, all the harmonics of the PWM signal. For cost and space saving reasons a high order and complex filter is not suggested. In the typical application, it has been prefered to decrease the roll-off frequency of a simple LPF filter to the lowest value as possible. However there is a limit :

- too low roll-off frequencies induce slow transient response of the filter. Consequently the VCO coarse adjustment software may be slowed down and may take too long.
  Typically the low pass filter LPFc contains a dominant pole ranging between 100 and 300Hz.
  Remark : Additionnaly, with a roll-off frequency of 100 to 300Hz. It is possible to make some adjustments of the PWM signal without generating fast phase changes in the VCO signal, and then without loosing the data. Adjustment of the PWM may be necessary to compensate for the slow thermal drift of the VCO.
  A voltage amplifier is used in the LPFc filter to generate the wide voltage swing required to bias the varicap diodes of the VCO.

$$V_{COARSE\ DC} \approx V_{LS\ DC} \cdot \frac{t_{ON}}{T} \cdot \left[1 + \frac{R29}{R28}\right] \qquad (13)$$

$V_{LS\ DC}$: local power supply votage
t_{ON} : duration of the high level at the output of gate G1
Remark : t_{ON} corresponds to (T-t_{ON} PWM) if G1 is inverting.
T : period of the PWM signal.

Figure 6 : Coarse Loop Filter, PWM Conversion



III - MULTIRATE APPLICATION (continued)

III.1.5 - Coarse Gain / Fine Gain (Figure 7)

As explained above the VCO is controlled by the sum of a fine and a coarse adjust signal.
How to select the gain of both loops ?

For clarity, the following explanations are based on the following example :

- Symbol rate Fs ranging from 20Mbauds to 30Mbauds
- The depth of the PWM signal is 8 bits (256 PWM steps)

In such an application the VCO operates from 40MHz to 60MHz (in practice from 36MHz to 66MHz to compensate for the dispersions of the VCO components). Out of this frequency range, 256 discrete frequency values are direcltly synthesised by the coarse adjust (PWM with 256 positions). The fine timing loop is used to synthesised any other frequency value existing between consecutive discrete values. Naturally to be able to synthesise any value, the total fine timing range ΔFf must be wider than the frequency spacing ΔS existing between two consecutive frequency values generated by the coarse loop. Again there is a compromise :

- Too wide fine timing ranges ΔFf ($>> \Delta S$) correspond to large values of Δf (relative range of the timing PLL, see relation 8). And then corresponds to less selective timing loops.
  In such a case, the Bit Error Rate (BER) is no optimized.
- Too narrow fine timing ranges ΔFf ($\approx \Delta S$) lead to critical coarse adjustment and requires a more frequent compensation of the thermal drifts of the VCO.

The experiments have shown that an optimum dimension of ΔFf is :

$$2\Delta S \leq \Delta Ff \leq 4\Delta S \qquad (14)$$

The total fine timimg range ΔFf corresponds to the complete swing of the CLK_REC signal. As seen previously the CLK_REC signal is low pass filtered and amplified to produce Vfine (Figure 5).

The VCO control voltage Vc is calculated as follows :

$$V_C = \frac{\frac{V_{COARSE}}{R25 + R26} + \frac{V_{FINE}}{R27}}{\frac{1}{R25 + R26} + \frac{1}{R27}} \qquad (15)$$

V_{COARSE} ranges from 0 till 28V

V_{FINE} ranges from 0 till 3.7V (3.3V multiplied by Af amplifier).

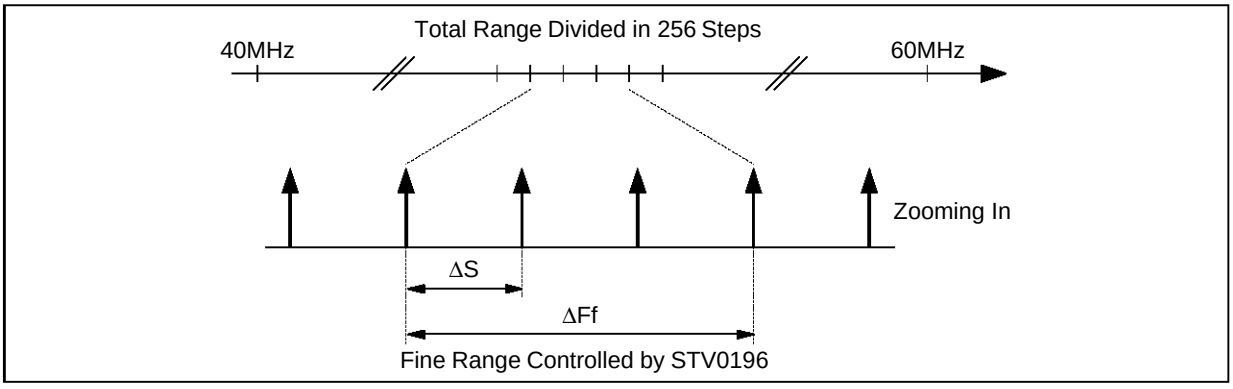
If $\Delta F = 3\Delta S$ (typical value), it means that V_{FINE} produces the same variation of Vc as 3 steps of the MCU PWM signal.

$$\Delta Ff = 3\Delta S$$

$$\frac{3}{256} \cdot \frac{V_{COARSE(Max.)}}{1 + \frac{R25 + R26}{R27}} = \frac{V_{FINE(Max.)}}{1 + \frac{R27}{R25 + R26}} \qquad (16)$$

Relation (16) is used to dimension the ratio between R27 and (R25+R26). In the typical application diagram R27 = 11 (R25+R26).

Figure 7 : Coarse Loop Gain versus Fine Loop Gain



III - MULTIRATE APPLICATION (continued)

III.2 - STV0196 Software Driver

This chapter is divided in 3 parts :
- Carrier and data search process
- Suggested processes while receiving a channel
- Recommanded register settings

III.2.1 - Carrier and Data Search

This software routine is called when changing RF channels or when changing symbol rates.
A simplified flow chart is given in Figure 9 and a more detailed one in Figure 10.

This routine drives the complete front-end : Tuner and LINK IC. The following functions are realised :
- Tuner setting to the wanted frequency.
- VCO frequency adjustment and locking to the incoming symbol rate (2Fs).
- Measure and compensation of the actual LNB frequency offset.
- Puncture rate and synchro search.

III.2.1.1 - General Strategy of this Software

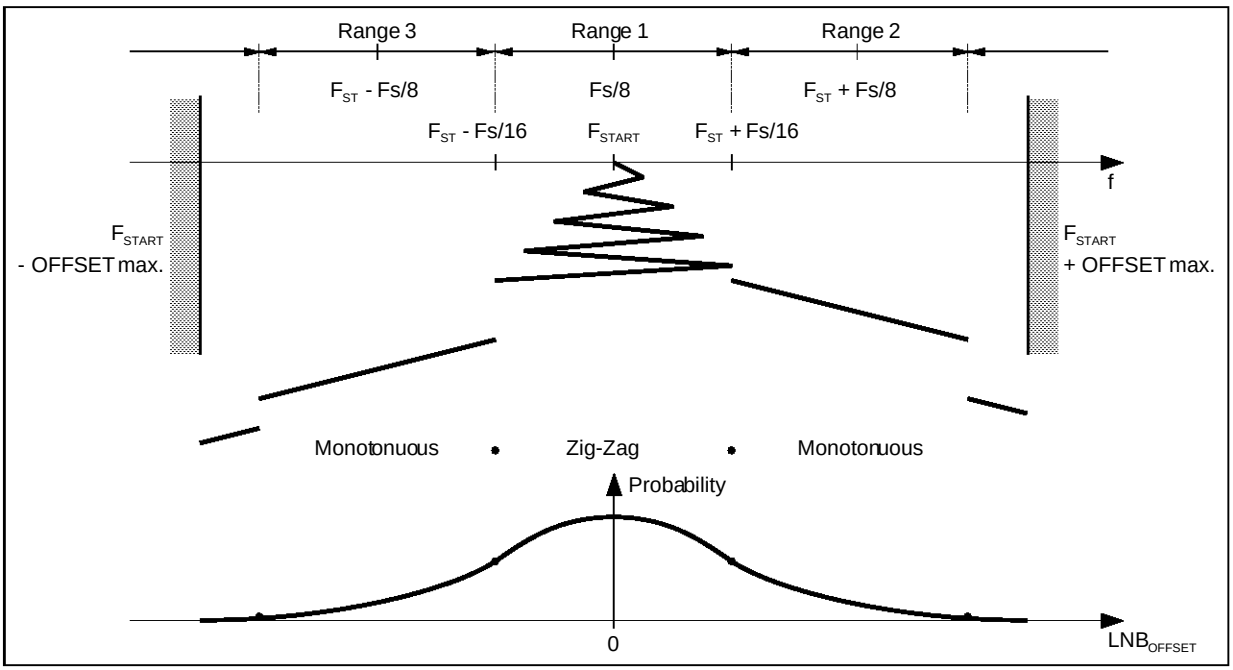
FOREWORD : The frequency band (typically ±5MHz) in which the carrier has to be searched is wider than the derotator range. Consequently, this frequency band is divided in sub-bands which width is equal to the derotator ranges (± Fs/16).

1. At first the tuner is set to the new frequency f_{CH}. The presence of signal is checked with the AGC function (remark : this function is reliable even in case of large LBN offset and before the timing loop is adjusted). Label A to B.
2. During the tuner settling time (rather long : few tens of ms to 100ms), the VCO is driven to the wanted value 2Fs (Fs : symbol rate). This operation is performed in two steps : VCO coarse timing (label X to C) and VCO fine timing (label C to D).
3. Before to close the timing loop, two conditions need to be simultanuously satisfied
   - the VCO frequency must be close enough to 2Fs (end of fine timing)
   - the signal carrying the clock signal must be present (AGC reporting a good level)
4. The timing phase locked loop (PLL) is closed (label E to F)
   The capture time of the timing loop is about 2ms, this delay is required before to check the lock. The lock is normally ensured if the two above conditions are respected. However a test is implemented ; a negative result would mean :
   - the required symbol rate does not match with the actual one carried by the channel (when RANGE = 1).
   - the timing loop has lost the lock when the tuner frequency has been offset (RANGE > 1).
5. Once the timing loop is correctly locked on the incoming symbol rate, the results of the derotator function are reliable, and the carrier search algorithm can be carried out.
   Basically the carrier search algorithm aims to find the carrier inside a frequency space comprised between (f_{CH}-OFFSET_MAX) and (fCH+OFFSET_MAX);
   generally OFFSET_MAX ≤ 5MHz.
   This frequency range is wider than the derotator range : ± Fs/16 (ex : ± 1.7MHz for Fs = 27Mbauds). Consequently to scan the required band, the search algorithm needs to bring offset to the tuner frequency (Figure 8).
   As satistically the actual frequency offset is low or null, the search start with no tuner offset :
   $$f_{START} = f_{CHANNEL} - f_{LO}$$
   f_{LO} : LNB local oscillator frequency
   Remark : at the first operation of the search algorithm, the OFFSET value may be memorized in a non volatile memory. With this care, in the future searches f_{START} can be given a first correction.
   The carrier search terminates when either a carrier is found (Label I) or when the current offset (|OFFSET + Derotator_frequency|) exceeds OFFSET_MAX.
6. Carrier search procedure :
   A. In the first range (RANGE = 1), the tuner is tuned to f_{START}. The first range is scanned in zig-zag starting from a frequency offset equal to zero. The zig-zag scanning is satistically expected to give the shortest search time since the LNB offset is satisitically low or null.
   Remark : the STV0196 features a "carrier offset evaluator". In theory, this indicator could be used to select which direction to check first (positive or negative offsets). However it appeared that the value reported by this indicator is dependant on the stationnary wave ratio (SWR) which exists in the coaxial cable ; it would sometimes leads to wrong decisions when the SWR is important.
   B. The center of the following ranges are spaced with a multiple of Fs/8 (RANGE > 1). Those following ranges are scanned in a monotonuous way : starting from the lowest offset (highest probability) :
   - for positive offsets : from f_{CH}-Fs/16 till f_{CH}+Fs/16
   - for negative offsets : from f_{CH}+Fs/16 till f_{CH}-Fs/16

   The sign of the first offset to give to the tuner is selected according to the "carrier offset evaluator"function ; in this way satistically the search time is minimized. Labels M, M1, M2.

III - MULTIRATE APPLICATION (continued)

Figure 8 : Carrier Search Strategy ; Example with Positive OFFSET in RANGE 2



7. Once the carrier is found (Reg Hex08 bit7=1), the VITERBI decoder automatically performs the following functions (if set in automatic mode : Reg Hex 06 bit 6 and bit 7 = 1) :
   - Puncture rate search
   - Puncture rate phase search
   - Recovery of the potential 90° phase ambiguity of the QPSK signal.

   The 180° phase ambiguity (not detectable by the VITERBI decoder) is monitored and corrected by the synchro byte decoder.

   All these searches require some time θ, for this reason a waiting time sequence is needed before to check wether the synchro is found (Reg Hex 08 bit 3). Label I to L.

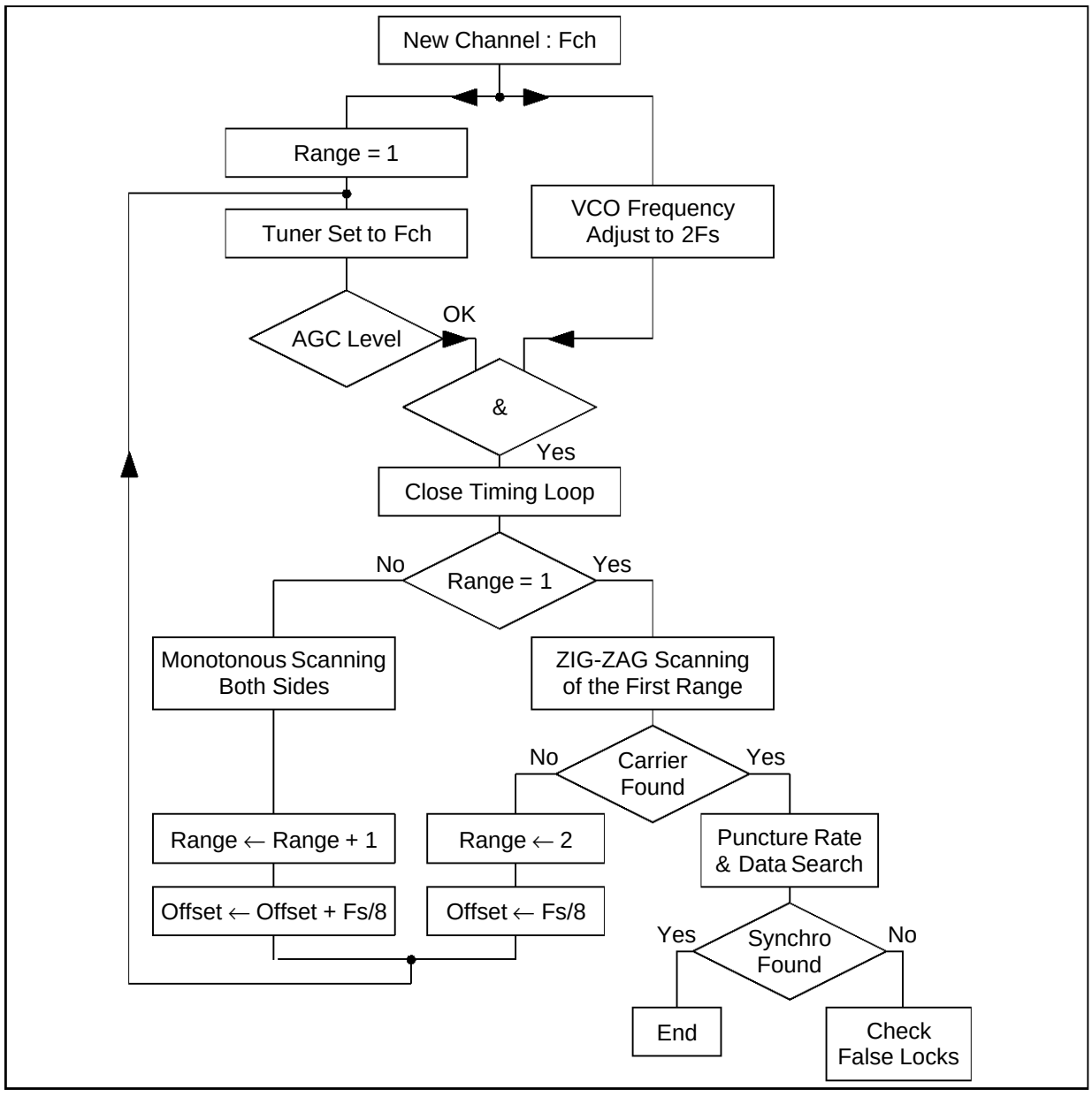
   Remark : the duration θ of the search widely depends on the number of allowed puncture rates during the search (this number may be reduced to one when the puncture rate (inner code) is provided by the NITs (Network Information Tables).

   The duration θ also depends on the sensitivity given to the synchro search (Reg Hex 06 : SN, TO, H bits). Finally the duration θ depends on the symbol rate Fs.

   The annexe 1 (on last page) gives how to estimate the maximum duration θ to get the synchro (after the carreir is found). Typically this duration is about 30ms when all puncture rates have to be checked.

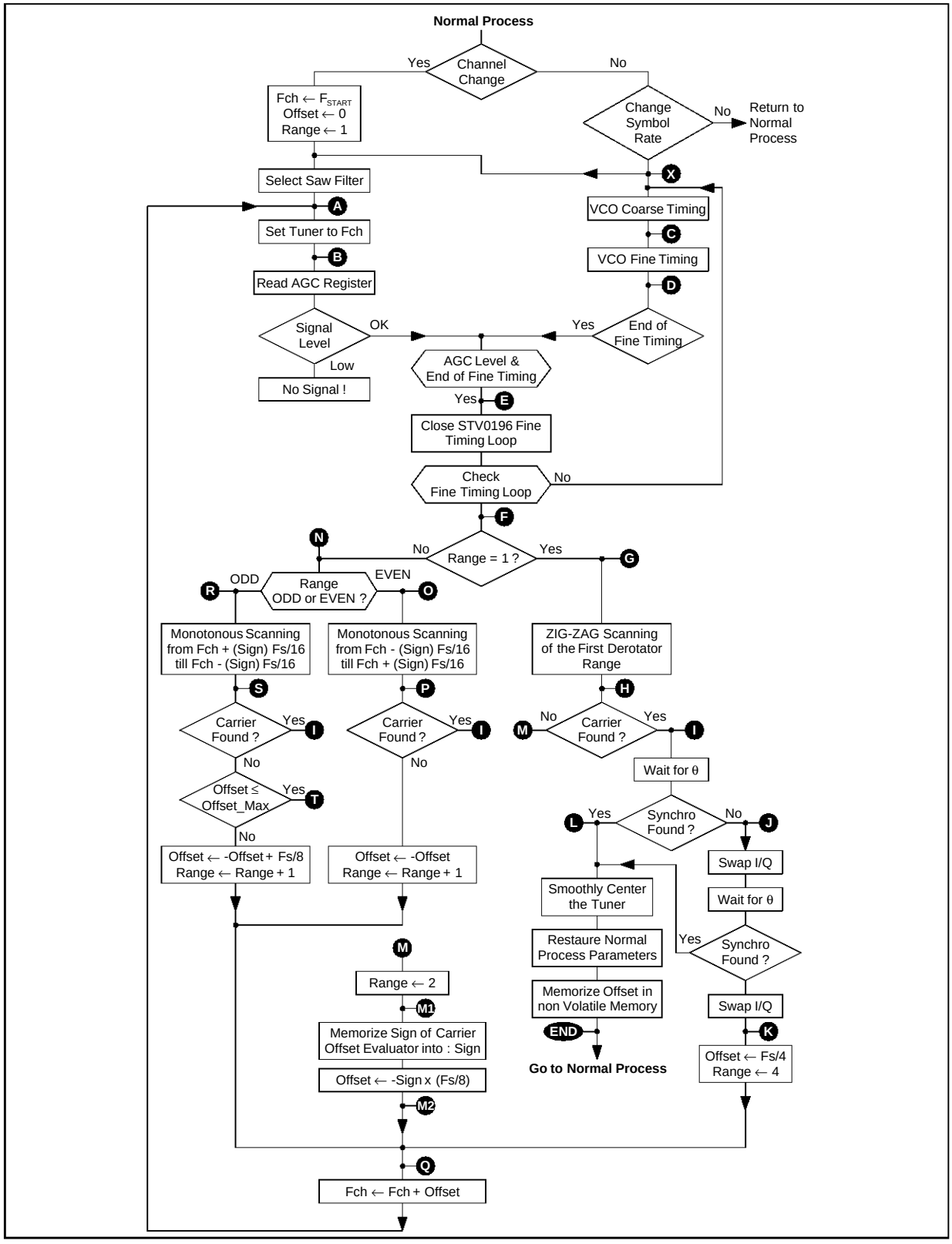
III - MULTIRATE APPLICATION (continued)

Figure 9 : Carrier and Data Search Algorithm (simplified)



III - MULTIRATE APPLICATION (continued)

Figure 10 : Carrier and Data Search Algorithm (detailed)



AN888-10.EPS

III - MULTIRATE APPLICATION (continued)

8. Once the synchro is found (Label L to END).
   The carrier and data search algorithm is almost completed ; the remaining steps are implemented to optimize the normal process operation :
   A. Smoothly centering the tuner frequency
      In this process the tuner frequency is adjusted so that the channel spectrum is well centered on the SAW filter of the tuner (reducing imbalance between the side bands). This operation is easily done by implementing a loop which adjusts the tuner frequency in such a way that the derotator frequency cancels (or nearly null : as the tuner frequency takes discrete values generally spaced by 62.5 or 125kHz).
      Practically the actual offset of the channel is :

      ACTUAL_OFFSET= OFFSET + delta

      OFFSET : is the offset given to the tuner frequency during the carrier search algorithm.
      delta : is the remaining offset part which is compensated by the derotator.
      delta = derotator frequency = N x (tuner steps)

      $$N = \frac{DEROTATOR\_FREQ}{128} \cdot \frac{Fs}{16} \cdot \frac{1}{tuner\_step}$$

      DEROTATOR_FREQ : Decimal value of Reg Hex 0F.
      The required compensation is N tuner steps. This compensation is done step by step in order not to loose the timing and the data.
   B. Restaure normal process parameters
      The carrier and data search algotithm has required some specific setting of the STV0196 registers. Those settings are not allways optimized for the normal process (channel demodulation). Chapter III.2.3 gives the recommanded register maps.
   C. In order to minimize the acquisition time of the future searches, the measured ACTUAL _OFFSET (OFFSET + delta) may be memorized in a non volatile memory.
      So that the starting theoritical frequency of the tuner f_{START} ($f_{CHANNEL}$ - f_{LO}) may be corrected before to launch the carrier and data search algorithm.
9. False locks (Label J to K)
   It may happens that no synchro is found in spite of the carrier found flag. This effect may have two different explanations :
   A. The RF signal is modulated as follows :
      RF(t) = I(t)sin(wt) + Q(t)cos(wt)
      while the general case is
      RF(t) = I(t)cos(wt) + Q(t)sin(wt).
      In such a case, a QPSK signal is recognised (carrier found) but no synchro can be found. To clarify this ambiguity the I and Q input are swapped (Reg Hex 00 bit 0). Naturally a new waiting period θ is needed before to check again the synchro flag.
      If no synchro is found, the second explanation has to be tested, before that I and Q inputs are swapped again to recover the original configuration.
   B. False lock of the QPSK demodulator :
      This may happen when the offset is about $\pm$ Fs/4, in such a case there is aliasing effect, and the QPSK demodulator locks during the first range (Zig-Zag).
      In this case, the tuner frequency is directly offset by + Fs/4. And RANGE is set to 4 to make sure that both + Fs/4 and - Fs/4 will be tried (to select the sign of this offset according to the carrier offset evaluator register would not be easy : potential spectral symetry produced by the aliasing effect combined with potential effect of the SWR).

III - MULTIRATE APPLICATION (continued)

III.2.1.2 - More Details about the VCO Frequency Adjustment Routines

As mentioned in Section III.1.1, the hardware system provides three tools :
- D/60 signal : feed back signal used to measure the VCO frequency
- a PWM signal : the coarse control of the VCO frequency
- a frequency reference

Remark about the frequency reference :
In practice, the commonly used reference is the horizontal synchro Hsync (or a multiple of it) produced by the video encoder (Hsync = 64µs (PAL) ; Hsync = 63.492µs (NTSC)). This reference itself depends on the 27MHz clock which typically has a dispersion lower than ±100 ppm (before to lock on the broadcasted reference : PCR).

Using a timer function of the MCU, the measurement of the VCO frequency is done as follows :

$$T_{VCO} \cdot 60 \cdot Count = N \cdot T_{REF}$$

T_{REF} : Hsync
T_{VCO} : VCO period
Count : Number of D/60 events counted by the timer.

VC0 Coarse Timing (Flow chart in Figure 11)

The purpose of the coarse adjust is to select the optimum PWM value. This routine is based on a binary search. The PWM is set in the middle of the range, and the corresponding VCO frequency (given by COUNT) is compared to the targeted value COARSE_COUNT. In the following loop, the range is halved, the limits are defined according to the results of the previous turn ; and again the PWM is set in the middle.

Breakdown of the chart :

A. At first the targeted counted value COARSE_COUNT is calculated according to the required symbol rate (given by the NITs). More precisely COARSE_ COUNT is the closest integer value to the following result :

$$COARSE\_COUNT = \frac{TIMER1}{60} \cdot 2Fs$$

TIMER 1 = N (Hsync)
N is the result of a compromise : a high N value induces a high accuracy but also a long counting time. In case of coarse adjust, the required precision does not need to very high because the number of steps is rather small : 256.

Let us optimize the N value. The dispersion of COARSE_COUNT is ±1.5 (rounding + counting error). This dispersion needs to be lower than half of a step to select a PWM without making error :

$$\frac{\Delta_{COARSE\_COUNT}}{COARSE\_COUNT} \leq 0.5 \left(\frac{1}{256}\right)$$

$| \Delta_{COARSE\_COUNT} | = 1.5$
$\Rightarrow COARSE\_COUNT \geq 768$
$\Rightarrow$ TIMER 1 ≥ 1.15ms @ Fs = 20 MBauds
$\Rightarrow N \geq 18$
Typically, to give some margin N is choosen in between in the range of 30 to 40. Label A to B.

B. Initialization :
During the coarse adjust the fine timing loop of the ST0196 is desabled (RegHex0C = 00). Additionnaly the fine timing loop is centered in order not to bias the coarse adjust. Label B to C.

C. The binary search :
This part countains all the others steps of the chart.
Remark : The counting does not start just after the PWM positionning, a delay corresponding to 7 time constants of the LPFc filter is neeed. With this care, the transient response of the filter does not disturb the measure.
The binary search is completed when either :
- the COUNT has one or less unit dispersion compared to COARSE_COUNT
- or when the remaining PWM range is less than 2 steps. Inside this remaining range a last search is done to define which PWM position generates the lowest dispersion compared to COARSE_COUNT.

D. Duration of the VCO coarse adjust :
With N = 40, the longest duration T of the coarse adjust is :

$$T = n \cdot (7\tau + TIMER\ 1)$$

with n = 7 and $\tau = R26 \cdot C31 = 330\mu s$
$\Rightarrow T = 34ms$

VCO Fine Timing (Flow chart in Figure 12)

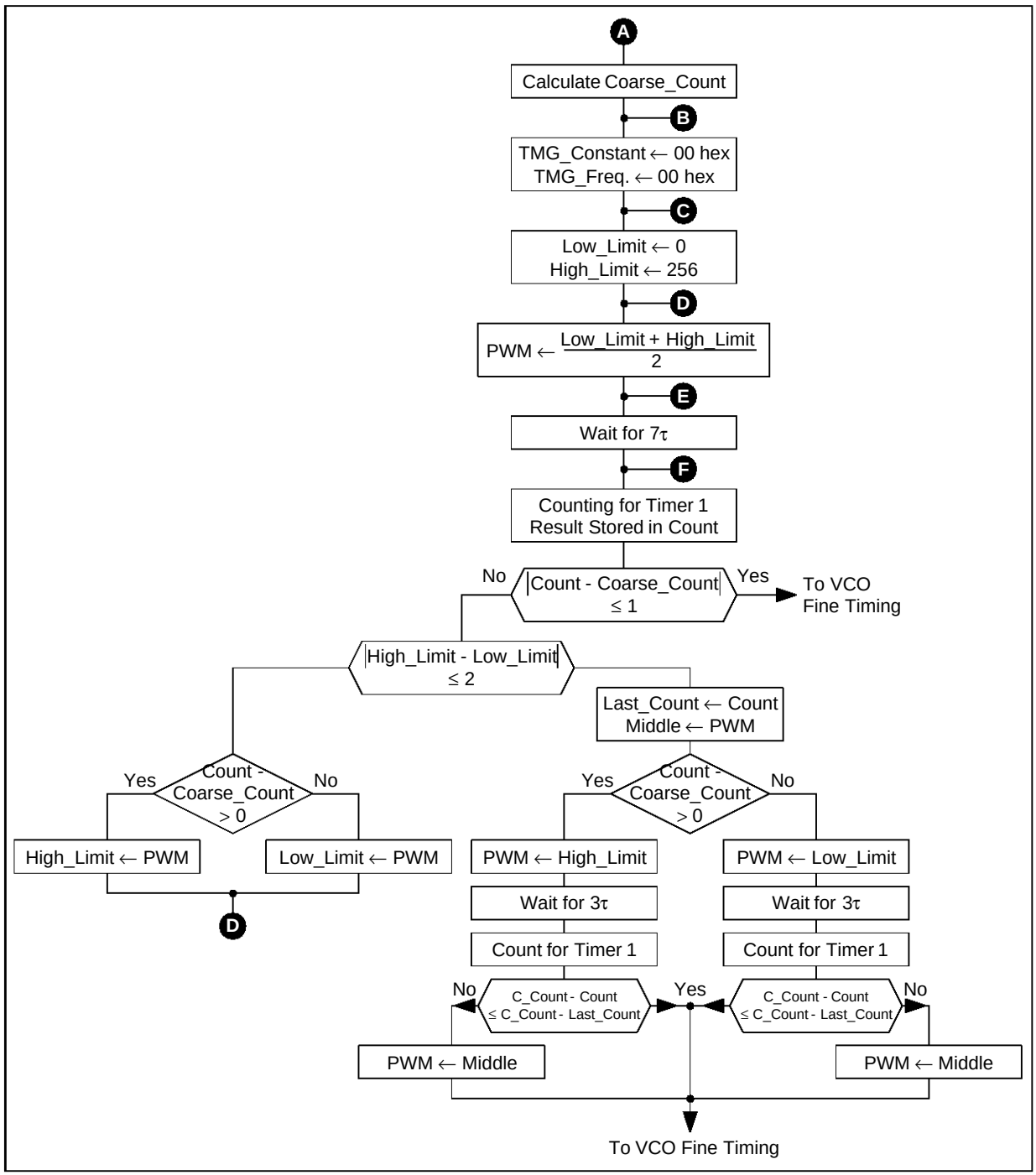
The purpose of this routine is to define the optimum DC biasing of the fine timimg loop (RegHex0D), so that the VCO frequency is as follows :

$$2Fs - 500ppm \leq F_{VCO} \leq 2Fs + 500ppm$$

When this condition is satisfied, the lock is ensured whatever the operating C/N conditions and whatever the initial LNB frequency offset.

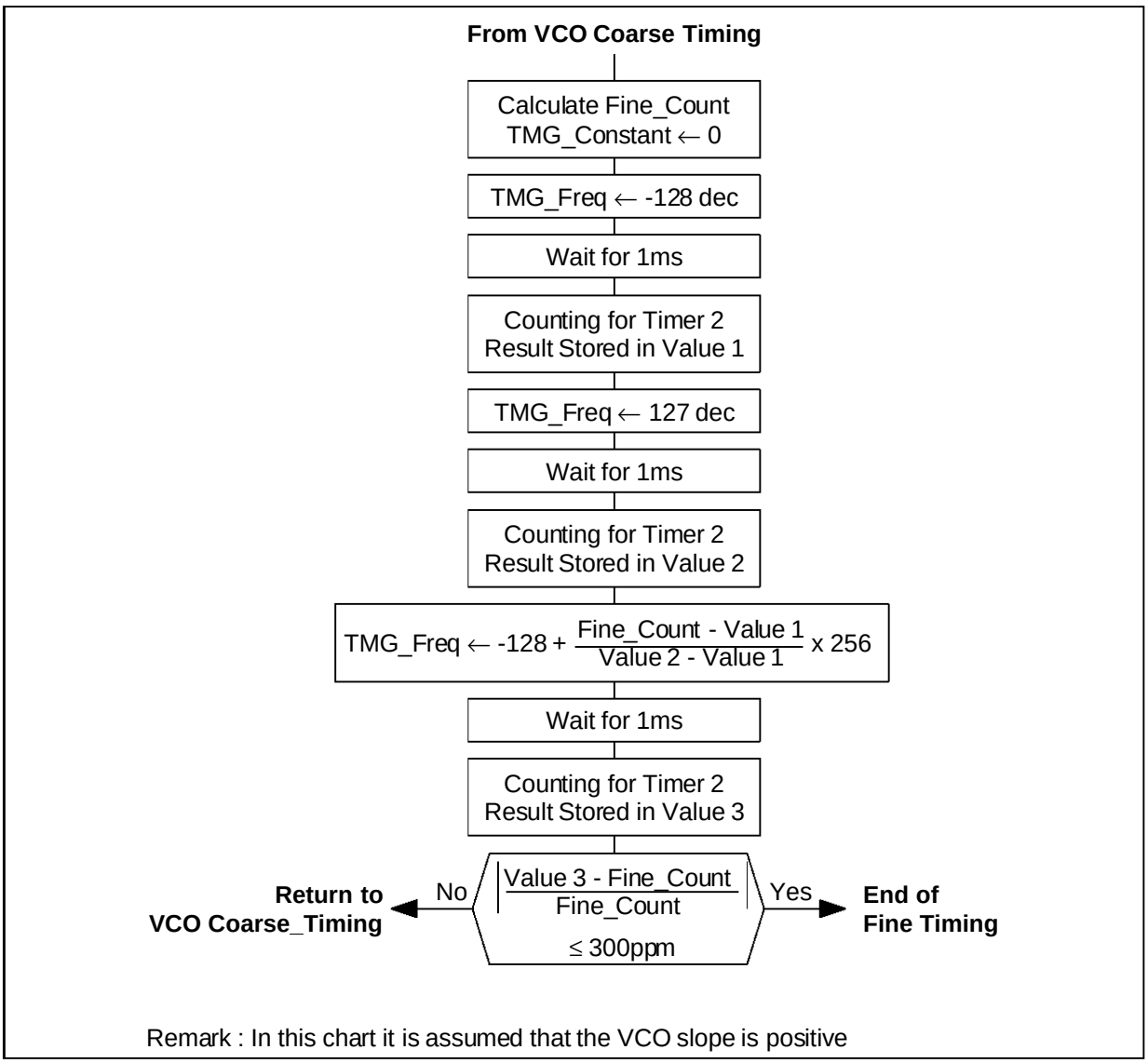
III - MULTIRATE APPLICATION (continued)

Figure 11 : VCO Coarse Timing Algorithm



III - MULTIRATE APPLICATION (continued)

Figure 12 : VCO Fine Timing Algorithm



Remark : In this chart it is assumed that the VCO slope is positive

Principle of the fine timing (see Figure 13) :
For small variations the VCO slope is very linear ; consequently the optimum fine timing position can be decided by an interpolating calculation. The two values required for this interpolation are the extremes of the fine timing loop.

In the fine timing, a higher accuracy is needed to ensure a dispersion lower than ±500ppm :

$$T_{VCO} \cdot 60 \cdot FINE\_COUNT = TIMER\,2 = Nf \cdot Hsync$$

$$\frac{\Delta T_{VCO}}{T_{VCO}} = \frac{\Delta TIMER2}{TIMER2} + \frac{\Delta FINE\_COUNT}{FINE\_COUNT} \leq 500ppm$$

$\frac{\Delta TIMER2}{TIMER2} = 100ppm$ (max. dispersion of the 27MHz clock before the lock)

$\Delta FINE\_COUNT = 1.5$

$\Rightarrow FINE\_COUNT \geq 3750$

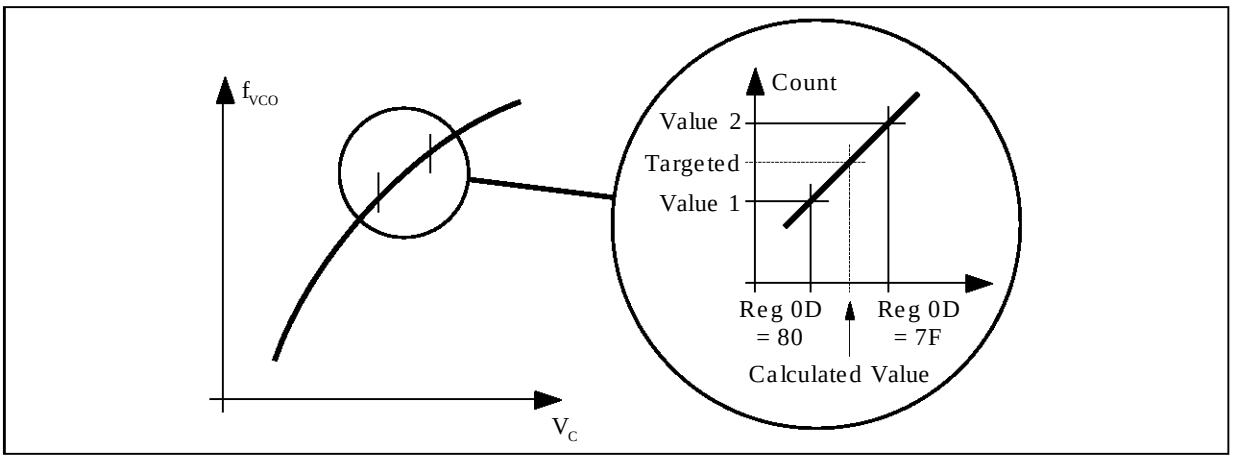
To give some margin FINE_COUNT is choosen about 10 000 ; consequently TIMER2 = 15ms $\Rightarrow$ Nf ≥ 234 (@ Fs = 20 Mbauds). Typically a Nf is choosen in the 200 to 400 range.

The routine itself is very simple : to measure the VCO frequency for both extremes of the STV0196 fine timing range and to make the interpolation.

Remark : A waiting time is required between the positionning of Reg Hex 0D and the counting procedure. Reason : to minimize the effect of the transient response of the LPFf filter. Delay is about 100µs to 1ms.

III - MULTIRATE APPLICATION (continued)

Figure 13 : VCO Fine Timing Strategy



III.2.1.3 - More Details about the Zig-zag and the Monotonuous Scanning

The zig-zag scanning and the monotonuous scanning procedure use the same basic sub-routine : The derotator frequency is forced by writting in Reg Hex 0F and after a certain delay (about 1ms) the carrier flag (Reg Hex 08 bit7) is checked. When this flag is high the carrier is considered as found. The delay is required to take into account the capture time of the derotator.

In order to minimize the scanning time, the derotator bandwidth is increased so that less steps are necessary to scan the complete derotator range.

The capture range and the frequency step are selected so that consecutive steps slightly overlap.

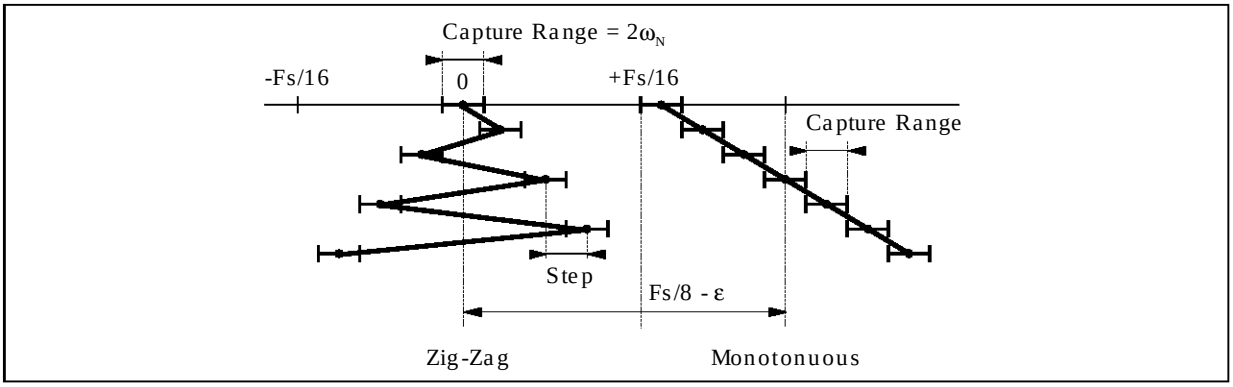
For instance with Fs = 20 Mbauds and Reg hex 0E = a3hex, ω_N = 44kHz, the step size can be $2\omega_N$ = 88kHz ; the complete range (width : Fs/8) can be scanned in 28 steps. To ensure a good overlap, typically about 40 steps are implemented. The scanning time is about 40ms.

Inside the monotonuous scanning procedures an additionnal test is implemented to make sure that the current offset does not exceed OFFSET_MAX :

$$\left|\text{OFFSET} + \frac{\text{DEROTATOR\_FREQ}}{128} \cdot \frac{\text{Fs}}{16}\right| \leq \text{OFFSET\_MAX}$$

DEROTATOR_FREQ : decimal value of register 0Fhex (signed value).

Figure 14 : Zig-Zag and Monotonuous Scanning of the Derotator Ranges



III - MULTIRATE APPLICATION (continued)

III.2.2 - Suggested Processes While Receiving a Channnel

Following informations are relevant to software processes which permanently monitor the STV0196 operation while demodulating a channel :

- Compensation of the LNB frequency slow drifts
- Compensation of the VCO frequency drifts
- Carrier to noise (C/N) estimation

III.2.2.1 - Compensation of the LNB Frequency Slow Drifts (Figure 15)

The outdoors unit (LNB) is subject to temperature changes which also happen during channel reception. It induces slow drifts of the LNB frequency. To compensate for those drifts, a routine regularly and permanently monitors the derotator frequency. When the derotator frequency becomes higher than 2 tuners steps (typically), the tuner frequency is adjusted in such a way to cancel the derotating frequency. The only care to be taken : before to change the tuner frequency, it is recommanded to widen the derotator bandwidth, with this care the derotator better tracks the frequency ramp produced by the tuner.

III.2.2.2 - Compensation of the VCO Frequency Drifts (Figure 16)

A VCO is subject to thermal drift (typically more than 10 000 ppm over a 25°C to 70°C temperature range). This drift is higher than the tracking range offered by the fine timing control of the STV0196 (about 8 000 ppm or equivalent to 3 coarse PWM steps).

The actual drift of the VCO versus the wanted frequency (2Fs) is measured by Reg hex0D.

On a regular basis (every 1s to 10s) this register is read. When the read value corresponds to a drift higher than ±0.8 step (typically), the coarse loop is given a one PWM step correction.

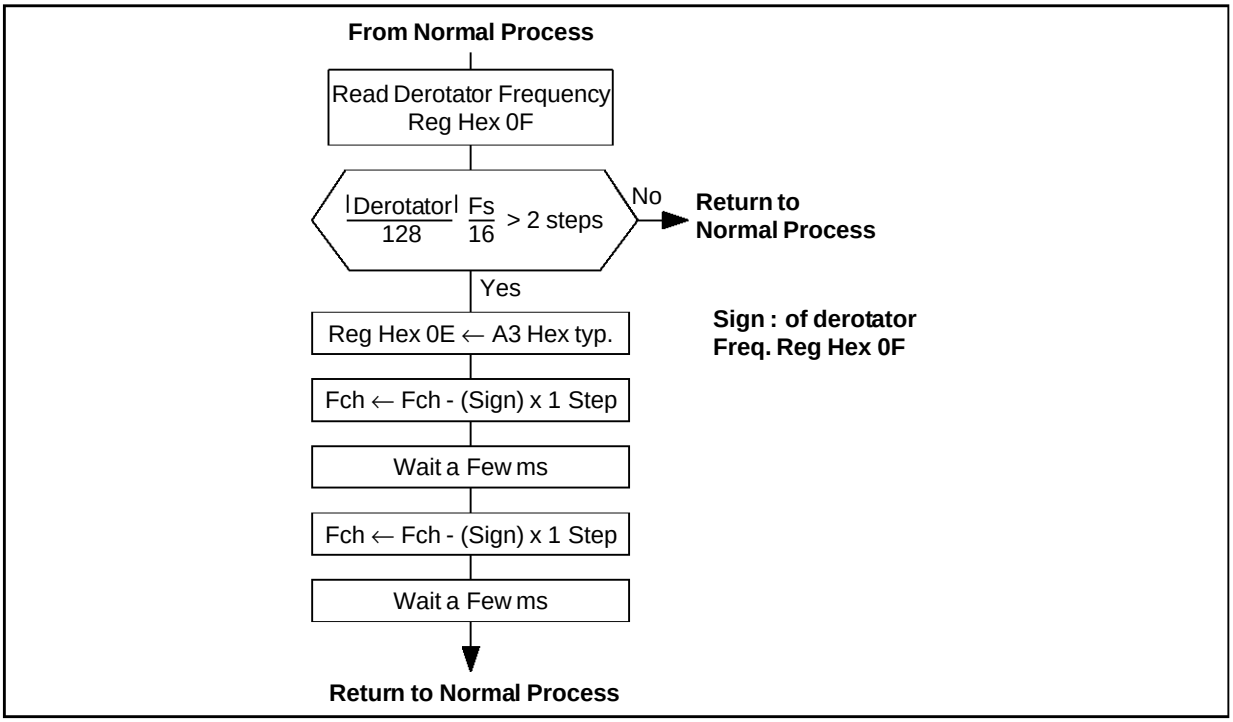
In order not to loose the lock, it is required to widen the timing loop bandwidth during this correction. Before to return to the normal process, the status (Reg hex08) is checked to make sure that the data have not been lost. This check is done after a delay Th which is needed to take into account the hysteresis provided by the H[1..0] bits of Reg hex06.

III.2.2.3 - Carrier to Noise Estimation

This function only exists in STV0196B and STV0196C versions.

The purpose of this function is to estimate the actual carrier to noise ratio (C/N) at the input of the STV0196B. This function is particularly interesting to optimize the dish positionning. The C/N estimation routine can be run during the carrier and data search and during the demodulation. For more details about this function, please refer to the ANNEXE 1 of the STV0196B specification.

Figure 15 : LNB Frequency Offset, Monitoring Routine (every 1 to 10s)



III - MULTIRATE APPLICATION (continued)

Figure 16 : VCO Frequency Drifts, Monitoring Routine (every 1 to 10s)

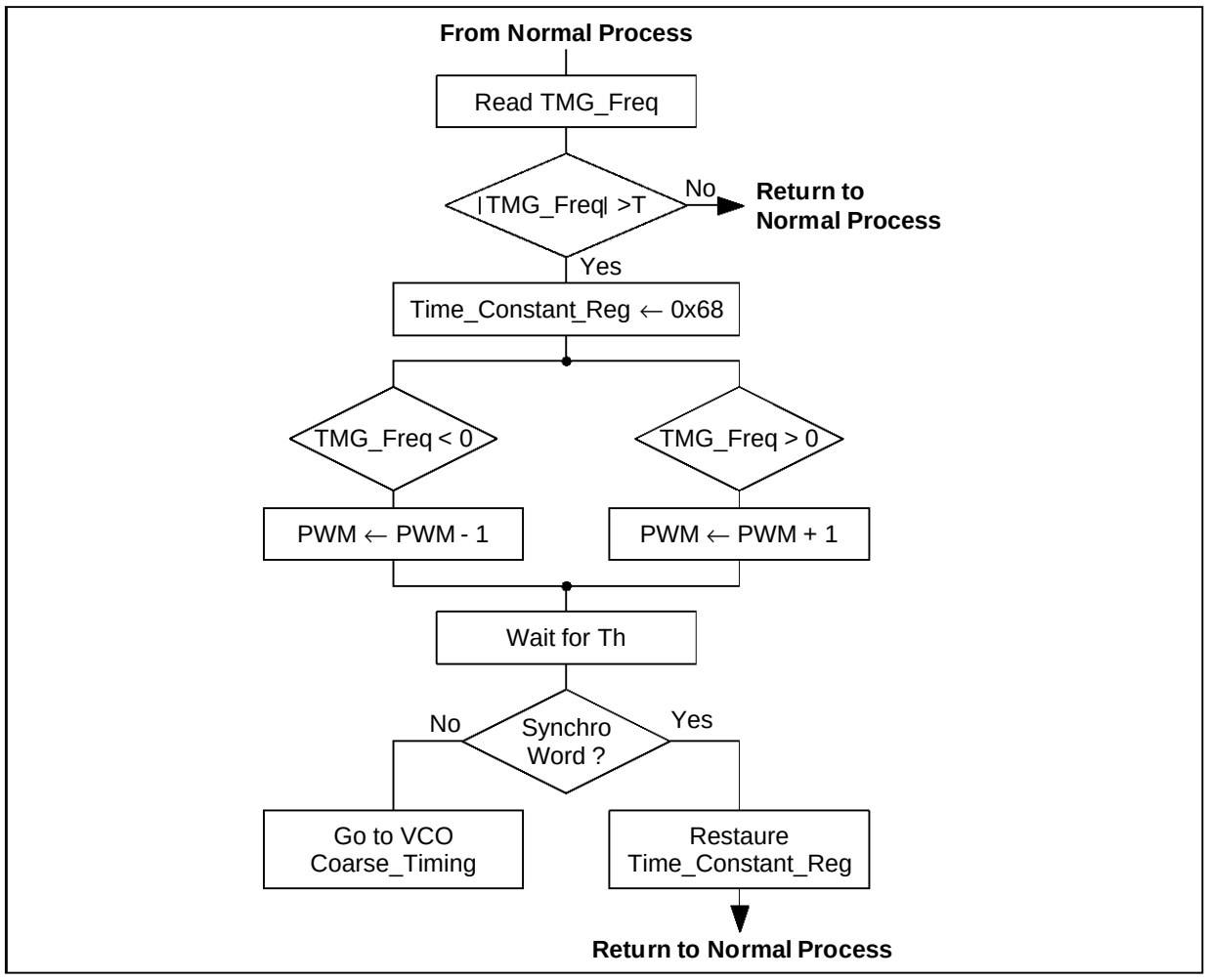
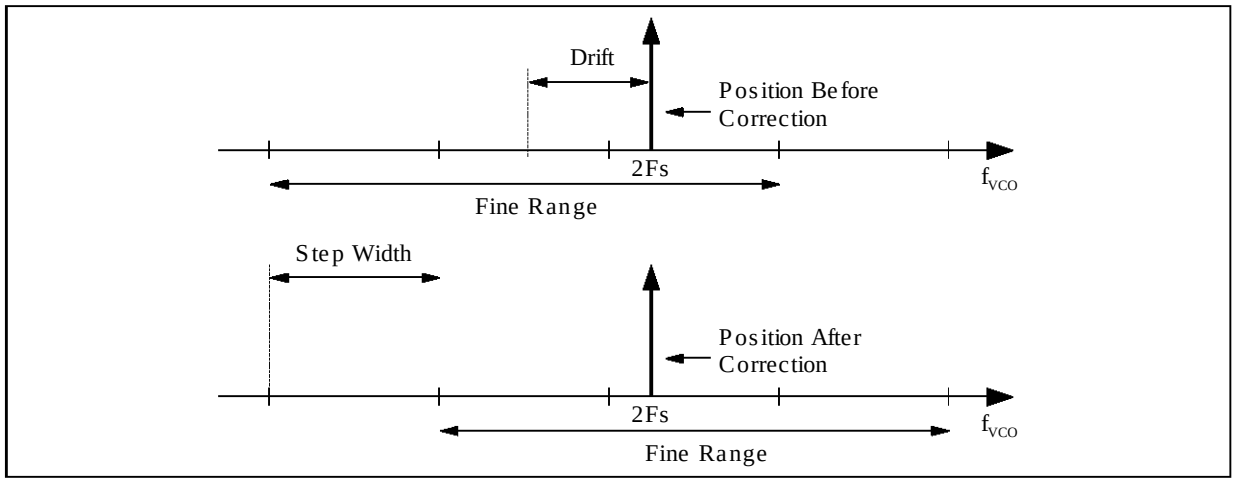


Figure 17 : VCO Frequency Drifts, Monitoring Routine



III - MULTIRATE APPLICATION (continued)

III.2.3 - Recommanded Register Settings

The following table gives the typical setting of the register versus different operating conditions :

- SEARCH : data and carrier search
- NORMAL : during demodulation and under normal C/N conditions
- LOW C/N : during demodulation and under low C/N conditions
- C/N Estimation : during the C/N estimation

The following table does not mention the read only registers. Conventions of the table :

- V : variable value.
- Fixed : value is frozen after the search routine.
- R : read only.
- R/W : either used in read or write mode.

Register Name	Hex add.	Search	Normal	Low C/N	C/N Estim.	Comments
Input Configuration	0	4 or 5	4	4	4	Note 1
Viterbi Threshold PR : 1/2	1	1E	1E	1E	1E	Note 2
PR : 2/3	2	14	14	14	14	Note 2
PR : 3/4	3	0F	0F	0F	0F	Note 2
PR : 5/6	4	9	9	9	9	Note 2
PR : 7/8	5	5	5	5	5	Note 2
Vsearch	6	2D	6F	6F	V	Note 3
Puncture Rate Enable	9	1F	Fixed	Fixed	Fixed	Note 4
Time Constant	0C	64	64/68	64	64	Note 5
Timing Frequency	0D	R/W	R	R	R	Note 6
Carrier Loop Parameter	0E	A3	A3	91	91	Note 7
Derotator Frequency	0F	R/W	R	R	R	Note 8
AGC Reference	11	14	14	14	V	Note 9
AGC Coefficient	13	1	1	1	1	

Notes :
1. In the search the register hex 00 is loaded with 05 hex when checking potential I/Q swapping.
2. The Viterbi threshold are determined experimentaly.
3. During the search, typically the Viterbi decoder is used in automatic mode. In normal and low C/N conditions the puncture rate is frozen, and the synchro counter is given a higher hysteresis (H[1..0] = 11). During the C/N estimation, the SN bits are changed according to the C/N estimation software routine (please refer to the ANNEXE 1 of the STV0196B specification).
4. During the search, typically all the puncture rates are allowed (however it may happen that the puncture rate is known by means of the NITs, in this case only one rate is allowed during the search).
5. The value 64hex is a good compromise : acceptable bit error rate and good stability in case of low C/N conditions. The value 68hex is temporarily set during the "compensation of the VCO frequency drifts" routine.
6. Normally this register is read. However during the VCO coarse and fine adjust routines, this register is written to force the VCO position.
7. The derotator bandwidth is lowered (91hex) under low C/N conditions in order to optimize the BER. The derotator bandwidth is wide (A3hex) during the search to fasten the sacnning of the different derotator ranges. The derotator bandwidth is also wide (A3hex) in normal conditions (when C/N is high) in order to be less sensitive to the microphonic effect which may happen in the tuner.
8. Normally it is a read register. However during the scanning of the derotator ranges (search) this register is written to force the derotating frequency.
9. The AGC reference is typically 14hex (20 dec). However when estimating high C/N ratios, its value is temporarily modified (see ANNEXE 1 of the STV0196B specification).

IV - FIXED RATE APPLICATIONS

In these applications only one symbol rate is satisfied (ex : 20Mbauds).
Naturally it is a simple case which can be covered by a multirate application. However in order to simplify both the hardware and the software, the application is different :
- The clock signal (timing) is generated by a VCXO (crystal).
- The software does not need all the routines related to the VCO.

IV.1 - Timing Loop : Hardware Description

The timing loop is made of a VCXO (voltage controled Xtal oscillator) made of discrete components. In this structure the VCXO is inside a phase lock loop (PLL).
The central frequency of the crystal is 2Fs. The frequency control is only required to ensure the lock whatever the dispersions of the crystal frequency (initial accuracy, thermal drifts, aging). The sum of all those dispersions is about ±100 ppm.
Overtone 3 type of XTAL may be used as long as the pull range is ≥100ppm.

IV.2 - STV0196 Software Driver

As far as the software is concerned the only differences between fixed rate and multirate applications are related to the timing loop. In fixed rate the following routines do not exist :
- during the search : the VCO coarse and fine timing
- during the normal process : compensation of the VCO frequency drifts.

The only care is : To load REG hex 0C with 00hex and Reg hex 0D with 00hex during the tuner settling time, so that the timing loop is opened and well centered before to close it. In doing so, the capture time is satistically minimized.

V - PCB LAYOUT RECOMMANDATIONS

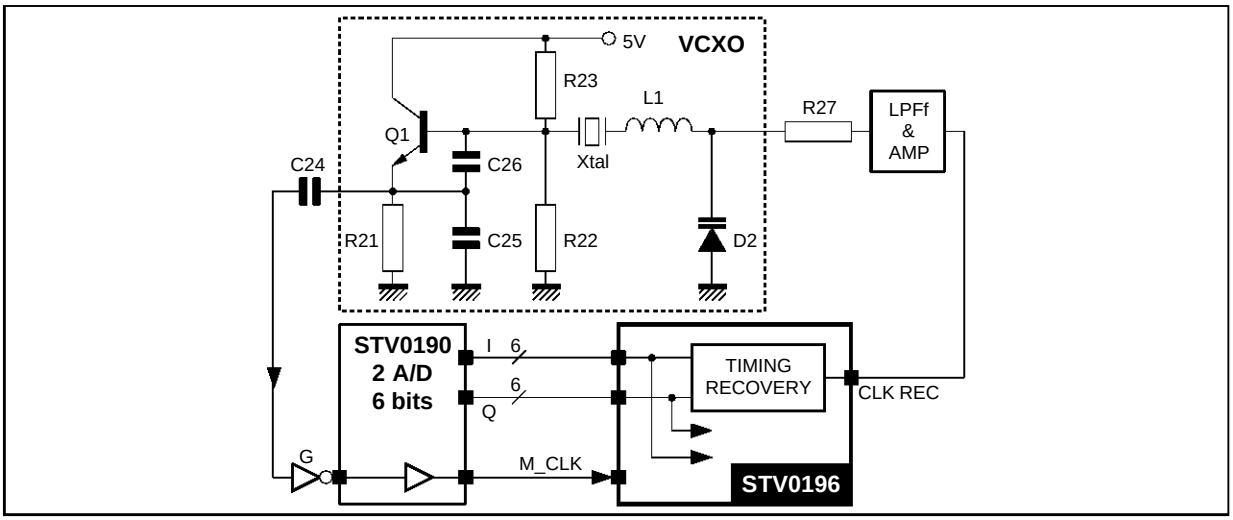
As any circuitry envolving both analog and digital parts, a lot of care has to be taken in the PCB layout and especially in the gound paths.

The basic rules are :
- to have two ground paths (analog and digital) well separated and linked with only one track.
- on the analog side, are connected :
  - the filtering capacitors of the tuner supply voltages (5V, 12V, 28V)
  - the filtering capacitor of the STV0190 V_{DDA} line
  - the filtering capacitors of V_{TOP}, V_{BOT}, V_{MIDA}, V_{MIDB} of the STV0190
- on the digital side, are connected :
  - the VDDL filtering capacitor of the STV0190
  - the VDDL filtering capacitors of the STV0196
  - the ground of the VC0
  - the ground of the operational amplifier (U4 of the demoboard)

Remark : In order to avoid phase jitter in the VCO signal, the ground of the operational amplifier is connected to a ground path which returns to the VCO before to be connected to the general digital ground.

Other PCB layout advices :
- To have the shortest connections as possible between the gate (U2 in the demoboard) and the CLKIN pin of the STV0190.
- To have the shortest connections as possible between the STV0190 outputs and the STV0196 I/Q inputs (if possible less than 3cm).
- To separate the analog and digital 3.3V supply lines by a filtering inductance (typically 22µH), same remark about the 5V supply line.
- When a multilayer PCB technology is used, it is recommanded not to have ground patch under the VCO (it generates parasitic capacitances which may change the VCO frequency).

Figure 18 : Fixed Rate Application, Timing Loop



VI - ANNEXE 1

The purpose of this chapter is to estimate the maximum waiting duration θ which is needed between the carrier found flag detection (Reg Hex 08 b7) and the data/synchro found flag detection (Reg Hex 08 b3).

This duration θ corresponds to the sum of two searches : Viterbi search Tv and Synchro search Ts :

$$\theta = Tv + Ts \qquad (20)$$

VI.1 - Estimation of the Maximum Tv Duration

The Viterbi decoder ensures the followings recognition :

A Puncture rate recognition.
B Puncture rate phase recognition.
C Check the potential 90° phase ambiguity of the QPSK demodulation.

The VITERBI decoder operates the search as follows :

A Check one after the other all the authorized puncture rates (1/2, 2/3, 3/4, 5/6, 7/8).
Remark : the puncture to be searched may be known by the Network Information Tables before to operate the search. In such a case, this puncture rate only is authorised. In doing so, the total search time can be dramatically shortened.

B Inside each puncture rate, the Viterbi decoder checks one after the other all the phases of the current puncture rate. The following table gives the number of phase Np for each puncture rate.

Puncture rate	1/2	2/3	3/4	5/6	7/8
Number of phases	1	3	2	6	8

C If all the phases of the current puncture rate have been unsuccessfully tested, the Viterbi decoder checks again all the phases with a 90° phase rotation.

Calculation of Tv

The duration Ts of each step of the operations A, B and C is programmable by means of the SN[1..0] bits (Reg Hex06 b4 b5).

$$Ts = \frac{BC}{2Fs \cdot PR} \qquad (21)$$

BC : Bit count selected by the SN bits.
Fs : Symbol rate.
PR : Current puncture rate.

Consequently for each puncture rate, the duration Tpr of the search is :

$$(Tpr)_i = 2 \cdot (Np)_i \cdot (Ts)_i \qquad (22)$$

So the maximum search time Tv can be estimated as follows (n : number of authorized puncture rates) :

$$Tv = \sum_{1}^{n} (Tpr)_i \qquad (23)$$

Exemple : Reg Hex 06 = 2D, Reg Hex 10 = 1F, Fs = 20 MBauds ⇒ Tv = 20.97ms.

VI.2 - Estimation of the Duration Ts

The synchro search operation starts as soon as the puncture rate is found. The synchro search can be divided in two steps :

- synchro word detection : its maximum duration To is programmable by means of TO[1..0] bits (Reg Hex 06 b2, b3).

$$To = \frac{(BC)_0}{2Fs \cdot PR}$$

BCo : bit count selected by the TO[1..0] bits

- and a synchro word counting session untill the count reaches a value choosen by the H[1..0] bits (Reg Hex 06 b0, b1). The duration Th of this session is :

$$Th = 8 \cdot \frac{BY}{2Fs \cdot PR} \cdot 204$$

BY : Hystersis given by the H[1..0] bits.

VI.3 - Exemple

Hypothesis :
Search with Reg Hex 06 = 2D and Reg Hex 10 = 1F
Additionnaly, assuming that the found puncture rate is : 3/4
Symbol rate Fs = 20 Mbauds
Results : Tv = 20.97ms, Ts = 6.1ms ⇒ θ = 27.07ms