

# Servo signal processor for CD

## BU9312AKS

The BU9312AKS is a CD servo signal processing IC that contains a speed doubling unadjusted PLL, program servo, and signal processor, and that delivers low voltage operation and low power consumption. This IC is ideal for miniaturized, low-power-consumption applications.

### ●Applications

Portable CD players, portable stereos and mini component stereo systems

### ●Features

- 1) Internal PLL circuit, allowing EFM data demodulation and bit clock sampling with minimum attached components.
- 2) Frame synch signal detection and protection.
- 3) Internal focus, tracking and thread servo filters. Characteristics can be controlled with commands from the controller.
- 4) Subcode serial output pin.
- 5) Output pins for P code and Q code.
- 6) Internal CLV sequencer that automatically sets the CLV mode.
- 7) Internal track jump sequencer that jumps the desired number of tracks.
- 8) Single-chip IC with deinterleaving function and internal C1 / C2 double error detection, correction and flag processor.
- 9) Signals to DAC are output via MSB fast 2<sup>SCOMP</sup> serial outputs, enabling control of ON / OFF operation of CD-ROM interpolators.
- 10) 16k bits of internal SRAM, for the storage of up to  $\pm 4$  frames of jitters.
- 11) Doubled-speed playback.

● Absolute maximum ratings (Ta = 25°C)

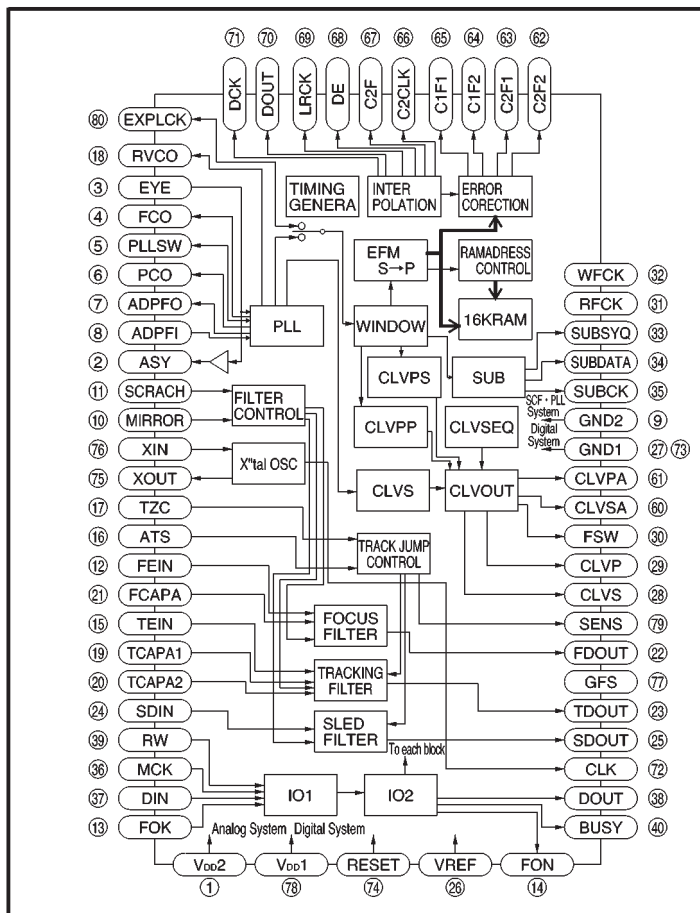
| Parameter             | Symbol           | Limits   | Unit |
|-----------------------|------------------|----------|------|
| Power supply voltage  | V <sub>CC</sub>  | 7        | V    |
| Power dissipation     | P <sub>d</sub>   | 400*     | mW   |
| Operating temperature | T <sub>opr</sub> | −25~+75  | °C   |
| Storage temperature   | T <sub>stg</sub> | −55~+125 | °C   |

\* Reduced by 4.0 mW for each increase in Ta of 1°C over 25°C.

● Recommended operating conditions (Ta = 25°C)

| Parameter            | Symbol          | Min. | Typ. | Max. | Unit |
|----------------------|-----------------|------|------|------|------|
| Power supply voltage | V <sub>CC</sub> | 3.0  | —    | 5.5  | V    |

● Block diagram



## ● Pin description

| Pin No. | Pin name | Analog / digital | I / O | Function   | I / O circuit |
|---------|----------|------------------|-------|--|---------------|
| 1       | VDD2     | —                | —     | PLL and servo filter block power supply                      | —             |
| 2       | ASY      | Digital          | O     | EFM signal slicing level control output                      | Fig.5         |
| 3       | EYE      | Digital          | I     | Input of EFM signals from the RF amplifier                   | Fig.4         |
| 4       | FCO      | Analog           | O     | PLL frequency comparison error voltage output                | Fig.7         |
| 5       | PLLSW    | Digital          | O     | PLL time constant switching                                  | Fig.3         |
| 6       | PCO      | Analog           | O     | PLL phase comparison error voltage output                    | Fig.7         |
| 7       | ADPFO    | Analog           | O     | PLL adding amplifier output                                  | Fig.2         |
| 8       | ADPFI    | Analog           | I     | PLL adding amplifier inverted input                          | Fig.1         |
| 9       | GND2     | —                | —     | PLL servo filter block ground                                | —             |
| 10      | MIRROR   | Digital          | I     | Mirror signal input  | Fig.4         |
| 11      | SCRACH   | Digital          | I     | Scratch signal input   | Fig.4         |
| 12      | FEIN     | Analog           | I     | Focus error signal input                                     | Fig.1         |
| 13      | FOK      | Digital          | I     | Focus OK signal input  | Fig.4         |
| 14      | FON      | Digital          | O     | Focus ON signal output                                       | Fig.5         |
| 15      | TEIN     | Analog           | I     | Tracking error signal input                                  | Fig.1         |
| 16      | ATS      | Analog           | I     | Anti-shock detection window comparator input                 | Fig.1         |
| 17      | TZC      | Analog           | I     | Tracking zero-cross comparator input                         | Fig.1         |
| 18      | RVCO     | Analog           | O     | PLL VCO free running resistor                                | Fig.2         |
| 19      | TCAPA1   | Analog           | I / O | Tracking servo filter capacitor connection                   | Fig.6         |
| 20      | TCAPA2   | Analog           | I / O | Tracking servo filter capacitor connection                   | Fig.6         |
| 21      | FCAPA    | Analog           | I / O | Focus servo filter capacitor connection                      | Fig.6         |
| 22      | FDOUT    | Analog           | O     | Focus driver output  | Fig.2         |
| 23      | TDOUT    | Analog           | O     | Tracking drive output  | Fig.2         |
| 24      | SDIN     | Analog           | I     | Thread amplifier input                                       | Fig.1         |
| 25      | SDOUT    | Analog           | O     | Thread driver output   | Fig.2         |
| 26      | VREF     | Analog           | I     | Bias voltage input   | Fig.6         |
| 27      | GND1     | —                | —     | Digital ground   | —             |
| 28      | CLVS     | Digital          | O     | Spindle motor drive output (speed control output)            | Fig.7         |
| 29      | CLVP     | Digital          | O     | Spindle motor drive output (rough or phase control output)   | Fig.7         |
| 30      | FSW      | Digital          | O     | Spindle motor output (filter time constant switching output) | Fig.3         |
| 31      | RFCK     | Digital          | O     | Read frame clock output (X'tal 7.35 kHz)                     | Fig.5         |
| 32      | WFCK     | Digital          | O     | Write frame clock output (7.35 kHz when locked on X'tal)     | Fig.5         |
| 33      | SUBSYQ   | Digital          | O     | Subcode sink S0 + S1 output                                  | Fig.5         |
| 34      | SUBDATA  | Digital          | O     | Subcode serial output  | Fig.5         |

| Pin No. | Pin name          | Analog / digital | I / O | Function   | I / O circuit |
|---------|-------------------|------------------|-------|--|---------------|
| 35      | SUBCK             | Digital          | I     | Subcode read clock   | Fig.4         |
| 36      | MCK               | Digital          | I     | Clock for CPU serial data reading or sub Q code reading  | Fig.4         |
| 37      | DIN               | Digital          | I     | CPU serial data input  | Fig.4         |
| 38      | DOUT              | Digital          | O     | Sub Q code or internal status serial output  | Fig.7         |
| 39      | RW                | Digital          | I     | Read / write switching or track jump command input<br>(H = data output from DOUT, L = data input from DIN) | Fig.4         |
| 40      | BUSY              | Digital          | O     | Busy output (L during track jumping)   | Fig.5         |
| 41~59   | N.C.              | —                | —     | —  | —             |
| 60      | CLVPA             | Analog           | O     | CLV phase linear output  | Fig.1         |
| 61      | CLVSA             | Analog           | O     | CLV speed linear output  | Fig.1         |
| 62      | C2F2              | Digital          | O     | C2 double correction flag  | Fig.5         |
| 63      | C2F1              | Digital          | O     | C2 single correction flag  | Fig.5         |
| 64      | C1F2              | Digital          | O     | C1 double correction flag  | Fig.5         |
| 65      | C1F1              | Digital          | O     | C1 single correction flag  | Fig.5         |
| 66      | C2CLK             | Digital          | O     | Strobe signal (f = 176.4 kHz)  | Fig.5         |
| 67      | C2F               | Digital          | O     | Correction status output   | Fig.5         |
| 68      | DE                | Digital          | O     | Strobe signal (f = 88.2 kHz)   | Fig.5         |
| 69      | LRCK              | Digital          | O     | Strobe signal (f = 44.1 kHz)   | Fig.5         |
| 70      | DOUTA             | Digital          | O     | Audio data output (2'SCOMP)  | Fig.5         |
| 71      | DOCK              | Digital          | O     | DOUTA bit clock (f = 2.1168 MHz)   | Fig.5         |
| 72      | CLK               | Digital          | O     | Clock output (4 settings selected with &hE4 command)   | Fig.5         |
| 73      | GND1              | —                | —     | Digital ground   | —             |
| 74      | RESET             | Digital          | I     | Internal circuit reset (pulled up with 100 k $\Omega$ internal resistor)                                   | Fig.8         |
| 75      | XOUT              | Digital          | O     | X'tal oscillator output (f = 16.9 MHz)   | Fig.9         |
| 76      | XIN               | Digital          | I     | X'tal oscillator input (f = 16.9 MHz)  | Fig.9         |
| 77      | GFS               | Digital          | O     | GFS monitor output (4 settings selected with &hE4 command)   | Fig.5         |
| 78      | V <sub>DD</sub> 1 | —                | —     | Digital power supply   | —             |
| 79      | SENS              | Digital          | O     | Status output for signal selected with the &hE4 command  | Fig.5         |
| 80      | EXPLCK            | Digital          | I / O | PLL output and playback clock input for attached PLL   | Fig.10        |

## ● Input / output circuits

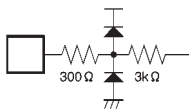


Fig. 1

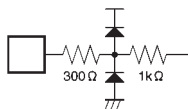


Fig. 2

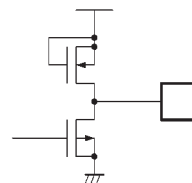


Fig. 3

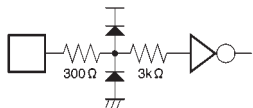


Fig. 4



Fig. 5

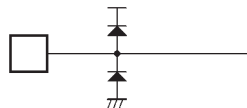


Fig. 6

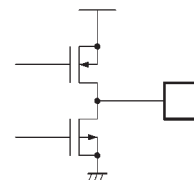


Fig. 7

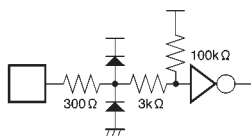


Fig. 8

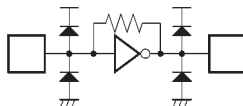


Fig. 9

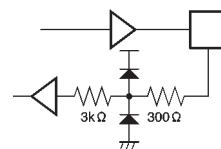


Fig. 10

● Electrical characteristics (unless otherwise noted, Ta = 25°C, V<sub>DD</sub> = 5V)

| Parameter                  | Symbol          | Min. | Typ. | Max.            | Unit | Conditions                    | Suitable pins |
|----------------------------|-----------------|------|------|-----------------|------|-------------------------------|---------------|
| Input voltage, high level  | V <sub>IH</sub> | 3.5  | —    | —               | V    |                               | *1            |
| Input voltage, low level   | V <sub>IL</sub> | —    | —    | 0.3             | V    |                               | *1            |
| Output voltage, high level | V <sub>OH</sub> | 4.0  | —    | V <sub>DD</sub> | V    | I <sub>OH</sub> = -1mA        | *2            |
| Output voltage, low level  | V <sub>OL</sub> | 0    | —    | 0.4             | V    | I <sub>OL</sub> = 1mA         | *2, 5         |
| Input resistance 1         | V <sub>O1</sub> | 80   | 100  | 120             | kΩ   | Between V <sub>DD1</sub> pins | *3            |
| Input resistance 2         | V <sub>O2</sub> | 60   | 75   | 90              | kΩ   | Between BIAS pins             | TZC           |
| Input resistance 3         | V <sub>O3</sub> | 180  | 230  | 280             | kΩ   | Between BIAS pins             | ATS           |
| Input resistance 4         | V <sub>O4</sub> | 20   | 25   | 30              | kΩ   | Between BIAS pins             | *6            |
| Input leakage current      | I <sub>LI</sub> | —    | —    | ±5              | μA   | V <sub>I</sub> = 0~5.25V      | *1, 2         |
| Output leakage current     | I <sub>LO</sub> | —    | —    | ±5              | μA   | V <sub>O</sub> = 0~5.25V      | *4, 5         |

Suitable pins

\*1 MIRROR, SCRACH, FOK, SUBCK, MCK, DIN, RW, RESET, EXPLCK, EYE

\*2 FON, CLVS, CLVP, RFCK, WFCK, SUBSYQ, SUBDATA, DOUT, BUSY, XOUT, SENS, GFS, ASY, C1F1, C1F2, C2F1, C2F2, C2CLK, C2F, DE, LRCK, DOCK, CLK

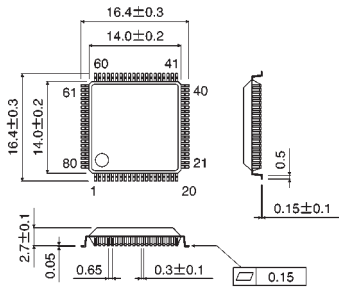
\*3 RESET

\*4 CLVS, CLVP

\*5 PLLSW, TCAPA2, FSW

\*6 FEIN, TEIN

## ● External dimensions (Units: mm)



SQFP80