PCM codec IC for digital cellular telephones BU8731KV

The BU8731KV is a PCM codec IC developed for use with digital cellular telephones. It contains analog input / output features such as a 14-bit linear precision, μ / A-LAW codec, mic and speaker amplifiers, and switching transistor for the ringer drive. This all makes the BU8731KV perfect for PDC and CDMA-type cellular telephones.

Applications

Digital cellular telephones

Features

- 1) +3V single power supply ($V_{DD} = 2.7V$ to 3.3V).
- 2) Built-in 14-bit precision linear, μ / A-LAW codec.
- Transmission filter for the codec unit conforms to ITU-T recommendations.
- 4) Built-in PLL circuit for system clock generation.
- Clock frequency for PCM data transmission can be set anywhere between 64kHz (128kHz when linear) to 2048kHz.
- 6) Analog input / output functions:
 - · Built-in mic amplifier.
 - Built-in receiver speaker amplifier (32 Ω BTL type).
 - Built-in earphone speaker amplifier (32 Ω single type).

- Built-in drive amplifier for reception REXT (600 Ω).
- Built-in electronic volume control for gain adjustment (for reception, transmission, and tone).
- Data signal I / O circuit allows for connection to external devices.
- For the REXT output and earphone output, softmute function reduces pop noise when the power is turned on and off.
- DTMF signal and scale tone signal generator functions are built into the tone signal generator block.
- 8) Internal switching transistor for ringer drive.
- 9) VQFP 48-pin package.

● Absolute maximum ratings (Ta = 25°C)

| Parameter | Symbol | Limits | Unit |
|---------------------------------|-------------------|---------------------|------|
| Digital power supply voltage | DV _{DD} | −0.3∼+4.5 | V |
| Amalan massau assaults scallana | RXV _{DD} | -0.3~+4.5 | ٧ |
| Analog power supply voltage | TXV _{DD} | -0.3~+4.5 | V |
| Digital input voltage | VDIN | DVss-0.3~DVpp+0.3 | V |
| A mala minumuk walka ma | 1/ | RXVss-0.3~RXVpp+0.3 | V |
| Analog input voltage | Vain | TXVss-0.3~TXVpp+0.3 | V |
| Input current | lin | -10~+10 | mA |
| Power dissipation | Pd | 400*1 | mW |
| Operating temperature | Tstg | −50~ +125 | °C |
| Storage temperature | Topr | −20~+85 | °C |

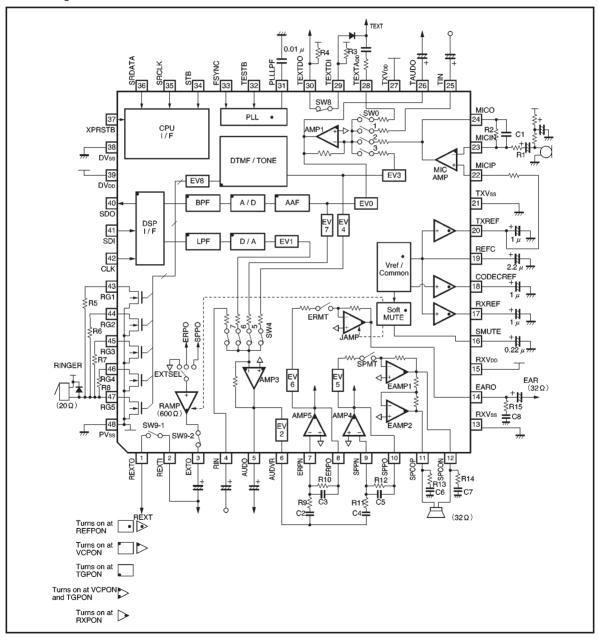
^{*1} Reduced by 4.0mW for each increase in Ta of 1°C over 25°C.

● Recommended operating conditions (Ta = 25°C)

| Parameter | Symbol | Min. | Тур. | Max. | Unit |
|------------------------------|-------------------|------|------|------|------|
| Digital power supply voltage | DVpp | 2.7 | _ | 3.3 | V |
| Analog power supply voltage | RXVDD | 2.7 | _ | 3.3 | V |
| Arialog power supply voltage | TXV _{DD} | 2.7 | _ | 3.3 | V |

ONot designed for radiation resistance.

Block diagram



Pin descriptions

| Pin No. Pin name I / O Function Minimum load resistance (Ω) Maximum load capacitance (F 1 N N N N N N N N N | | | | | | l |
|--|----|--------|-----|---|------------------------------------|---------------------------------------|
| REXTI 1/O Reception data input | | | | | Minimum load resistance (Ω) | Maximum load capacitance (F) |
| Section Rink Reception audio direct input Reception signal gain adjustment Sok Sop | 1 | REXTO | 1/0 | Reception data output | _ | _ |
| RIN | 2 | REXTI | 1/0 | Reception data input | _ | _ |
| 5 AUDO O Reception signal direct output 50k 50p 6 AUDVR O Reception signal external output 50k 50p 7 ERPN I Amplifier output for earphone gain adjustment — — 8 ERPO O Amplifier output for earphone gain adjustment 50k 50p 9 SPPN I Amplifier output for speaker gain adjustment — — 10 SPPO O Amplifier inverse input for speaker gain adjustment 50k 50p 11 SPCOP O Receiver speaker amplifier non-inverse output 32 (BTL) — 12 SPCON O Receiver speaker amplifier inverse output 32 (BTL) — 13 RXVss — Analog ground for reception — — 14 EARO Earphone speaker amplifier output 32 — — 16 SMUTE I Time constant for soft mute setting — 0.22 μ*1 17 RXREF O <t< td=""><td>3</td><td>EXTO</td><td>0</td><td>Amplifier output for reception signal gain adjustment</td><td>600</td><td>-</td></t<> | 3 | EXTO | 0 | Amplifier output for reception signal gain adjustment | 600 | - |
| 6 AUDVR O Reception signal external output 50k 50p 7 ERPN I Amplifier inverse input for earphone gain adjustment — — — — — — — — — — — — — — — — — — — | 4 | RIN | -1 | Reception audio direct input | _ | _ |
| 7 ERPN I Amplifier inverse input for earphone gain adjustment — — 8 ERPO O Amplifier output for speaker gain adjustment 50k 50p 9 SPPN I Amplifier inverse input for speaker gain adjustment — — 10 SPPO O Amplifier output for speaker gain adjustment 50k 50p 11 SPPOOP O Receiver speaker amplifier non-inverse output 32 (BTL) — 12 SPCON O Receiver speaker amplifier output 32 (BTL) — 13 RXVss — Analog ground for reception — — 14 EARO O Earphone speaker amplifier output 32 — 15 RXVso — Analog power supply for reception — — 16 SMUTE I Time constant for soft mute setting — 0.22 μ*1 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF | 5 | AUDO | 0 | Reception signal direct output | 50k | 50p |
| 8 ERPO O Amplifier output for earphone gain adjustment 50k 50p 9 SPPN I Amplifier inverse input for speaker gain adjustment — — 10 SPPO O Amplifier output for speaker gain adjustment 50k 50p 11 SPCOP O Receiver speaker amplifier non-inverse output 32 (BTL) — 12 SPCON O Receiver speaker amplifier inverse output 32 (BTL) — 13 RXVss — Analog ground for reception — — 14 EARO O Earphone speaker amplifier inverse output 32 — 15 RXVso — Analog prower supply for reception — — 16 SMUTE I Time constant for soft mute setting — — — 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF O Analog reference voltage output for transmission — 1 μ*1 20 | 6 | AUDVR | 0 | Reception signal external output | 50k | 50p |
| 9 SPPN 1 Amplifier inverse input for speaker gain adjustment — — 10 SPPO 0 Amplifier output for speaker gain adjustment 50k 50p 11 SPCOP 0 Receiver speaker amplifier non-inverse output 32 (BTL) — 12 SPCON 0 Receiver speaker amplifier inverse output 32 (BTL) — 13 RXVss — Analog ground for reception — — 14 EARO 0 Earphone speaker amplifier output 32 — 15 RXVos — Analog preacher amplifier output 32 — 16 SMUTE I Time constant for soft mute setting — — — 16 SMUTE I Time constant for soft mute setting — — — 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF O Analog reference voltage output for transmission — 1 μ*1 20 | 7 | ERPN | -1 | Amplifier inverse input for earphone gain adjustment | _ | _ |
| 10 SPPO O Amplifier output for speaker gain adjustment 50k 50p 11 SPCOP O Receiver speaker amplifier non-inverse output 32 (BTL) — 12 SPCON O Receiver speaker amplifier inverse output 32 (BTL) — 13 RXVss — Analog ground for reception — — — — — — — — — — — — — — — — — — — | 8 | ERPO | 0 | Amplifier output for earphone gain adjustment | 50k | 50p |
| 111 SPCOP O Receiver speaker amplifier non-inverse output 32 (BTL) — 12 SPCON O Receiver speaker amplifier inverse output 32 (BTL) — 13 RXVss — Analog ground for reception — — 14 EARO O Earphone speaker amplifier output 32 — 15 RXVso — Analog power supply for reception — — 16 SMUTE I Time constant for soft mute setting — 0.22 μ*1 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF O Analog reference voltage output for codec — 1 μ*1 19 REFC O Analog reference voltage output for transmission — 2.2 μ*1 20 TXREF O Analog ground for transmission — 1 μ*1 21 TXVss — Analog ground for transmission — — 21 MICIP I Mic | 9 | SPPN | ı | Amplifier inverse input for speaker gain adjustment | _ | _ |
| 12 SPCON O Receiver speaker amplifier inverse output 32 (BTL) — 13 RXVss — Analog ground for reception — — 14 EARO O Earphone speaker amplifier output 32 — 15 RXVbo — Analog power supply for reception — — 16 SMUTE I Time constant for soft mute setting — 0.22 μ*1 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF O Analog reference voltage output for reception — 1 μ*1 19 REFC O Analog reference voltage output for codec — 1 μ*1 20 TXREF O Analog reference voltage output for transmission — 2.2 μ*1 20 TXREF O Analog reference voltage output for transmission — — 1 μ*1 21 TXVss — Analog ground for transmission — — — 21 | 10 | SPPO | 0 | Amplifier output for speaker gain adjustment | 50k | 50p |
| 13 RXVss — Analog ground for reception — — — — — — — — — — — — — — — — — — — | 11 | SPCOP | 0 | Receiver speaker amplifier non-inverse output | 32 (BTL) | _ |
| 14 EARO O Earphone speaker amplifier output 32 | 12 | SPCON | 0 | Receiver speaker amplifier inverse output | 32 (BTL) | _ |
| 15 RXVoo — Analog power supply for reception — — 16 SMUTE I Time constant for soft mute setting — $0.22\mu^{\pm1}$ 17 RXREF O Analog reference voltage output for reception — $1\mu^{\pm1}$ 18 CODCREF O Analog reference voltage output for codec — $1\mu^{\pm1}$ 19 REFC O Analog reference voltage output — $2.2\mu^{\pm1}$ 20 TXREF O Analog reference voltage output for transmission — $1\mu^{\pm1}$ 21 TXVss — Analog ground for transmission — — 22 MICIP I Mic amplifier non-inverse input — — 23 MICIN I Mic amplifier inverse input — — 24 MICO O Mic amplifier output 50k 50p 25 TIN I Transmission audio direct input — — 26 TAUDO O Transmission analog output 50k 50p 27 TXVoo — Analog power supply for transmission — — 28 TEXTADO I Transmission adata signal input — <td>13</td> <td>RXVss</td> <td>_</td> <td>Analog ground for reception</td> <td>_</td> <td>_</td> | 13 | RXVss | _ | Analog ground for reception | _ | _ |
| 16 SMUTE I Time constant for soft mute setting — 0.22 μ*1 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF O Analog reference voltage output for codec — 1 μ*1 19 REFC O Analog reference voltage output — 2.2 μ*1 20 TXREF O Analog reference voltage output — 2.2 μ*1 21 TXVss — Analog ground for transmission — 1 μ*1 21 TXVss — Analog ground for transmission — — — — 23 MICIN I Mic amplifier non-inverse input — — — — — — — — — — — — — — — — — — — | 14 | EARO | О | Earphone speaker amplifier output | 32 | _ |
| 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF O Analog reference voltage output for codec — 1 μ*1 19 REFC O Analog reference voltage output — 2.2 μ*1 20 TXREF O Analog reference voltage output — 2.2 μ*1 21 TXVss — Analog ground for transmission — 1 μ*1 21 TXVss — Analog ground for transmission — — — — — — — — — — — — — — — — — — — | 15 | RXVDD | _ | Analog power supply for reception | _ | _ |
| 17 RXREF O Analog reference voltage output for reception — 1 μ*1 18 CODCREF O Analog reference voltage output for codec — 1 μ*1 19 REFC O Analog reference voltage output — 2.2 μ*1 20 TXREF O Analog reference voltage output — 2.2 μ*1 21 TXVss — Analog ground for transmission — 1 μ*1 21 TXVss — Analog ground for transmission — — — — — — — — — — — — — — — — — — — | 16 | SMUTE | 1 | Time constant for soft mute setting | _ | 0.22 µ*1 |
| 18 CODCREF O Analog reference voltage output for codec $-$ 1 $μ^{*1}$ 19 REFC O Analog reference voltage output $-$ 2.2 $μ^{*1}$ 20 TXREF O Analog reference voltage output for transmission $-$ 1 $μ^{*1}$ 21 TXVss $-$ Analog ground for transmission $ -$ 22 MICIP I Mic amplifier non-inverse input $ -$ 23 MICIN I Mic amplifier inverse input $ -$ 24 MICO O Mic amplifier output $-$ 50k 50p 25 TIN I Transmission audio direct input $ -$ 26 TAUDO O Transmission analog output $-$ 50k 50p 27 TXVo _D $-$ Analog power supply for transmission $ -$ 28 TEXTADO I Transmission signal incremental input $ -$ 29 TEXTDI I/O Transmission data signal input $ -$ 30 TEXTDO I/O Transmission data signal output $ -$ 31 PLLLPF I/O Input/output filter connector for PLL circuit $-$ 0.01 $μ^{*1}$ 32 TESTB I Test input ($-$ DVo _D) $ -$ 33 FSYNC I PLL reference clock input $ -$ 35 SRCLK I CPU I/F strobe input $ -$ 36 SRDATA I CPU I/F address data input $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 38 $-$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 38 $-$ 37 XPRSTB I System reset input (L: reset) $ -$ 38 $-$ 37 XPRSTB I System reset input (L: reset) $ -$ 39 $-$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 $-$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 $-$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 $-$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 XPRSTB I System reset input (L: reset) $ -$ 39 XPRSTB I System reset input (L: reset) $-$ | 17 | RXREF | 0 | Analog reference voltage output for reception | _ | |
| 19 REFC O Analog reference voltage output $-$ 2.2 $μ^*1$ 20 TXREF O Analog reference voltage output for transmission $-$ 1 $μ^*1$ 21 TXVss $-$ Analog ground for transmission $ -$ 22 MICIP I Mic amplifier non-inverse input $ -$ 23 MICIN I Mic amplifier inverse input $ -$ 24 MICO O Mic amplifier output $-$ 50k 50p 25 TIN I Transmission audio direct input $ -$ 26 TAUDO O Transmission analog output $-$ 50k 50p 27 TXVpp $-$ Analog power supply for transmission $ -$ 28 TEXTAop I Transmission signal incremental input $ -$ 29 TEXTDI I/O Transmission data signal output $ -$ 30 TEXTDO I/O Transmission data signal output $ -$ 31 PLLLPF I/O Input/output filter connector for PLL circuit $-$ 0.01 $μ^*1$ 32 TESTB I Test input $(-+$ DVpp) $ -$ 33 FSYNC I PLL reference clock input $ -$ 35 SRCLK I CPU I/F strobe input $ -$ 36 SRDATA I CPU I/F stoke input $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ 37 XPRSTB I System reset input (L: reset) $ -$ | 18 | | 0 | Analog reference voltage output for codec | _ | |
| 20 TXREF O Analog reference voltage output for transmission — 1 μ*1 21 TXVss — Analog ground for transmission — — 22 MICIP I Mic amplifier non-inverse input — — 23 MICIN I Mic amplifier inverse input — — 24 MICO O Mic amplifier output 50k 50p 25 TIN I Transmission audio direct input — — 26 TAUDO O Transmission audio direct input — — — 26 TAUDO O Transmission audio direct input — — — 26 TAUDO O Transmission audio direct input — — — 26 TAUDO O Transmission audio direct input — — — 27 TXVbo — Analog power supply for transmission — — — 28 TEXTADO I Transmission signal incremental input — — — 29 T | 19 | | 0 | <u> </u> | _ | · · · · · · · · · · · · · · · · · · · |
| 21 TXVss — Analog ground for transmission — — 22 MICIP I Mic amplifier non-inverse input — — 23 MICIN I Mic amplifier inverse input — — 24 MICO O Mic amplifier output 50k 50p 25 TIN I Transmission audio direct input — — 26 TAUDO O Transmission analog output 50k 50p 27 TXVpp — Analog power supply for transmission — — 28 TEXTApp I Transmission signal incremental input — — 29 TEXTDI I / O Transmission data signal input — — 30 TEXTDO I / O Transmission data signal output — — 31 PLLLPF I / O Input/output filter connector for PLL circuit — — 31 PLLLPF I / O Input/output filter connector for PLL circuit — — — 32 TESTB I Test input (→DVpp) — — — — | 20 | | 0 | Analog reference voltage output for transmission | _ | |
| 22 MICIP I Mic amplifier non-inverse input — — 23 MICIN I Mic amplifier inverse input — — 24 MICO O Mic amplifier output 50k 50p 25 TIN I Transmission audio direct input — — 26 TAUDO O Transmission analog output 50k 50p 27 TXVob — Analog power supply for transmission — — 28 TEXTADD I Transmission signal incremental input — — 29 TEXTDI I/O Transmission data signal input — — — 30 TEXTDO I/O Transmission data signal output — — — 31 PLLLPF I/O Input/output filter connector for PLL circuit — 0.01 μ*1 32 TESTB I Test input (→DVob) — — 33 FSYNC I PLL reference clock input — < | 21 | | _ | <u> </u> | _ | _ |
| 23 MICIN I Mic amplifier inverse input — — — 24 MICO O Mic amplifier output 50k 50p 25 TIN I Transmission audio direct input — — 26 TAUDO O Transmission analog output 50k 50p 27 TXV _{DD} — Analog power supply for transmission — — 28 TEXTADD I Transmission signal incremental input — — 29 TEXTDI I / O Transmission data signal incremental input — — 30 TEXTDO I / O Transmission data signal output — — 31 PLLLPF I / O Input/output filter connector for PLL circuit — 0.01 μ*1 32 TESTB I Test input (→DVob) — — 33 FSYNC I PLL reference clock input — — 34 STB I CPU I/F strobe input — — | 22 | | | | _ | _ |
| 24 MICO O Mic amplifier output 50k 50p 25 TIN I Transmission audio direct input — — 26 TAUDO O Transmission analog output 50k 50p 27 TXV _{DD} — Analog power supply for transmission — — 28 TEXTA _{DD} I Transmission signal incremental input — — 29 TEXTDI I/O Transmission data signal input — — 30 TEXTDO I/O Transmission data signal output — — 31 PLLLPF I/O Input/output filter connector for PLL circuit — — 0.01 μ*1 32 TESTB I Test input (→DV _{DD}) — — — 33 FSYNC I PLL reference clock input — — — 34 STB I CPU I/F strobe input — — — 35 SRCLK I CPU I/F shift clock input | | | | | _ | _ |
| 25 TIN I Transmission audio direct input — — 26 TAUDO O Transmission analog output 50k 50p 27 TXV _{DD} — Analog power supply for transmission — — 28 TEXTADD I Transmission signal incremental input — — 29 TEXTDI I / O Transmission data signal input — — 30 TEXTDO I / O Transmission data signal output — — 31 PLLLPF I / O Input/output filter connector for PLL circuit — — 0.01 μ*1 32 TESTB I Test input (→DV _{DD}) — — — 33 FSYNC I PLL reference clock input — — — 34 STB I CPU I/F strobe input — — — 35 SRCLK I CPU I/F address data input — — — 36 SRDATA I CPU | | | | , | 50k | 50p |
| 26 TAUDO O Transmission analog output 50k 50p 27 TXV _{DD} — Analog power supply for transmission — — 28 TEXTADD I Transmission signal incremental input — — 29 TEXTDI I / O Transmission data signal input — — 30 TEXTDO I / O Transmission data signal output — — 31 PLLLPF I / O Input/output filter connector for PLL circuit — 0.01 μ*1 32 TESTB I Test input (→DV _{DD}) — — 33 FSYNC I PLL reference clock input — — 34 STB I CPU I/F strobe input — — 35 SRCLK I CPU I/F shift clock input — — 36 SRDATA I CPU I/F address data input — — — 37 XPRSTB I System reset input (L: reset) — — < | | | | • • | _ | _ |
| 27 TXV _{DD} — Analog power supply for transmission — — 28 TEXTA _{DD} I Transmission signal incremental input — — 29 TEXTDI I / O Transmission data signal input — — 30 TEXTDO I / O Transmission data signal output — — 31 PLLLPF I / O Input/output filter connector for PLL circuit — 0.01 μ*1 32 TESTB I Test input (→DV _{DD}) — — 33 FSYNC I PLL reference clock input — — 34 STB I CPU I/F strobe input — — 35 SRCLK I CPU I/F shift clock input — — 36 SRDATA I CPU I/F address data input — — 37 XPRSTB I System reset input (L: reset) — — | | | 0 | | 50k | 50p |
| 28 TEXTADD I Transmission signal incremental input — — 29 TEXTDI I / O Transmission data signal input — — 30 TEXTDO I / O Transmission data signal output — — 31 PLLLPF I / O Input/output filter connector for PLL circuit — 0.01 μ*1 32 TESTB I Test input (→DV _{DD}) — — 33 FSYNC I PLL reference clock input — — 34 STB I CPU I/F strobe input — — 35 SRCLK I CPU I/F shift clock input — — 36 SRDATA I CPU I/F address data input — — 37 XPRSTB I System reset input (L: reset) — — | | | _ | <u> </u> | _ | _ |
| 29 TEXTDI I / O Transmission data signal input — | 28 | | ı | ** | _ | _ |
| 30 TEXTDO I / O Transmission data signal output — — — | 29 | | 1/0 | <u> </u> | _ | _ |
| 32 TESTB I Test input (→DVob) — — 33 FSYNC I PLL reference clock input — — 34 STB I CPU I/F strobe input — — 35 SRCLK I CPU I/F shift clock input — — 36 SRDATA I CPU I/F address data input — — 37 XPRSTB I System reset input (L: reset) — — | 30 | | 1/0 | <u> </u> | _ | _ |
| 32 TESTB I Test input (→DVob) — — 33 FSYNC I PLL reference clock input — — 34 STB I CPU I/F strobe input — — 35 SRCLK I CPU I/F shift clock input — — 36 SRDATA I CPU I/F address data input — — 37 XPRSTB I System reset input (L: reset) — — | 31 | PLLLPF | 1/0 | Input/output filter connector for PLL circuit | _ | 0.01 μ*1 |
| 34 STB I CPU I/F strobe input — — 35 SRCLK I CPU I/F shift clock input — — 36 SRDATA I CPU I/F address data input — — 37 XPRSTB I System reset input (L: reset) — — | 32 | TESTB | 1 | Test input (→DVɒɒ) | _ | _ |
| 35 SRCLK I CPU I/F shift clock input — — — | 33 | FSYNC | 1 | PLL reference clock input | _ | _ |
| 36 SRDATA I CPU I/F address data input - - - | 34 | STB | 1 | CPU I/F strobe input | _ | _ |
| 37 XPRSTB I System reset input (L: reset) — — | 35 | SRCLK | ı | CPU I/F shift clock input | _ | _ |
| | 36 | SRDATA | 1 | CPU I/F address data input | _ | _ |
| 38 DVss — Digital ground — — — | 37 | XPRSTB | Ī | System reset input (L: reset) | _ | _ |
| | 38 | DVss | | Digital ground | _ | _ |

^{*1} Recommended value.

| Pin No. | Pin name | 1/0 | Function | Minimum load resistance (Ω) | Maximum load capacitance (F) |
|---------|------------------|-----|----------------------------------|-----------------------------|------------------------------|
| 39 | DV _{DD} | - | Digital power supply | _ | _ |
| 40 | SDO | 0 | PCM signal output | _ | _ |
| 41 | SDI | 1 | PCM signal input | _ | _ |
| 42 | CLK | -1 | PCM signal shift clock input | _ | _ |
| 43 | RG1 | 0 | Ringer drive transistor output 1 | 100 (for 3V) | _ |
| 44 | RG2 | 0 | Ringer drive transistor output 2 | 60 (for 3V) | _ |
| 45 | RG3 | 0 | Ringer drive transistor output 3 | 40 (for 3V) | _ |
| 46 | RG4 | 0 | Ringer drive transistor output 4 | 30 (for 3V) | _ |
| 47 | PG5 | 0 | Ringer drive transistor output 5 | 20 (for 3V) | _ |
| 48 | PVss | _ | Ground for ringer | _ | _ |



● Electrical characteristics (unless otherwise noted, Ta = 25°C, DV_{DD} = RXV_{DD} = TXV_{DD} = 3.0V, FSYNC = 8kHz)

| Parameter | Symbol | Min. | Тур. | Max. | Unit | Conditions |
|-----------------------------------|--------|--------------------------|------|-------------------------|------|--|
| 〈DC characteristics〉 | | | • | | | |
| | IDD1 | _ | 8.0 | (11.5) | mA | All power on (FSYNC=8kHz) |
| | loo2 | _ | 7.0 | (10.2) | mA | Reference, audio, SPC on (FSYNC=8kHz) |
| | IDD3 | _ | 6.0 | (8.6) | mA | Reference, audio, earphone on (FSYNC=8kHz) |
| Current consumption*1 | IDD4 | _ | 5.4 | (7.8) | mA | Reference, audio, RAMP on (FSYNC=8kHz) |
| | IDD5 | _ | 5.1 | (7.3) | mA | Reference and audio on (FSYNC=8kHz) |
| | IDD6 | _ | 3.7 | (5.3) | mA | Reference and tone on (FSYNC=8kHz) |
| | loo7 | _ | 3.3 | (4.8) | mA | Only reference on (FSYNC=8kHz) |
| | BDD8 | _ | 0.1 | 20 | μΑ | Complete power down (FSYNC=fixed) |
| Digital input high level voltage | ViH | 0.8 DV _{DD} | _ | _ | V | _ |
| Digital input low level voltage | VıL | _ | _ | 0.2 DV _{DD} | V | - |
| Digital input high level current | Іін | _ | _ | 10 | μΑ | V _{IH} =DV _{DD} |
| Digital input low level current | lι∟ | -10 | _ | _ | μΑ | V _{IL} =0V |
| Digital output high level voltage | Vон | DV _{DD} -0.5 | _ | _ | V | Ioн=—1mA |
| Digital output low level voltage | Vol | _ | _ | 0.5 | ٧ | loL=1mA |

^{*1} The power supply voltage (DVDD, RXVDD, and TXVDD) is 3V. There is no load on the digital and analog output pins. Digital input pins other than the FSYNC and CLK pins are connected to DVDD or DVss.

Analog input pins are connected to TXREF or RXREF with the proper resistance.

With soft mute off (SMUTE=0).

Communication ICs BU8731KV

●Electrical characteristics (unless otherwise noted, Ta = 25°C, DV_{DD} = RXV_{DD} = TXV_{DD} = 3.0V, FSYNC = 8kHz, gain of each attenuator = 0dB)

| Parameter | Symbol | Min. | Тур. | Max. | Unit | Conditions | | | |
|--|------------------|-------|-------------|-------|-------|-------------------------------------|-----------------|----------------------------------|--|
| ⟨Transmission charact | eristics> | | | | | | | | |
| Signal to total power | | 24 | _ | _ | | | -45dBm0 | | |
| distortion ratio (A→D) | Spt | 29 | _ | _ | dB | 1020Hz reference | -40dBm0 | C-Wgt | |
| TEXTADD→SDO | | 35 | _ | _ | | 10.0.0.0 | 0~-30dBm0 | | |
| Signal to total power | | 24 | _ | _ | | | -45dBm0 | | |
| distortion ratio (D→A) | SDR | 29 | _ | _ | dB | 1020Hz reference | -40dBm0 | C-Wgt | |
| SDI→AUDO | | 35 | _ | _ | | | 0~-30dBm0 | | |
| Transmission level | | -0.9 | _ | 0.9 | | | −55dBm0 | Reference level | |
| characteristics (A→D) | G тх | -0.6 | _ | 0.6 | dB | 1020Hz reference | —50dBm0 | =-10dBm0 | |
| TEXTADD→SDO | | -0.3 | _ | 0.3 | | 7010101100 | 0~-40dBm0 | C-Wgt | |
| Transmission level | | -0.9 | _ | 0.9 | | | —55dBm0 | Reference level | |
| characteristics (D→A) | GTR | -0.6 | _ | 0.6 | dB | 1020Hz reference | -50dBm0 | =-10dBm0 | |
| SDI→AUDO | | -0.3 | _ | 0.3 | | | 0~-40dBm0 | C-Wgt | |
| Transmission output lovel | Vотх | 0.275 | 0.346 | 0.436 | Vrms | 1020Hz, 0dBm0 input reference | MICO→SDO | MICO output level is measured | |
| Transmission output level | | 0.275 | 0.346 | 0.436 | Vrms | | TEXTADD →SDO | TEXTADD input leve is measured | |
| Reception output level | Vorx | 0.291 | 0.346 | 0.411 | Vrms | 1020Hz, 0dBm0 input reference | SDI→AUDO | _ | |
| Transmission noise during no conversation | V _{NTX} | _ | —75 | -65 | dBm0C | _ | MIC→SDO | C-Wgt | |
| Reception noise during no conversation | VNRX | _ | — 79 | -70 | dBm0C | _ | SDI→AUDO | C-Wgt | |
| | | 24 | _ | _ | | | 0.06kHz | | |
| | | 0 | _ | 2.5 | | | 0.2kHz | | |
| Transmission loss frequency characteristics | | -0.3 | _ | 0.3 | - In | 1020Hz, | 0.3~3.0kHz | | |
| (A→D) | GRX | -0.3 | _ | 0.9 | - dB | 0dBm0 input reference | 3.4kHz | _ | |
| TEXTADD→SDO | | 0 | _ | _ | | | 3.6kHz | | |
| | | 6.5 | _ | _ | | | 3.78kHz | | |
| Transmission loss | | -0.3 | _ | 0.3 | | | 0.0~3.0kHz | | |
| frequency characteristics | | -0.3 | _ | 0.9 | 1 | 1020Hz, | 3.4kHz | | |
| (D→A) SDI→AUDO | GRR | 0 | _ | _ | - dB | 0dBm0 input reference | 3.6kHz | _ | |
| ,. | | 6.5 | _ | _ | 1 | | 3.78kHz | | |



| Param | eter | Symbol | Min. | Тур. | Max. | Unit | Conditions | | | |
|-----------------|--------|------------------|---------------------|------|-------|------|---------------------------|----------------|-----------|--|
| ⟨Tone genera | tor〉 | | | | | | | | | |
| | HTONE | V _{TNH} | -16 -14 -12 | | →AUDO | | | | | |
| Tone output | IIIONL | VINH | — 16 | -14 | -12 | dBV | Set at 2kHz | →SDO | 30kHz LPF | |
| level | LTONE | VTNL | -16 | -14 | -12 | | | →AUDO | | |
| Tone distortion | n | SDTN | _ | -40 | -29 | dB | HTONE set at 2kHz →AUDO | | 30kHz LPF | |
| ⟨Attenuator⟩ | | | I | | | | 1 | | | |
| | EV0 | Gvo | 10 | 12 | 14 | | MICO→SDC |), EV0=12dB | | |
| | EV1 | Gv ₁ | 1 | 3 | 5 | | SDI→AUDO | , EV1=3dB | | |
| | EV2 | Gv2 | -2 | 0 | 2 | | SDI→AUDV | R, EV2=0dB | | |
| Absolute | EV3 | Gvз | 4 | 6 | 8 | -ID | →SDO, EV3 | =6dB | | |
| gain | EV4 | Gv4 | 4 | 6 | 8 | dB | →AUDO, E\ | →AUDO, EV4=6dB | | |
| | EV5 | Gv5 | 12 | 14 | 16 | | SPPO→SPCOP-SPCON, EV5=8dB | | | |
| | EV6 | Gv6 | 6 | 8 | 10 | | ERPO→EARO, EV6=8dB | | | |
| | EV7 | Gv7 | -7 | -5 | -3 | | MICO→AUDO, EV7=-5dB | | | |
| | EV0 | Gewo | -31 | _ | 0 | | →SDO | | | |
| | EV1 | GEW1 | -7 | _ | 0 | | →AUDO | | | |
| | EV2 | GEW2 | —31 | _ | 0 | | →AUDVR | | | |
| Volum | EV3 | GEW3 | — 31 | _ | 0 | 40 | →SDO | | | |
| level setting | EV4 | GEW4 | —31 | _ | 0 | dB | →AUDO | | | |
| | EV5 | GEW5 | -15 | _ | 0 | | →SPCOP-SPCON | | | |
| | EV6 | GEW6 | —15 | _ | 0 | | →EARO | →EARO | | |
| | EV7 | GEW7 | -15 | _ | 0 | | →AUDO | | | |
| | EV0 | ΔGE0 | 0.2 | 1 | 1.8 | | →SDO | | | |
| | EV1 | ΔGE1 | 0.2 | 1 | 1.8 | | →AUDO | | | |
| | EV2 | ∆ GE2 | 0.2 | 1 | 1.8 | | →AUDVR | | | |
| Volume | EV3 | Δ GE3 | 0.2 | 1 | 1.8 | 4D | →SDO | | | |
| step width | EV4 | ∆ GE4 | 0.2 | 1 | 1.8 | dB | →AUDO | | | |
| | EV5 | Δ GE5 | 0.2 | 1 | 1.8 | | →SPCOP-S | PCON | | |
| | EV6 | ∆ GE6 | 0.2 | 1 | 1.8 | | →EARO | | | |
| | EV7 | Δ GE7 | 0.2 | 1 | 1.8 | | →AUDO | | | |

| Parameter | Symbol | Min. | Тур. | Max. | Unit | Conditions | | | |
|------------------------------|-------------------|------|------|-------|------|-------------------------|---------------------|--|--|
| (Mic amplifier) | | | | | | | | | |
| Closed-loop gain | Gсмс | 0 | _ | 40 | dB | →MICO | MIC AMP | | |
| ⟨Reception driver⟩ | | | | | | | | | |
| Closed lean main | G CAM4 | 0 | _ | 40 | dB | →SPPO | AMP4 | | |
| Closed-loop gain | G _{CAM5} | 0 | _ | 40 | ав | →ERPO | AMP5 | | |
| Voltage gain | GVRA | -1.5 | 0 | 1.5 | dB | →EXTO | RAMP, RL=600 Ω | | |
| Output nower | Роја | 2 | 15 | _ | | →EARO | JAMP, RL=32Ω | | |
| Output power | POEA | 6.4 | 40 | _ | mW | →SPCOP-SPCON | EAMP2-EAMP1, RL=32Ω | | |
| Maximum output level | Vom | -2 | _ | _ | dBV | →EXTO | RAMP, RL=600Ω | | |
| ⟨Ringer drive⟩ | • | | | | | | 1 | | |
| Maximum output drive current | lo(max.) | 150 | _ | _ | mA | VSAT (RG5) <0.7 | V | | |
| Driven output voltage 1 | V ₀₁ | _ | _ | 0.7 | V | lo=150mA, RG5 | | | |
| Driven output voltage 2 | V _{O2} | _ | _ | 0.6 | V | lo=100mA, RG4 | | | |
| Driven output voltage 3 | Vos | _ | _ | 0.5 | V | lo=75mA, RG3 | | | |
| Driven output voltage 4 | V ₀₄ | _ | _ | 0.4 | V | Io=50mA, RG2 | | | |
| Driven output voltage 5 | V _{O5} | _ | _ | 0.3 | V | Io=30mA, RG1 | | | |
| OFF leak current | l _L | _ | 0.1 | 3 | μΑ | Vo=3V, RG1~RG5=OFF | | | |
| ⟨PLL block⟩ | • | - | | | | | | | |
| PLL lead-in time | T _{PL} | _ | 5 | (100) | ms | Guaranteed design value | | | |

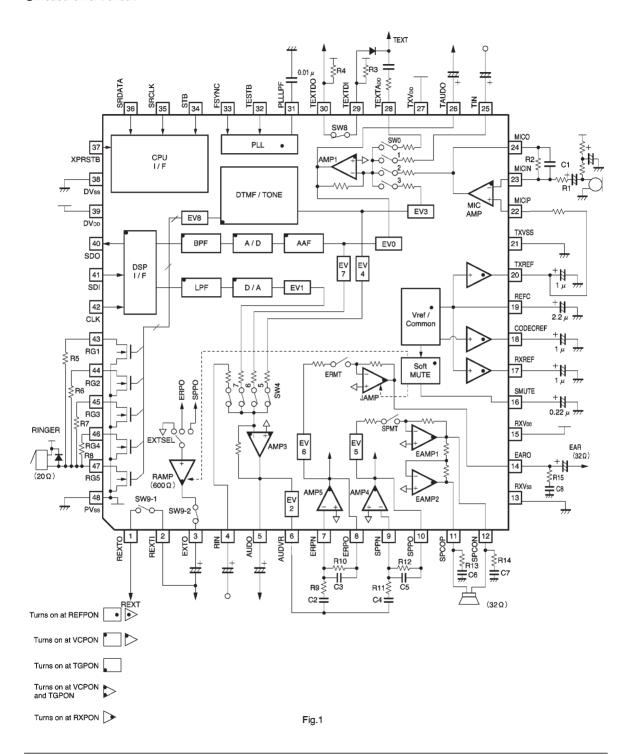


●Digital AC characteristics

| Parameter | | Symbol | Min. | Тур. | Max. | Unit |
|-----------------------------------|-------------------------|---------------|-------|-------|-------|------|
| ⟨Serial data interface / timing⟩ | | | | | | |
| Data clock frequency | μ/A-LAW | fcLKU | 64 | _ | 2048 | kHz |
| Data clock frequency | Linear | fcLKL | 128 | _ | 2048 | kHz |
| Frame sync signal frequency | | fsync | 7.996 | 8.000 | 8.004 | kHz |
| | | Tsr | 100 | _ | _ | ns |
| Communication sync signal timing | 1 | Tss | 100 | _ | _ | ns |
| | | Тѕн | 100 | _ | _ | ns |
| Digital input rise time | TIR | _ | _ | 20 | ns | |
| Digital input fall time | Digital input fall time | | | | 20 | ns |
| SDI setup time | | Trs | 100 | _ | _ | ns |
| SDI hold time | | Твн | 100 | _ | _ | ns |
| ⟨Register write timing⟩ | | | | | | |
| SRCLK frequency | | fclk | _ | _ | 3 | MHz |
| SRDATA input setup time | | tsuda | 100 | _ | _ | ns |
| SRDATA input hold time | | t htda | 100 | _ | _ | ns |
| Input setup time (SRCLK high vs. | Tsud | 333 | _ | _ | ns | |
| Input hold time (SRCLK high vs. S | fhtd | 1000 | _ | _ | ns | |
| STB strobe pulse width | | fpwd | 667 | _ | _ | ns |

Communication ICs

Measurement circuit



●External dimensions (Units: mm)

