

Quad 2-input AND gate

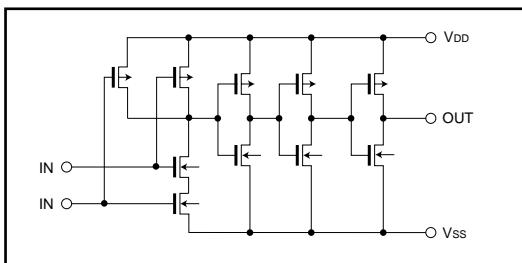
BU4081B / BU4081BF / BU4081BFV

The BU4081B, BU4081BF, and BU4081BFV are dual-input positive-logic AND gates with four circuits mounted on a single chip. An inverter-type buffer is added to the gate output, improving input / output transmission speed, and an increased load capacitance suppresses fluctuation in transmission time to a minimum.

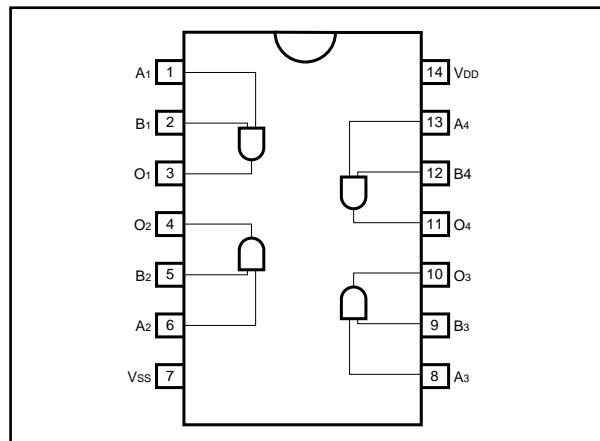
●Features

- 1) Low power dissipation.
- 2) Wide range of operating power supply voltages.
- 3) High input impedance.
- 4) High fan-out.
- 5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Logic circuit diagram



●Block diagram



● Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Limits		Unit
Power supply voltage	V _{DD}	−0.3 ~ +18		V
Power dissipation	P _d	1000 (DIP), 450 (SOP), 350 (SSOP)		mW
Operating temperature	T _{opr}	−40 ~ +85		°C
Storage temperature	T _{stg}	−55 ~ +150		°C
Input voltage	V _{IN}	−0.3 ~ V _{DD} + 0.3		V
I/O pin current	I _{l/o}	± 10		mA

● Electrical characteristics (unless otherwise noted, V_{SS} = 0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions	Measurement circuit
Input high level voltage	V _{IH}	3.5	—	—	V	5	—	Fig.1
		7.0	—	—		10		
		11.0	—	—		15		
Input low level voltage	V _{IL}	—	—	1.5	V	5	—	Fig.1
		—	—	3.0		10		
		—	—	4.0		15		
Input high level current	I _{IH}	—	—	0.3	μA	15	V _{IH} = 15V	Fig.1
Input low level current	I _{IL}	—	—	−0.3	μA	15	V _{IL} = 0V	Fig.1
Output high level voltage	V _{OH}	4.95	—	—	V	5	I _O = 0mA	Fig.1
		9.95	—	—		10		
		14.95	—	—		15		
Output low level voltage	V _{OL}	—	—	0.05	V	5	I _O = 0mA	Fig.1
		—	—	0.05		10		
		—	—	0.05		15		
Output high level current	I _{OH}	−0.16	—	—	mA	5	V _{OH} = 4.6V	Fig.1
		−0.4	—	—		10	V _{OH} = 9.5V	
		−1.2	—	—		15	V _{OH} = 13.5V	
Output low level current	I _{OL}	0.44	—	—	mA	5	V _{OL} = 0.4V	Fig.1
		1.1	—	—		10	V _{OL} = 0.5V	
		3.0	—	—		15	V _{OL} = 1.5V	
Static current dissipation	I _{DD}	—	—	1	μA	5	V _I = V _{DD} or GND	—
		—	—	2		10		
		—	—	4		15		

Switching characteristics (unless otherwise noted, $V_{SS} = 0V$, $T_a = 25^\circ C$, $C_L = 50pF$)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V _{DD} (V)	Conditions	Measurement circuit
Output rise time	t_{TLH}	—	180	—	ns	5	—	Fig.2
		—	90	—		10		
		—	65	—		15		
Output fall time	t_{THL}	—	100	—	ns	5	—	Fig.2
		—	50	—		10		
		—	40	—		15		
“L” to “H” Propagation delay time	t_{PLH}	—	160	—	ns	5	—	Fig.2
		—	65	—		10		
		—	50	—		15		
“H” to “L” Propagation delay time	t_{PHL}	—	160	—	ns	5	—	Fig.2
		—	65	—		10		
		—	50	—		15		
Input capacitance	C_{IN}	—	5	—	pF	—	—	—

● Measurement circuits

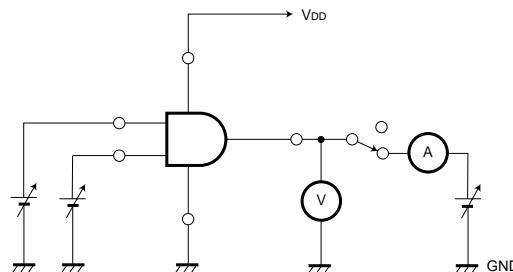


Fig. 1 DC characteristics

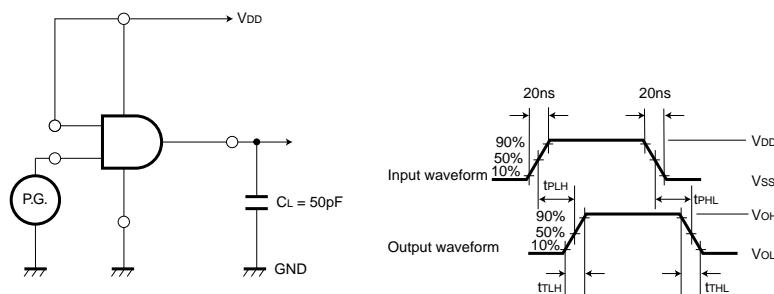


Fig. 2 Switching characteristics

● Electrical characteristic curve

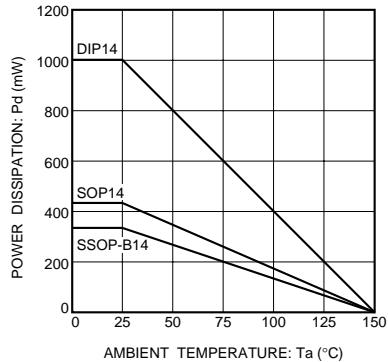


Fig. 3 Power dissipation vs. Ta

● External dimensions (Units: mm)

