Input selector for high resolution displays

BH7659S

The BH7659S is an input signal switching IC developed for high resolution displays that has three fc = 250MHz wide-band video switching circuits for RGB video signal switching and four CMOS analog switching circuits for switching between H_D and V_D signals as well as I^2C bus signals (SDA and SCL).

●Applications

High-resolution displays and high-definition TVs

●Features

1) Operates with a 5V power supply voltage.
2) Built-in, wide-band switching circuit for RGB switching (fc = 250MHz).
3) SDA and SCL as well as H_D and V_D signal switching is possible.
4) Built-in power save function.

●Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	8.0	V
Power dissipation	Pd	1300*	mW
Operating temperature	Topr	– 25 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

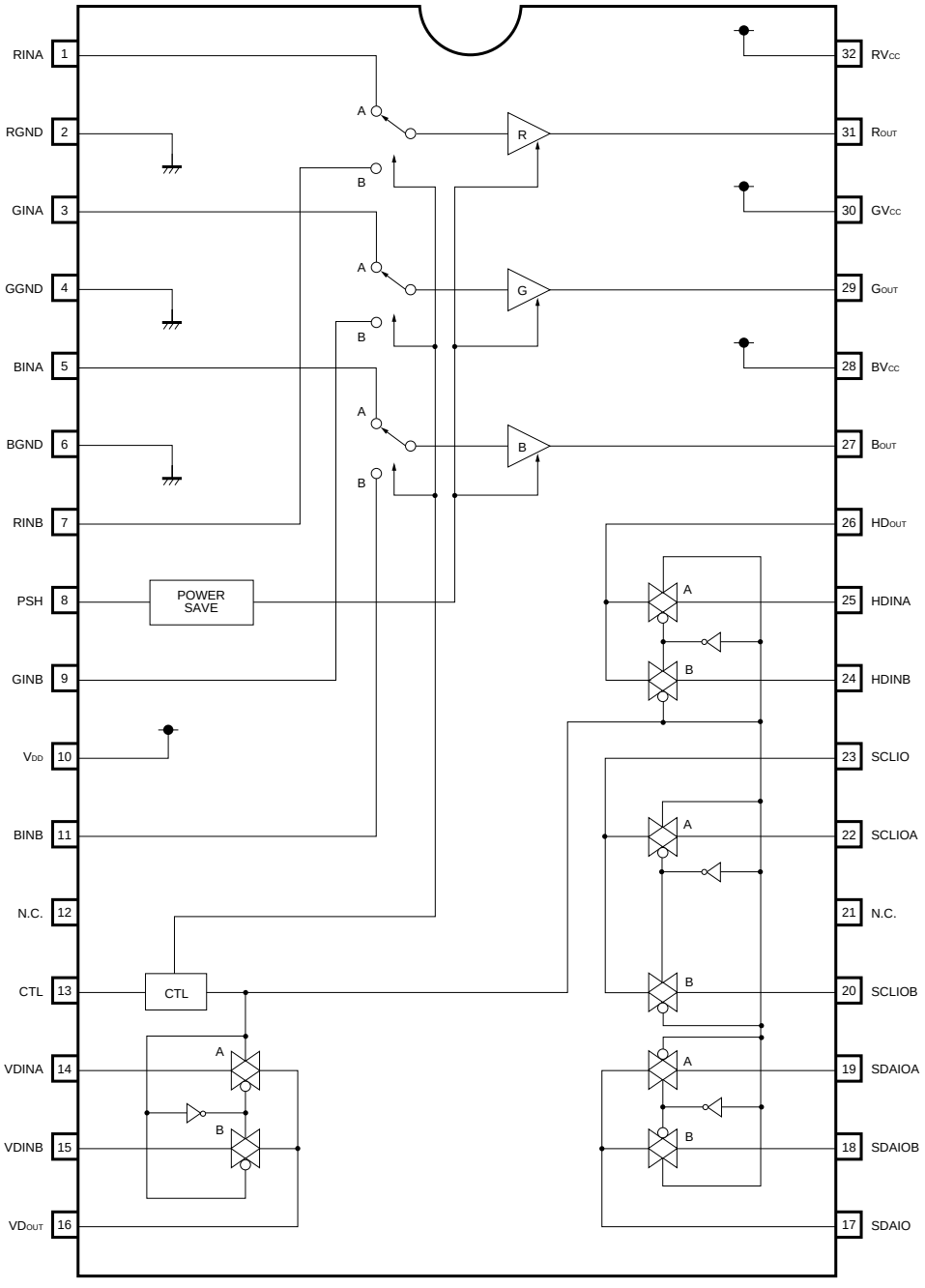
* Reduced by 13mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

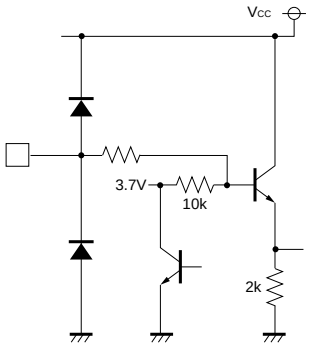
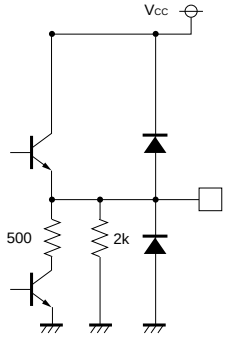
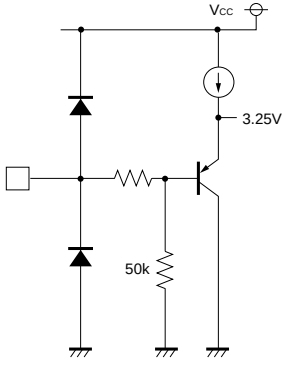
Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{CC}	4.5	5.0	5.5	V

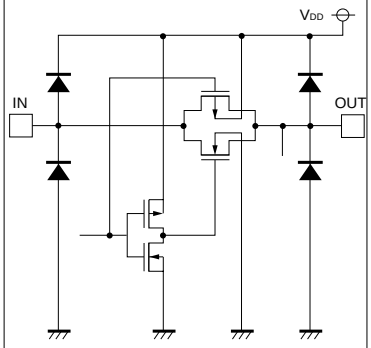
○Not designed for radiation resistance.

●Block diagram



●Input / output equivalent circuits

Pin No.	Pin description (pin name)	Reference potential	Input / output circuit	Function
1 3 5 7 9 11	Red signal input A (RINA) Green signal input A (GINA) Blue signal input A (BINA) Red signal input B (RINB) Green signal input B (GINB) Blue signal input B (BINB)	3.5V when selected 0V when not selected8		Switches between the two RGB signaling systems. Input B is selected by setting the CTL pin to high and input A to low.
27 29 31	Blue signal output (BOUT) Green signal output (GOUT) Red signal output (ROUT)	1.85V		Power save activates by setting the PSH pin to high.
8 9	Power save input (PSH) Control input (CTL)	0V		PSH Power save off ≦ 1.5V Power save on ≧ 3.5V CTL Input A ≧ 3.5V Input B ≦ 1.5V

Pin No.	Pin description (pin name)	Reference potential	Input / output circuit	Function
14 15 16 17 18 19 20 22 24 25 26 27	VD signal input A (VDINA) VD signal input B (VDINB) VD signal output (VDOUT) SDA signal I / O (SDAIO) SDA signal I / O B (SDAIOB) SDA signal I / O A (SDAIOA) SCL signal I / O B (SCLIOB) SCL signal I / O A (SCLIOA) SCL signal I / O (SCLIO) HD signal input B (HDINB) HD signal input A (HDINA) HD signal output (HDOUT)	0V		Switches between the two VD, HD, SDA, and SCL signaling systems. Input B is selected by setting the CTL pin to high and input A to low. Bi-directional I / O is possible with CMOS analog switch
2	Red ground (RGND)	0V	—	Red video SW block GND
4	Green ground (GGND)	0V	—	Green video SW block GND
6	Blue ground (BGND)	0V	—	Blue video SW block and CMOS SW block GND
10	CMOS power supply voltage (V_{DD})	5V	—	CMOS SW block V_{DD}
28	Blue power supply voltage (BV_{CC})	5V	—	Blue video SW block V_{CC}
30	Green power supply voltage (GV_{CC})	5V	—	Green video SW block V_{CC}
32	Red power supply voltage (RV_{CC})	5V	—	Red video SW block V_{CC}

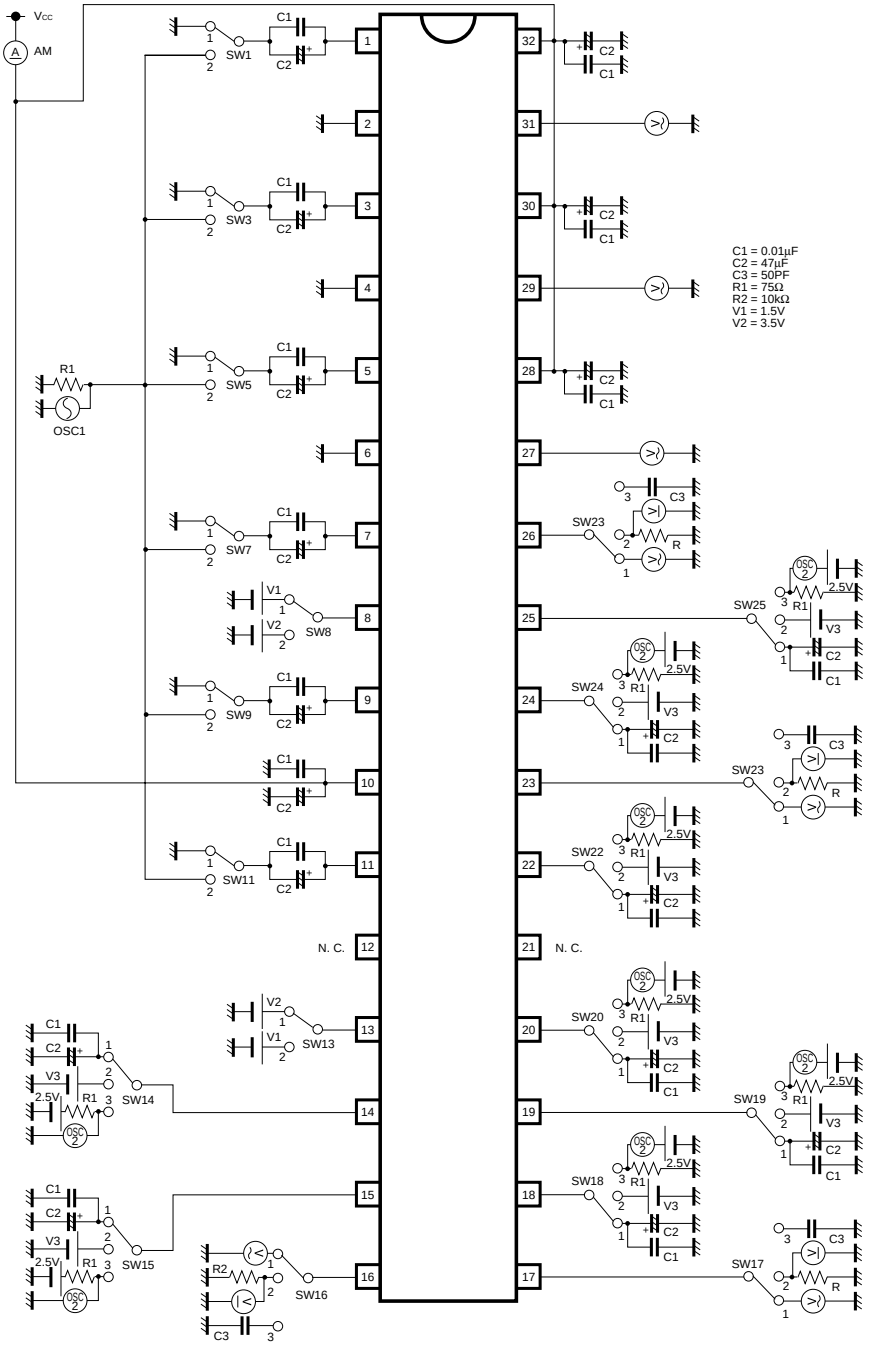
●Electrical characteristics (unless otherwise noted, V_{CC} = 5.0V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
⟨Overall device⟩						
Circuit current	I_{CC}	15	25	35	mA	—
Circuit current during power save	I_{PSV}	7	14	22	mA	PS = "H"
⟨R, G, and B video switches⟩						
Voltage gain	G_V	– 1.0	– 0.5	0	dB	f = 10MHz
Interchannel relative gain	ΔG_{VC}	– 0.5	0	0.5	dB	f = 10MHz
Interblock relative gain	ΔG_{VB}	– 0.5	0	0.5	dB	f = 10MHz
Output dynamic range	V_{OM}	2.6	—	—	V_{P-P}	f = 1kHz
⟨CMOS analog switch⟩						
On-resistance	R_{ON}	—	200	400	Ω	V_{IN} = 2.5V
Interchannel on-resistance difference	ΔR_{ON}	—	20	40	Ω	V_{IN} = 2.5V
Interchannel crosstalk	CT	—	– 70	– 55	dB	f = 150kHz
Transmission delay time	t_D	—	20	—	ns	RL = 10Ω, CL = 50pF
⟨Control block⟩						
High level voltage	V_H	3.5	—	—	V	—
Low level voltage	V_L	—	—	1.5	V	—

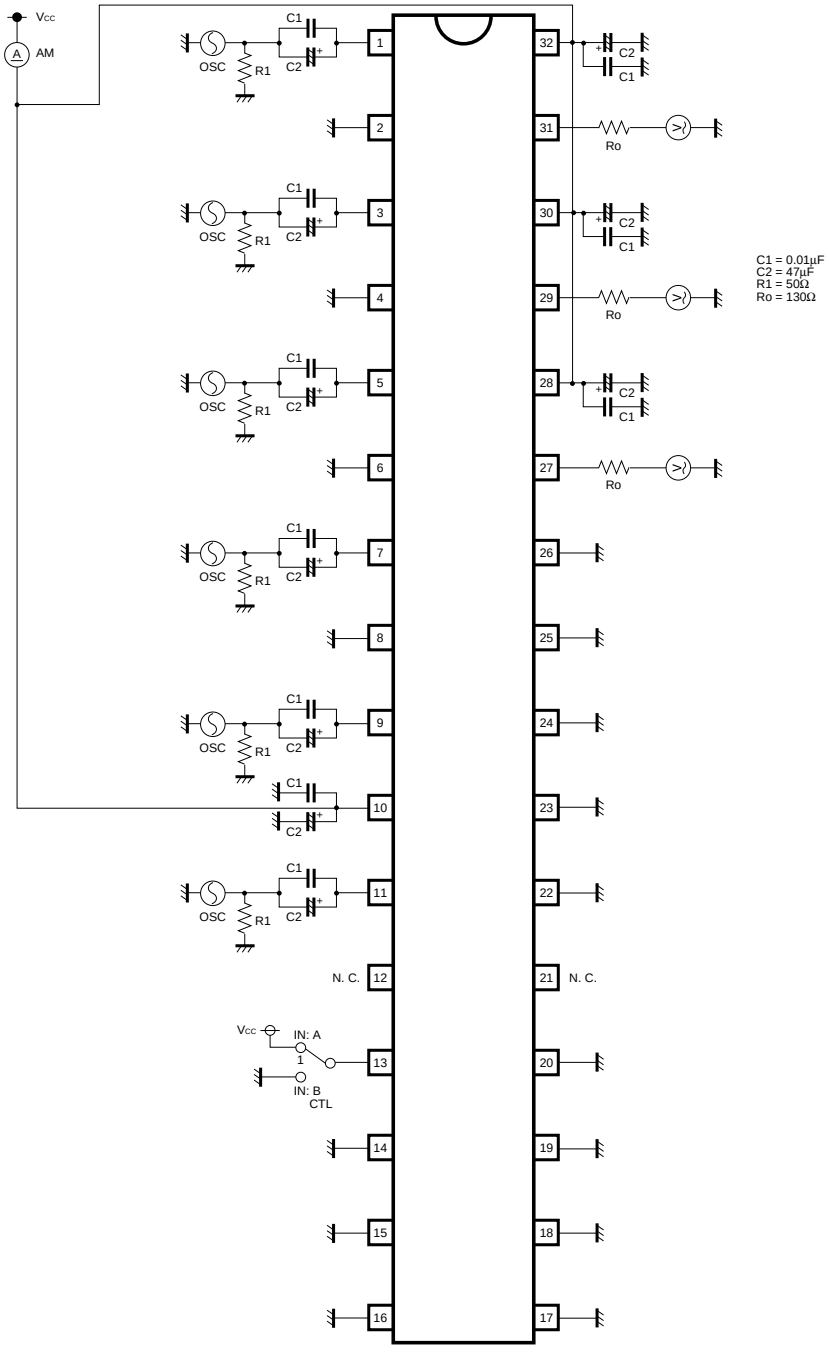
●Guaranteed design parameters (unless otherwise noted, V_{CC} = 5V, Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
⟨R, G, and B video switches⟩						
Frequency characteristics 1	f_1	– 3.0	0	+ 1.0	dB	f = 50MHz
Frequency characteristics 2	f_2	– 6.0	– 3	– 1.0	dB	f = 250MHz
Interchannel relative frequency characteristics	Δf_C	– 0.5	0	0.5	dB	f = 50MHz
Interblock relative frequency characteristics	Δf_B	– 0.5	0	0.5	dB	f = 50MHz
Interchannel crosstalk 1	CT_{C1}	—	– 50	– 35	dB	f = 50MHz
Interchannel crosstalk 2	CT_{C2}	—	– 30	– 15	dB	f = 250MHz
Interblock crosstalk 1	CT_{B1}	—	– 50	– 35	dB	f = 50MHz
Interblock crosstalk 2	CT_{B2}	—	– 30	– 15	dB	f = 250MHz

●Measurement circuit 1



●Measurement circuit 2



●Measurement conditions

〈Overall device〉 measurement circuit 1

Parameter	Switch conditions		Notes
	8	Others	
Circuit current	1	1	(1)
Circuit during power save	2	1	(2)

〈R, G, and B video switches〉 measurement circuit 2

Parameter		Input pin: (OSC)						Switch conditions	Notes
		1	7	3	9	5	11	CTL	
Voltage gain (G_V)	RinA	○	—	—	—	—	—	IN: A	(3)
Output dynamic range	RinB	—	○	—	—	—	—	IN: B	(6)
(V_{OM})	GinA	—	—	○	—	—	—	IN: A	
Frequency characteristics 1 (f_1)	GinB	—	—	—	○	—	—	IN: B	(7)
	BinA	—	—	—	—	○	—	IN: A	
Frequency characteristics 2 (f_2)	BinB	—	—	—	—	—	○	IN: B	(8)
Interchannel	RinA→B	○	—	—	—	—	—	IN: B	(11)
crosstalk 1	RinB→A	—	○	—	—	—	—	IN: A	
(CT_{C1})	GinA→B	—	—	○	—	—	—	IN: B	
Interchannel	GinB→A	—	—	—	○	—	—	IN: A	(12)
crosstalk 2	BinA→B	—	—	—	—	○	—	IN: B	
(CT_{C2})	BinB→A	—	—	—	—	—	○	IN: A	
Interblock	G→RinA	—	—	○	—	—	—	IN: A	(13)
crosstalk 1	B→RinA	—	—	—	—	○	—	IN: A	
(CT_{B1})	R→GinA	○	—	—	—	—	—	IN: A	
Interblock	B→GinA	—	—	—	—	○	—	IN: A	(14)
crosstalk 2	R→BinA	○	—	—	—	—	—	IN: A	
(CT_{B2})	G→BinA	—	—	○	—	—	—	IN: A	
Interchannel relative gain: ΔG_{VC}									(4)
Interblock relative gain: ΔG_{VB}									(5)
Interchannel relative frequency characteristics: Δf_C									(9)
Interblock relative frequency characteristics: Δf_B									(10)

〈C-ROM analog switch〉 measurement circuit 1

Parameter		Switch conditions														Notes
		13	14	15	16	17	18	19	20	22	23	24	25	26	others	
On-resistance	VDinA	1	2	1	2	1	1	1	1	1	1	1	1	1	1	(15)
(R_{ON})	VDinB	2	1	2	2	1	1	1	1	1	1	1	1	1	1	
	SDinA	1	1	1	1	2	1	2	1	1	1	1	1	1	1	
	SDinB	2	1	1	1	2	2	1	1	1	1	1	1	1	1	
	SCinA	1	1	1	1	1	1	1	1	2	2	1	1	1	1	
	SCinB	2	1	1	1	1	1	1	2	1	2	1	1	1	1	
	HDinA	1	1	1	1	1	1	1	1	1	1	1	2	2	1	
	HDinB	2	1	1	1	1	1	1	1	1	1	2	1	2	1	
Interchannel	VDinA→B	1	3	1	1	1	1	1	1	1	1	1	1	1	1	(17)
crosstalk	VDinB→A	2	1	3	1	1	1	1	1	1	1	1	1	1	1	
(CT)	SDinA→B	1	1	1	1	1	1	3	1	1	1	1	1	1	1	
	SDinB→A	2	1	1	1	1	3	1	1	1	1	1	1	1	1	
	SCinA→B	1	1	1	1	1	1	1	1	3	1	1	1	1	1	
	SCinB→A	2	1	1	1	1	1	1	3	1	1	1	1	1	1	
	HDinA→B	1	1	1	1	1	1	1	1	1	1	1	3	1	1	
	HDinB→A	2	1	1	1	1	1	1	1	1	1	3	1	1	1	
Transmission delay	VDinA	1	3	1	3	1	1	1	1	1	1	1	1	1	1	(18)
time (t_D)	VDinB	2	1	3	3	1	1	1	1	1	1	1	1	1	1	
	SDinA	1	1	1	1	3	1	3	1	1	1	1	1	1	1	
	SDinB	2	1	1	1	3	3	1	1	1	1	1	1	1	1	
	SCinA	1	1	1	1	1	1	1	1	3	3	1	1	1	1	
	SCinB	2	1	1	1	1	1	1	3	1	3	1	1	1	1	
	HDinA	1	1	1	1	1	1	1	1	1	1	1	3	3	1	
	HDinB	2	1	1	1	1	1	1	1	1	1	3	1	3	1	
Interchannel on-resistance difference (ΔR_{ON})																(16)

Notes:

(1) Circuit current: I_{CC}; measurement of the circuit current.

(2) Circuit current during power save: I_{PSV}; measurement of the circuit current during power save.

(3) Voltage gain: G_V

V_{IN} = 1.0V_{P-P}, f = 10MHz sine wave input from the OSC

G_V = 20log (V_{OUT} / V_{IN}) [dB]

(4) Interchannel relative gain: ΔG_{VC}

ΔG_{VC} = G_VRa – G_VRb, G_VGa – G_VGb, G_VBa – G_VBb [dB]

(5) Interblock relative gain: ΔG_{VB}

ΔG_{VB}R = G_VRa – G_VGa, G_VRa – G_VGb, G_VRa – G_VBa, G_VRa – G_VBb [dB]

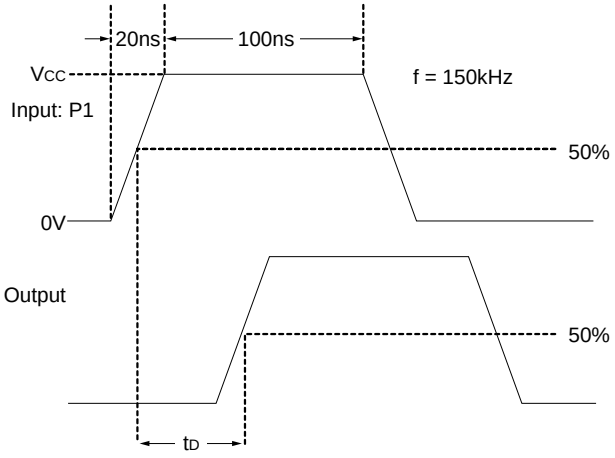
ΔG_{VB}G = G_VGa – G_VRa, G_VGa – G_VRb, G_VGa – G_VBa, G_VGa – G_VBb [dB]

ΔG_{VB}B = G_VBa – G_VRa, G_VBa – G_VRb, G_VBa – G_VGa, G_VBa – G_VBb [dB]

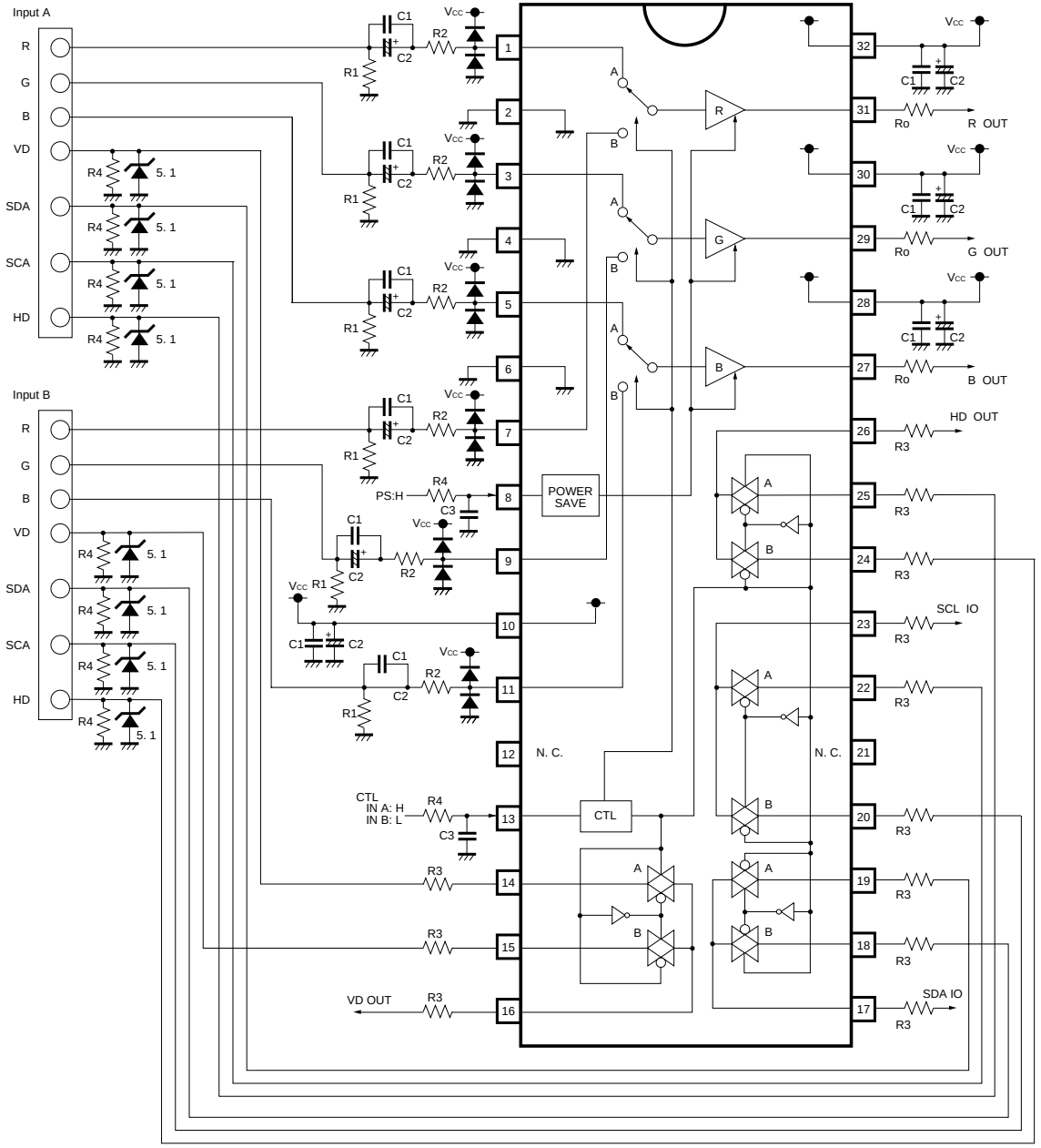
(6) Output dynamic range: V_{OM}

Connect a distortion meter to the output. After adding a f = 1kHz sine wave input from the OSC, adjust the input level so that the output distortion is 1.0%. The output voltage at that time is V_{OM} [V_{P-P}].

(7) Frequency characteristics 1: f1
Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 10MHz and 50MHz sine wave input from the OSC.
f1 = G_V (50MHz) – G_V (10MHz) [dB]
(8) Frequency characteristics 2: f2
Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 10MHz and 250MHz sine wave input from the OSC.
f2 = G_V (250MHz) – G_V (10MHz) [dB]
(9) Interchannel relative frequency characteristics: Δfc
Δfc = f1 (INA) – f1 (INB) [dB]
(10) Interblock relative frequency characteristics: Δfb
Δfb = f1 (RINA) – f1 (GINA), f1 (GINA) – f1 (BINA), f1 (BINA) – f1 (RINA) [dB]
= f1 (RINB) – f1 (GINB), f1 (GINB) – f1 (BINB), f1 (BINB) – f1 (RINB) [dB]
(11) Interchannel crosstalk 1: CT_{C1}
Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 50MHz sine wave input from the OSC.
CT_{C1} = 20log (V_{OUT} / V_{IN}) [dB]
(12) Interchannel crosstalk 2: CT_{C2}
Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 250MHz sine wave input from the OSC.
CT_{C2} = 20log (V_{OUT} / V_{IN}) [dB]
(13) Interblock crosstalk 1: CT_{B1}
Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 50MHz sine wave input from the OSC.
CT_{B1} = 20log (V_{OUT} / V_{IN}) [dB]
(14) Interblock crosstalk 2: CT_{B2}
Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 250MHz sine wave input from the OSC.
CT_{B2} = 20log (V_{OUT} / V_{IN}) [dB]
(15) On-resistance: R_{ON}
$\Delta R_{ON} = (V_{OUT} / V_{IN} - 1) \times 10^4$ [Ω]
(16) Interchannel on-resistance difference: ΔR_{ON}
$\Delta R_{ON} = R_{ON}$ (INA) – R_{ON} (INB)
(17) Interchannel crosstalk: CT
Apply to the input pin a V_{IN} = 1.0V_{P-P}, f = 150MHz sine wave input from the OSC2.
CT = 20log (V_{OUT} / V_{IN}) [dB]
(18) Transmission delay time: t_D
Apply to the input pin the rectangular wave of P1 from the OSC2.



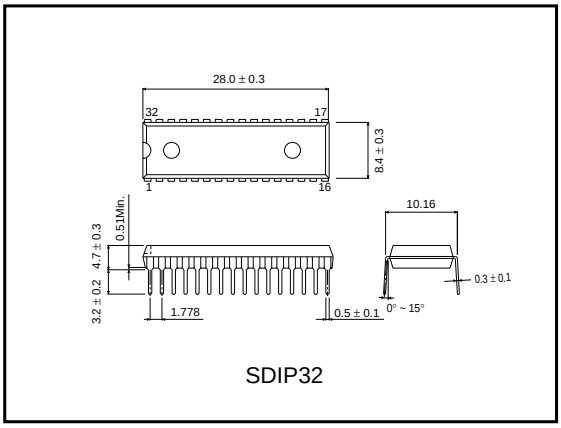
●Application example



Note: The Ro value differs depending on the load capacitance.
Set so that the frequency characteristics are flat.

R1 = 75Ω C1 = 0.01µF
R2 = 47Ω C2 = 47µF
R3 = 100Ω C3 = 0.1µF
R4 = 1.2kΩ

●External dimensions (Units: mm)



SDIP32