Dual-line serial control sound processor IC

BH3866AS

The BH3866AS is a signal processing IC developed for the control of volume and tone quality in TV equipment. Since dual-line serial control (I^2C BUS) is used, the volume level and tone quality in TV equipment can be changed using signals such as those from a microcomputer or similar device.

●Applications

DVDs, personal computers, high-vision TVs, karaoke sets, digital broadcasts, CATVs, and other TV equipment

●Features

1) 3-channel volume and sound quality control (for stereo and center speakers).
2) Absorption of volume deviation between input sources and improved S / N ratio, for better sound quality, using an AGC circuit.
3) Control through I^2C BUS serial control.
4) Internal pseudo-stereo circuit provides phase-shift matrix surround effect.

●Absolute maximum ratings (Ta = 25°C)

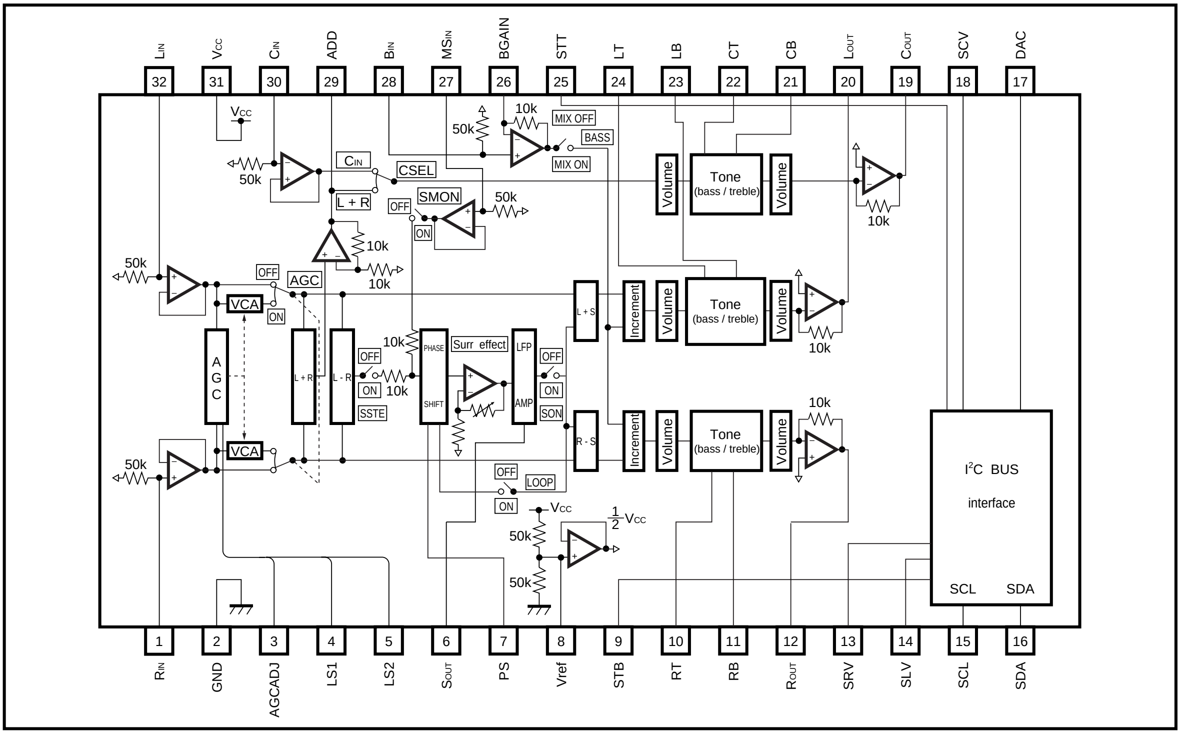
Parameter	Symbol	Limits	Unit
Power supply voltage	V_{CC}	10.0	V
Power dissipation	Pd	1250*	mW
Operating temperature	Topr	– 25 ~ + 75	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

* Reduced by 12.5mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	7.0	—	9.5	V

●Block diagram

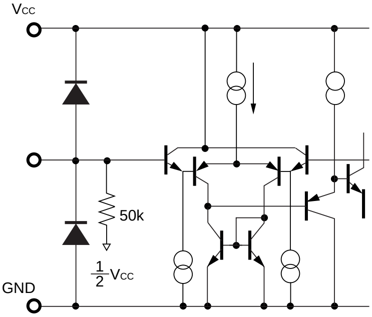
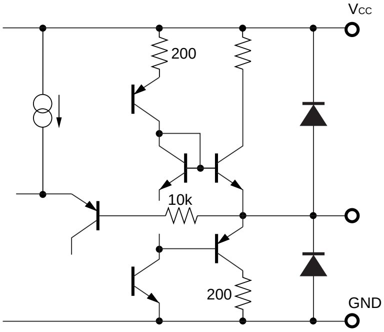
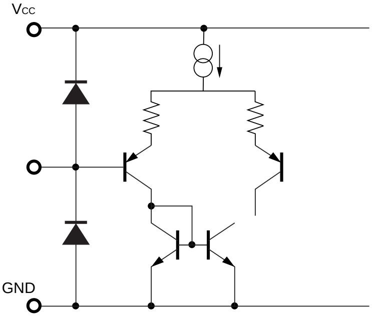
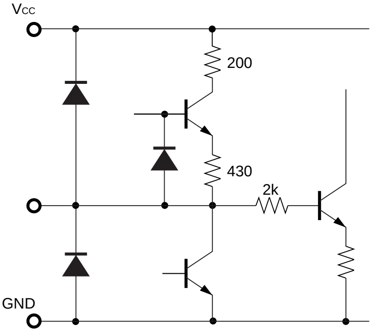


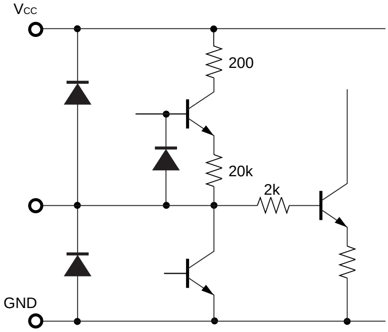
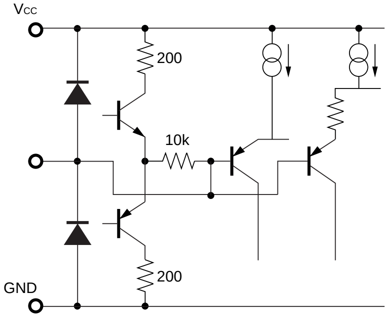
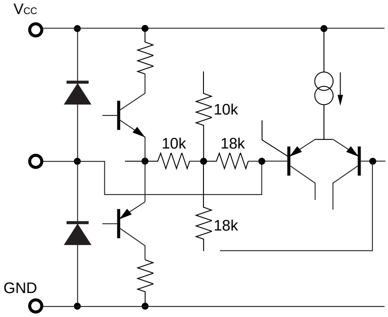
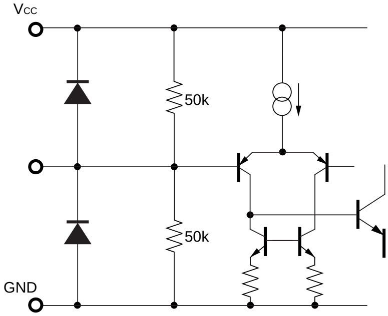
●Pin descriptions

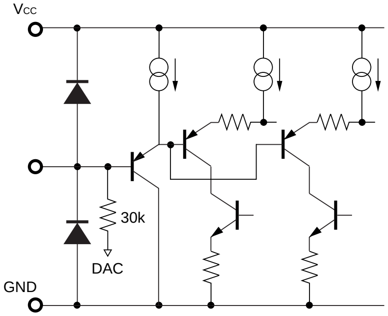
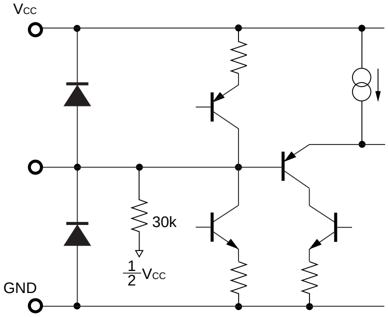
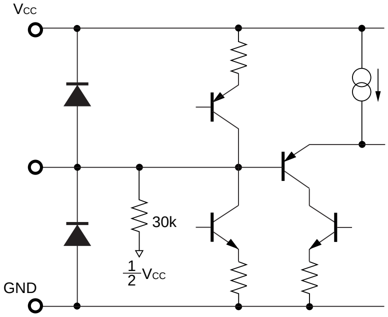
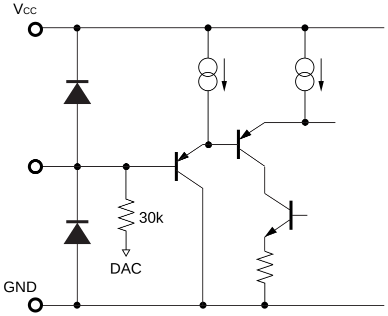
Pin No.	Pin name	Function
1	R_{IN}	Rch input
2	GND	Ground
3	AGCADJ	AGC 0dB adjustment
4	LS1	AGC level sensor 1
5	LS2	AGC level sensor 2
6	S_{OUT}	Sch output pin and LPF
7	PS	Phase shift pin (internal resistance: 18kΩ)
8	Vref	1 / 2 V_{CC}
9	STB	Bass shock sound integration
10	RT	Rch Treble fc setting
11	RB	Rch Bass fc setting
12	R_{OUT}	Rch output
13	SRV	Vol Rch shock sound integration
14	SLV	Vol Lch shock sound integration
15	SCL	I^{2}C communications clock
16	SDA	I^{2}C communications data

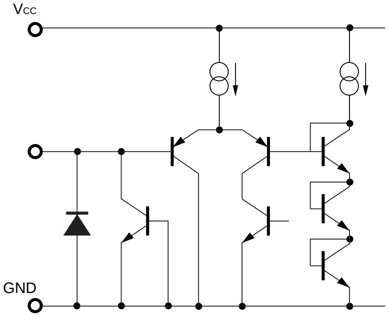
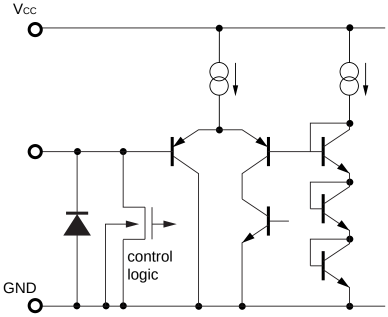
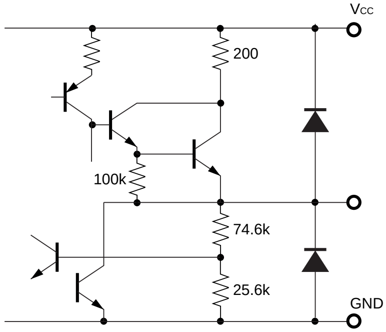
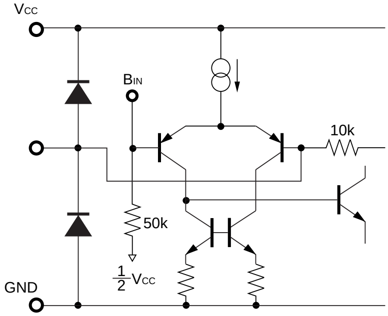
Pin No.	Pin name	Function
17	DAC	Expansion DAC (L / H)
18	SCV	Vol Cch shock sound integration
19	C_{OUT}	Cch output
20	L_{OUT}	Lch output
21	CB	Cch Bass fc setting
22	CT	Cch Treble fc setting
23	LB	Lch Bass fc setting
24	LT	Lch Treble fc setting
25	STT	Treble shock sound integration
26	BGAIN	Bass Mix Gain adjustment
27	MS_{IN}	Mono Sur input
28	B_{IN}	Bass detection LPF operating amplifier input
29	ADD	L + R added output after AGC
30	C_{IN}	Cch input
31	V_{CC}	Power supply, 9V
32	L_{IN}	Lch input

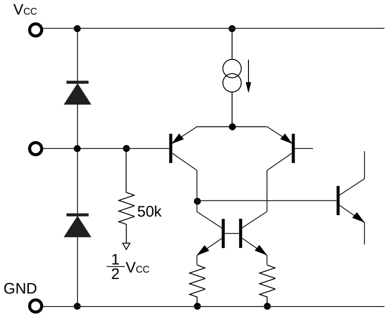
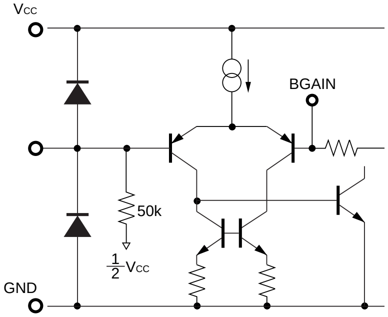
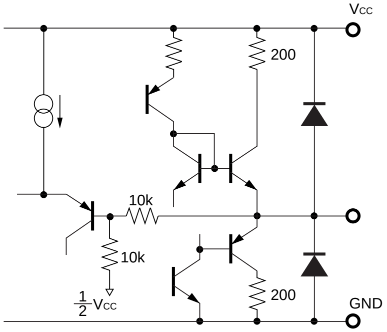
●Input / output circuits

Pin No.	Pin name	Pin voltage	Zin	I / O	Equivalent circuit	Function
1 30 32	RIN CIN LIN	4.5V	50k	I		Input pins.
12 19 20	ROUT COUT LOUT	4.5V	—	O		Output pins.
3	AGCADJ	—	—	I		AGC 0dB adjustment pin. This pin is connected to the base of PNP. The current output from this pin is 1µA (Typ.) Max.
4	LS1	—	—	—		Time constant pin on the side that suppresses the AGC signal level.

Pin No.	Pin name	Pin voltage	Zin	I / O	Equivalent circuit	Function
5	LS2	—	—	—		Time constant pin on the side that amplifies the AGC signal level.
6	SOUT	4.5V	10k	O		Serves as both the output pin for the surround and pseudo-stereo effects, and the LPF pin.
7	PS	—	—	—		For the phase-shifter filter for the surround and pseudo-stereo effects.
8	Vref	4.5V	—	—		1 / 2 VCC. This voltage serves as the power supply for the signal system.

Pin No.	Pin name	Pin voltage	Zin	I / O	Equivalent circuit	Function
9 25	STB STT	—	30k	—		Integration pins that prevent shock sound when switching the bass and treble levels.
10 22 24	RT CT LT	4.5V	30k	—		Treble filter pins for the left, right, and center channels.
11 21 23	RB CB LB	4.5V	30k	—		Bass filter pins for the left, right, and center channels.
13 14 18	SRV SLV SCV	—	30k	—		Integration pins that prevent shock sound when switching the volume levels on the left, right, and center channels.

Pin No.	Pin name	Pin voltage	Zin	I / O	Equivalent circuit	Function
15	SCL	—	—	I		SCL pin for the I^{2}C BUS. This is the clock pin.
16	SDA	—	—	I		SDA pin for the I^{2}C BUS. The Acknowledge signal is output from this pin. This is the data pin.
17	DAC	0 / 5	—	O		0V and 5V output pin that enables control with the I^{2}C BUS.
26	BGAIN	4.5V	—	—		Gain adjustment pin used to mix the bass on the left and right channels.

Pin No.	Pin name	Pin voltage	Zin	I / O	Equivalent circuit	Function
27	$\mathrm{MS_{IN}}$	4.5V	50k	I		Surround input section for monaural signals in the surround section.
28	$\mathrm{B_{IN}}$	4.5V	50k	I		Bass signal input to the left and right channels.
29	ADD	4.5V	—	O		Incremented output from the left and right channels following AGC.
31	$\mathrm{V_{CC}}$	9V	—	—	—	Power supply pin.
2	GND	0V	—	—	—	Ground pin.

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{CC} = 9V, f = 1kHz, Rg = 600Ω, RL = 10kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent circuit current	I_Q	—	35	65	mA	V_{IN} = 0Vrms
Max. output voltage, Rch	V_{OMR}	2.1	2.5	—	Vrms	THD = 1%(Ⓒ)
Max. output voltage, Lch	V_{OML}	2.1	2.5	—	Vrms	THD = 1%(Ⓒ)
Max. output voltage, Cch	V_{OMC}	2.1	2.5	—	Vrms	THD = 1%(Ⓒ)
Voltage gain, Rch	G_{VR}	– 1.5	0	1.5	dB	V_{IN} = 1Vrms, G_{VR} = 20log (Ⓑ / V_{IN})
Voltage gain, Lch	G_{VL}	– 1.5	0	1.5	dB	V_{IN} = 1Vrms, G_{VL} = 20log (Ⓑ / V_{IN})
Voltage gain, Cch	G_{VC}	– 1.5	0	1.5	dB	V_{IN} = 1Vrms, G_{VC} = 20log (Ⓑ / V_{IN})
Total harmonic distortion, Rch	THD_R	—	0.01	0.1	%	V_{IN} = 1Vrms
Total harmonic distortion, Lch	THD_L	—	0.01	0.1	%	V_{IN} = 1Vrms
Total harmonic distortion, Cch	THD_C	—	0.1	0.3	%	V_{IN} = 1Vrms
Output noise voltage, Rch	V_{NOR}	—	35	70	µVrms	Rg = 0Ω, DIN AUDIO
Output noise voltage, Lch	V_{NOL}	—	35	70	µVrms	Rg = 0Ω, DIN AUDIO
Output noise voltage, Cch	V_{NOC}	—	35	70	µVrms	Rg = 0Ω, DIN AUDIO
Residual noise voltage, Rch	V_{MNOR}	—	3	10	µVrms	Rg = 0Ω, DIN AUDIO
Residual noise voltage, Lch	V_{MNOL}	—	3	10	µVrms	Rg = 0Ω, DIN AUDIO
Residual noise voltage, Cch	V_{MNOC}	—	3	10	µVrms	Rg = 0Ω, DIN AUDIO
Crosstalk, Rch→Lch	$CT_{R\text{-}L}$	70	78	—	dB	V_{IN} = 1Vrms, $CT_{R\text{-}L}$ = 20log (Ⓑ_R / Ⓑ_L)
Crosstalk, Rch→Cch	$CT_{R\text{-}C}$	70	78	—	dB	V_{IN} = 1Vrms, $CT_{R\text{-}C}$ = 20log (Ⓑ_R / Ⓑ_C)
Crosstalk, Lch→Rch	$CT_{L\text{-}R}$	70	78	—	dB	V_{IN} = 1Vrms, $CT_{L\text{-}R}$ = 20log (Ⓑ_L / Ⓑ_R)
Crosstalk, Lch→Cch	$CT_{L\text{-}C}$	66	71	—	dB	V_{IN} = 1Vrms, $CT_{L\text{-}C}$ = 20log (Ⓑ_L / Ⓑ_C)
Crosstalk, Cch→Rch	$CT_{C\text{-}R}$	70	78	—	dB	V_{IN} = 1Vrms, $CT_{C\text{-}R}$ = 20log (Ⓑ_C / Ⓑ_R)
Crosstalk, Cch→Lch	$CT_{C\text{-}L}$	70	78	—	dB	V_{IN} = 1Vrms, $CT_{C\text{-}L}$ = 20log (Ⓑ_C / Ⓑ_L)
Input impedance, Rch	R_{INR}	35	50	65	kΩ	f_{INR} = 1kHz, V_{IN} = 1Vrms, $R_{INR} = \frac{50k \times \text{Ⓐ}}{(1 - \text{Ⓐ})}$
Input impedance, Lch	R_{INL}	35	50	65	kΩ	f_{INL} = 1kHz, V_{IN} = 1Vrms, $R_{INR} = \frac{50k \times \text{Ⓐ}}{(1 - \text{Ⓐ})}$
Input impedance, Cch	R_{INC}	35	50	65	kΩ	f_{INC} = 1kHz, V_{IN} = 1Vrms, $R_{INR} = \frac{50k \times \text{Ⓐ}}{(1 - \text{Ⓐ})}$
Output impedance, Rch	R_{OUTR}	—	—	50	Ω	f_{OUTR} = 1kHz, $R_{OUTR} = \frac{1k \times \text{Ⓓ}}{1 - \text{Ⓓ}}$
Output impedance, Lch	R_{OUTL}	—	—	50	Ω	f_{OUTL} = 1kHz, $R_{OUTL} = \frac{1k \times \text{Ⓓ}}{1 - \text{Ⓓ}}$
Output impedance, Cch	R_{OUTC}	—	—	50	Ω	f_{OUTC} = 1kHz, $R_{OUTC} = \frac{1k \times \text{Ⓓ}}{1 - \text{Ⓓ}}$
Ripple rejection, Rch	RR_R	40	53	—	dB	f_{RR} = 100Hz, V_{RR} = 100mVrms, $RR_R = 20\log\frac{V_{RR}}{\text{Ⓑ}}$
Ripple rejection, Lch	RR_L	40	53	—	dB	f_{RR} = 100Hz, V_{RR} = 100mVrms, $RR_R = 20\log\frac{V_{RR}}{\text{Ⓑ}}$
Ripple rejection, Cch	RR_C	40	53	—	dB	f_{RR} = 100Hz, V_{RR} = 100mVrms, $RR_R = 20\log\frac{V_{RR}}{\text{Ⓑ}}$
Muting level, Rch	V_{MUTER}	80	90	—	dB	V_{IN} = 1Vrms, $V_{MUTER} = 20\log\frac{V_{IN}}{\text{Ⓑ}}$
Muting level, Lch	V_{MUTEL}	80	90	—	dB	V_{IN} = 1Vrms, $V_{MUTEL} = 20\log\frac{V_{IN}}{\text{Ⓑ}}$
Muting level, Cch	V_{MUTEC}	80	90	—	dB	V_{IN} = 1Vrms, $V_{MUTEC} = 20\log\frac{V_{IN}}{\text{Ⓑ}}$

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Volume attenuation, Rch	ATT_{MAXR}	80	90	—	dB	V_{IN} = 1Vrms, $ATT_{MAXR} = 20\log \frac{V_{IN}}{\textcircled{B}}$
Volume attenuation, Lch	ATT_{MAXL}	80	90	—	dB	V_{IN} = 1Vrms, $ATT_{MAXL} = 20\log \frac{V_{IN}}{\textcircled{B}}$
Volume attenuation, Cch	ATT_{MAXC}	80	90	—	dB	V_{IN} = 1Vrms, $ATT_{MAXC} = 20\log \frac{V_{IN}}{\textcircled{B}}$
Channel balance 1, Rch→Lch	$CB_{1R\text{-}L}$	– 1.5	0	1.5	dB	V_{IN} = 1Vrms, $CB_{1R\text{-}L} = 20\log \frac{\textcircled{B}\,R}{\textcircled{B}\,L}$
Channel balance 1, Rch→Cch	$CB_{1R\text{-}C}$	– 1.5	0	1.5	dB	V_{IN} = 1Vrms, $CB_{1R\text{-}C} = 20\log \frac{\textcircled{B}\,R}{\textcircled{B}\,C}$
Channel balance 1, Lch→Cch	$CB_{1L\text{-}C}$	– 1.5	0	1.5	dB	V_{IN} = 1Vrms, $CB_{1L\text{-}C} = 20\log \frac{\textcircled{B}\,L}{\textcircled{B}\,C}$
Channel balance 2, Rch→Lch	$CB_{2R\text{-}L}$	– 2.0	0	2.0	dB	V_{IN} = 1Vrms, $CB_{2R\text{-}L} = 20\log \frac{\textcircled{B}\,R}{\textcircled{B}\,L}$
Channel balance 2, Rch→Cch	$CB_{2R\text{-}C}$	– 2.0	0	2.0	dB	V_{IN} = 1Vrms, $CB_{2R\text{-}C} = 20\log \frac{\textcircled{B}\,R}{\textcircled{B}\,C}$
Channel balance 2, Lch→Cch	$CB_{2L\text{-}C}$	– 2.0	0	2.0	dB	V_{IN} = 1Vrms, $CB_{2L\text{-}C} = 20\log \frac{\textcircled{B}\,L}{\textcircled{B}\,C}$
Bass boost gain, Rch	VB_{MAXR}	13	15.5	18	dB	Comparison with f = 100Hz, V_{IN} = 100mVrms, bass flat
Bass boost gain, Lch	VB_{MAXL}	13	15.5	18	dB	Comparison with f = 100Hz, V_{IN} = 100mVrms, bass flat
Bass boost gain, Cch	VB_{MAXC}	13	15.5	18	dB	Comparison with f = 100Hz, V_{IN} = 100mVrms, bass flat
Bass cut gain, Rch	VB_{MINR}	– 18	– 15.5	– 13	dB	Comparison with f = 100Hz, V_{IN} = 100mVrms, bass flat
Bass cut gain, Lch	VB_{MINL}	– 18	– 15.5	– 13	dB	Comparison with f = 100Hz, V_{IN} = 100mVrms, bass flat
Bass cut gain, Cch	VB_{MINC}	– 18	– 15.5	– 13	dB	Comparison with f = 100Hz, V_{IN} = 100mVrms, bass flat
Treble boost gain, Rch	VT_{MAXR}	9	12	15	dB	Comparison with f = 10kHz, V_{IN} = 100mVrms, treble flat
Treble boost gain, Lch	VT_{MAXL}	9	12	15	dB	Comparison with f = 10kHz, V_{IN} = 100mVrms, treble flat
Treble boost gain, Cch	VT_{MAXC}	9	12	15	dB	Comparison with f = 10kHz, V_{IN} = 100mVrms, treble flat
Treble cut gain, Rch	VT_{MINR}	– 15	– 12	– 9	dB	Comparison with f = 10kHz, V_{IN} = 100mVrms, treble flat
Treble cut gain, Lch	VT_{MINL}	– 15	– 12	– 9	dB	Comparison with f = 10kHz, V_{IN} = 100mVrms, treble flat
Treble cut gain, Cch	VT_{MINC}	– 15	– 12	– 9	dB	Comparison with f = 10kHz, V_{IN} = 100mVrms, treble flat
AGC input / output level 1, Rch	V_{AGC1R}	0.7	1	1.4	mVrms	V_{IN} = 1mVrms
AGC input / output level 1, Lch	V_{AGC1L}	0.7	1	1.4	mVrms	V_{IN} = 1mVrms
AGC input / output level 2, Rch	V_{AGC2R}	50	80	110	mVrms	V_{IN} = 50mVrms
AGC input / output level 2, Lch	V_{AGC2L}	50	80	110	mVrms	V_{IN} = 50mVrms
AGC input / output level 3, Rch	V_{AGC3R}	90	130	170	mVrms	V_{IN} = 110mVrms
AGC input / output level 3, Lch	V_{AGC3L}	90	130	170	mVrms	V_{IN} = 110mVrms
AGC input / output level 4, Rch	V_{AGC4R}	160	210	260	mVrms	V_{IN} = 1Vrms

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
AGC input / output level 4, Lch	V_{AGC4L}	160	210	260	mVrms	V_{IN} = 1Vrms
Total harmonic distortion at AGC ON, Rch	THD_{AGCR}	—	0.4	1	%	V_{IN} = 200mVrms
Total harmonic distortion at AGC ON, Lch	THD_{AGCL}	—	0.4	1	%	V_{IN} = 200mVrms
Max. surround gain, Rch	V_{SUMAXR}	4	6	8	dB	V_{IN} = 100mVrms, V_{SUMAXR} = 20log Ⓑ / V_{IN}
Max. surround gain, Lch	V_{SUMAXL}	4	6	8	dB	V_{IN} = 100mVrms, V_{SUMAXL} = 20log Ⓑ / V_{IN}
Min. surround gain, Rch	V_{SUMINR}	0	1	3.5	dB	V_{IN} = 100mVrms, V_{SUMINR} = 20log Ⓑ / V_{IN}
Min. surround gain, Lch	V_{SUMINL}	0	1	3.5	dB	V_{IN} = 100mVrms, V_{SUMINL} = 20log Ⓑ / V_{IN}
Surround gain at Loop ON, Rch	V_{LPSUR}	1.5	4	6.5	dB	V_{IN} = 100mVrms, V_{LPSUR} = 20log Ⓑ / V_{IN}
Surround gain at Loop ON, Lch	V_{LPSUL}	1.5	4	6.5	dB	V_{IN} = 100mVrms, V_{LPSUL} = 20log Ⓑ / V_{IN}
Bass Add ON gain, Rch	V_{BAONR}	7.5	10	12.5	dB	f = 100Hz, V_{IN} = 100mVrms, V_{BAONR} = 20log Ⓑ / V_{IN}
Bass Add ON gain, Lch	V_{BAONL}	7.5	10	12.5	dB	f = 100Hz, V_{IN} = 100mVrms, V_{BAONL} = 20log Ⓑ / V_{IN}
Pseudo-stereo gain, Rch	V_{MONR}	– 6.5	– 4	– 1.5	dB	V_{IN} = 100mVrms, V_{MONR} = 20log Ⓑ / V_{IN}
Pseudo-stereo gain, Lch	V_{MONL}	1.5	4	6.5	dB	V_{IN} = 100mVrms, V_{MONL} = 20log Ⓑ / V_{IN}
DAC pin operating voltage 1	V_{DAC1}	4.7	5	5.3	V	
DAC pin operating voltage 2	V_{DAC2}	—	0	0.3	V	
Suction current at I²C BUS ACK	I_{ACK}	2	—	—	mA	
SCL and SDA pin input high level	V_{IHI}	3.5	—	5	V	
SCL and SDA pin input low level	V_{ILO}	—	—	0.9	V	

✻ The phases are the same between the input and output signal pins.

●Measurement circuit

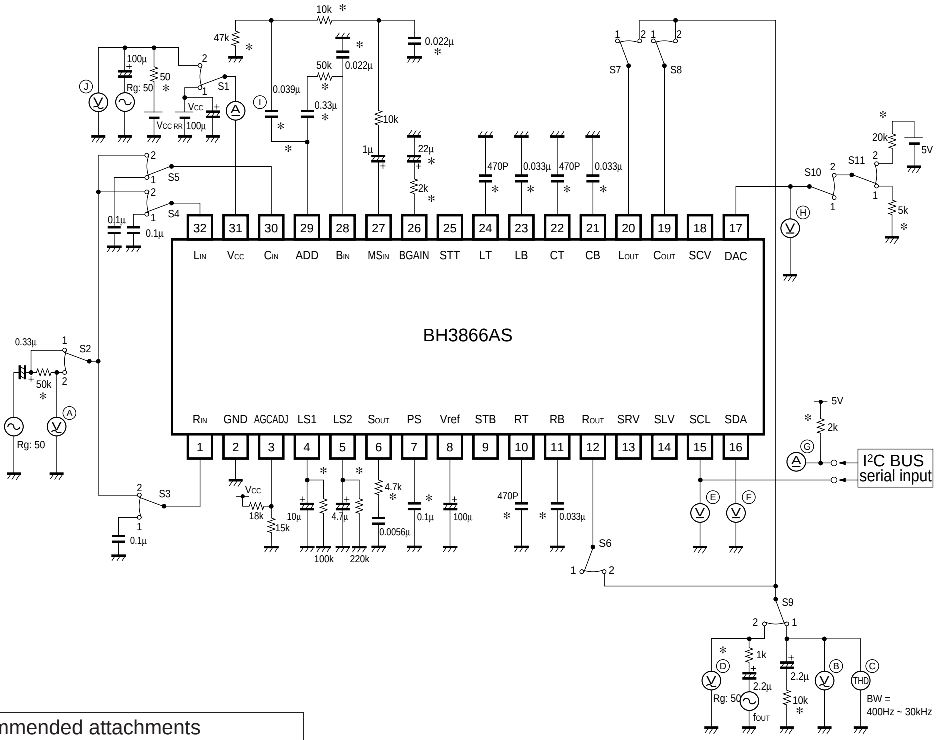


Fig.1

○Recommended attachments

①Elements marked with an asterisk

- Carbon-sheathed resistors: ± 1%
- Film capacitors: ± 1%
- Ceramic capacitors: ± 1%

②Unless otherwise noted, the following attachments should be used.

- Carbon-sheathed resistors: ± 5%
- Film capacitors: ± 20%

Precautions concerning wiring

①A bare ground should be used for GND.

②The wiring pattern of the I²C BUS should be separate from that of the analog unit, to avoid crosstalk.

③Parallel positioning of the SCL and SDA lines of the I²C BUS should be avoided wherever possible. If they are adjacent, they should be shielded.

●Measurement circuit switch operation

Slave address

MSB LSB

1	0	0	0	0	0	1	0

Parameter	Symbol	SW NO.											I²C BUS														Measurement point
													Selected address / data														
		1	2	3	4	5	6	7	8	9	10	11	0	0	0	1	0	2	0	3	0	4	0	5	0	6	
Quiescent circuit current	I_Q	1	—	1	1	1	1	1	1	—	1	—	F	F	F	F	F	F	2	0	2	0	0	0	0	C	Ⓘ
Max. output voltage, Rch	V_{OMR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	0	0	0	C	Ⓑ
Max. output voltage, Lch	V_{OML}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Max. output voltage, Cch	V_{OMC}	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	F	F	2	0	2	0	0	0	0	C	Ⓑ
Voltage gain, Rch	G_{VR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	0	0	0	C	Ⓑ
Voltage gain, Lch	G_{VL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Voltage gain, Cch	G_{VC}	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	F	F	2	0	2	0	0	0	0	C	Ⓑ

Slave address

MSB							LSB
1	0	0	0	0	0	1	0

Parameter	Symbol	SW NO.											I²C BUS														Measurement point
													Selected address / data														
		1	2	3	4	5	6	7	8	9	10	11	0	0	0	1	0	2	0	3	0	4	0	5	0	6	
Total harmonic distortion, Rch	THD_R	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	0	0	0	C	Ⓒ
Total harmonic distortion, Lch	THD_L	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	0	0	0	C	Ⓒ
Total harmonic distortion, Cch	THD_C	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	F	F	2	0	2	0	0	0	0	C	Ⓒ
Output noise voltage, Rch	V_{NOR}	1	1	1	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	0	0	0	C	Ⓑ
Output noise voltage, Lch	V_{NOL}	1	1	1	1	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Output noise voltage, Cch	V_{NOC}	1	1	1	1	1	1	1	2	1	1	—	0	0	0	0	F	F	2	0	2	0	0	0	0	C	Ⓑ
Residual noise voltage, Rch	V_{MNOR}	1	1	1	1	1	2	1	1	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Residual noise voltage, Lch	V_{MNOL}	1	1	1	1	1	1	2	1	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓒ
Residual noise voltage, Cch	V_{MNOC}	1	1	1	1	1	1	1	2	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓒ
Crosstalk, Rch→Lch	$CT_{R\text{-}L}$	1	1	2	1	1	1	2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	C	Ⓑ
Crosstalk, Rch→Cch	$CT_{R\text{-}C}$	1	1	2	1	1	1	1	2	1	1	—	0	0	F	F	F	F	2	0	2	0	0	0	0	C	Ⓑ
Crosstalk, Lch→Rch	$CT_{L\text{-}R}$	1	1	1	2	1	2	1	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	C	Ⓑ
Crosstalk, Lch→Cch	$CT_{L\text{-}C}$	1	1	1	2	1	1	1	2	1	1	—	F	F	0	0	F	F	2	0	2	0	0	0	0	C	Ⓑ
Crosstalk, Cch→Rch	$CT_{C\text{-}R}$	1	1	1	1	2	2	1	1	1	1	—	0	0	F	F	F	F	2	0	2	0	0	0	0	C	Ⓑ
Crosstalk, Cch→Lch	$CT_{C\text{-}L}$	1	1	1	1	2	1	2	1	1	1	—	F	F	0	0	F	F	2	0	2	0	0	0	0	C	Ⓑ
Input impedance, Rch	R_{INR}	1	2	2	1	1	1	1	1	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓐ
Input impedance, Lch	R_{INL}	1	2	1	2	1	1	1	1	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓐ
Input impedance, Cch	R_{INC}	1	2	1	1	2	1	1	1	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓐ
Output impedance, Rch	R_{OUTR}	1	1	1	1	1	2	1	1	2	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓓ
Output impedance, Lch	R_{OUTL}	1	1	1	1	1	1	2	1	2	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓓ
Output impedance, Cch	R_{OUTC}	1	1	1	1	1	1	1	2	2	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓓ
Ripple rejection, Rch	RR_R	2	1	1	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	0	0	0	C	Ⓑ
Ripple rejection, Lch	RR_L	2	1	1	1	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Ripple rejection, Cch	RR_C	2	1	1	1	1	1	1	2	1	1	—	0	0	0	0	F	F	2	0	2	0	0	0	0	C	Ⓑ
Muting level, Rch	V_{MUTER}	1	1	2	1	1	2	1	1	1	1	—	F	F	F	F	F	F	2	0	2	0	0	0	0	E	Ⓑ
Muting level, Lch	V_{MUTEL}	1	1	1	2	1	1	2	1	1	1	—	F	F	F	F	F	F	2	0	2	0	0	0	0	E	Ⓑ
Muting level, Cch	V_{MUTEC}	1	1	1	1	2	1	1	2	1	1	—	F	F	F	F	F	F	2	0	2	0	0	0	0	E	Ⓑ
Volume attenuation, Rch	ATT_{MAXR}	1	1	2	1	1	2	1	1	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Volume attenuation, Lch	ATT_{MAXL}	1	1	1	2	1	1	2	1	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Volume attenuation, Cch	ATT_{MAXC}	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	0	0	2	0	2	0	0	0	0	C	Ⓑ
Channel balance 1, Rch→Lch	$CB_{1R\text{-}L}$	1	1	2	2	1	2 / 1	1 / 2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	C	Ⓑ
Channel balance 1, Rch→Cch	$CB_{1R\text{-}C}$	1	1	2	1	2	2 / 1	1	1 / 2	1	1	—	0	0	F	F	F	F	2	0	2	0	0	0	0	C	Ⓑ
Channel balance 1, Lch→Cch	$CB_{1L\text{-}C}$	1	1	1	2	2	1	2 / 1	1 / 2	1	1	—	F	F	0	0	F	F	2	0	2	0	0	0	0	C	Ⓑ
Channel balance 2, Rch→Lch	$CB_{2R\text{-}L}$	1	1	2	2	1	2 / 1	1 / 2	1	1	1	—	3	3	3	3	0	0	2	0	2	0	0	0	0	C	Ⓑ
Channel balance 2, Rch→Cch	$CB_{2R\text{-}C}$	1	1	2	1	2	2 / 2	1	1 / 2	1	1	—	0	0	3	3	3	3	2	0	2	0	0	0	0	C	Ⓑ
Channel balance 2, Lch→Cch	$CB_{2L\text{-}C}$	1	1	1	2	2	1	2 / 1	1 / 2	1	1	—	3	3	0	0	3	3	2	0	2	0	0	0	0	C	Ⓑ
Bass boost gain, Rch	VB_{MAXR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	7	F	2	0	0	0	0	C	Ⓑ

Slave address

MSB LSB

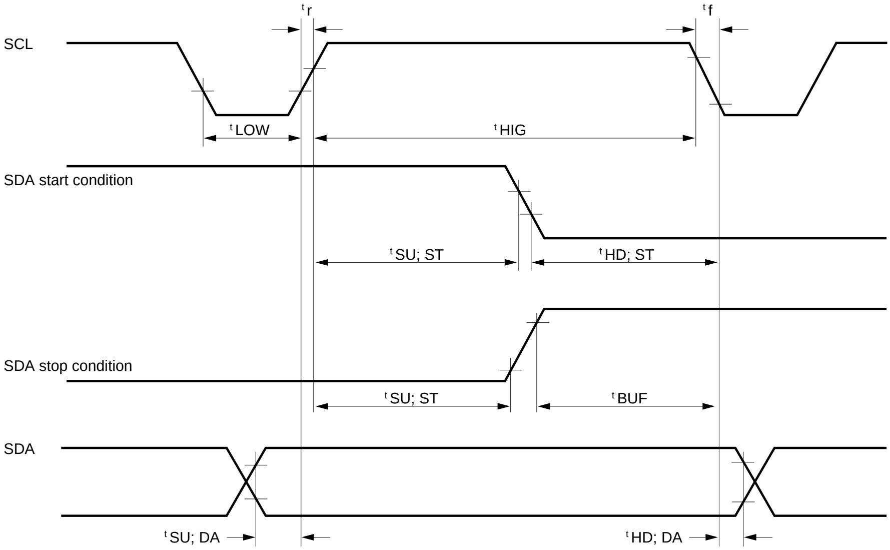
1	0	0	0	0	0	1	0

Parameter	Symbol	SW NO.											I²C BUS														Measurement point
													Selected address / data														
		1	2	3	4	5	6	7	8	9	10	11	0	0	0	1	0	2	0	3	0	4	0	5	0	6	
Bass boost gain, Lch	VB_{MAXL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	7	F	2	0	0	0	0	C	Ⓑ
Bass boost gain, Cch	VB_{MAXC}	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	F	F	7	F	2	0	0	0	0	C	Ⓑ
Bass cut gain, Rch	VB_{MINR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	0	0	2	0	0	0	0	C	Ⓑ
Bass cut gain, Lch	VB_{MINL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	0	0	2	0	0	0	0	C	Ⓑ
Bass cut gain, Cch	VB_{MINC}	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	F	F	0	0	2	0	0	0	0	C	Ⓑ
Treble boost gain, Rch	VT_{MAXR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	7	F	0	0	0	C	Ⓑ
Treble boost gain, Lch	VT_{MAXL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	7	F	0	0	0	C	Ⓑ
Treble boost gain, Cch	VT_{MAXC}	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	F	F	2	0	7	F	0	0	0	C	Ⓑ
Treble cut gain, Rch	VT_{MINR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	0	0	0	0	0	C	Ⓑ
Treble cut gain, Lch	VT_{MINL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	0	0	0	0	0	C	Ⓑ
Treble cut gain, Cch	VT_{MINC}	1	1	1	1	2	1	1	2	1	1	—	0	0	0	0	F	F	2	0	0	0	0	0	0	C	Ⓑ
AGC input / output level 1, Rch	V_{AGC1R}	1	1	2	2	1	2	1	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
AGC input / output level 1, Lch	V_{AGC1L}	1	1	2	2	1	1	2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
AGC input / output level 2, Rch	V_{AGC2R}	1	1	2	2	1	2	1	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
AGC input / output level 2, Lch	V_{AGC2L}	1	1	2	2	1	1	2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
AGC input / output level 3, Rch	V_{AGC3R}	1	1	2	2	1	2	1	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
AGC input / output level 3, Lch	V_{AGC3L}	1	1	2	2	1	1	2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
AGC input / output level 4, Rch	V_{AGC4R}	1	1	2	2	1	2	1	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
AGC input / output level 4, Lch	V_{AGC4L}	1	1	2	2	1	1	2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓑ
Total harmonic distortion at AGC ON, Rch	THD_{AGCR}	1	1	2	2	1	2	1	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓒ
Total harmonic distortion at AGC ON, Lch	THD_{AGCL}	1	1	2	2	1	1	2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	0	0	0	1	Ⓒ
Max. surround gain, Rch	V_{SUMAXR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	C	F	0	0	Ⓑ
Max. surround gain, Lch	V_{SUMAXL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	C	F	0	0	Ⓑ
Min. surround gain, Rch	V_{SUMINR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	C	0	0	0	Ⓑ
Min. surround gain, Lch	V_{SUMINL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	C	0	0	0	Ⓑ
Surround gain at Loop ON, Rch	V_{LPSUR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	D	6	0	0	Ⓑ
Surround gain at Loop ON, Lch	V_{LPSUL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	D	6	0	0	Ⓑ
Bass Add ON gain, Rch	V_{BAONR}	1	1	2	1	1	2	1	1	1	1	—	0	0	F	F	0	0	2	0	2	0	0	0	1	0	Ⓑ
Bass Add ON gain, Lch	V_{BAONL}	1	1	1	2	1	1	2	1	1	1	—	F	F	0	0	0	0	2	0	2	0	0	0	1	0	Ⓑ
Pseudo-stereo gain, Rch	V_{MONR}	1	1	2	2	1	2	1	1	1	1	—	F	F	F	F	0	0	2	0	2	0	A	F	0	0	Ⓑ
Pseudo-stereo gain, Lch	V_{MONL}	1	1	2	2	1	1	2	1	1	1	—	F	F	F	F	0	0	2	0	2	0	A	F	0	0	Ⓑ
DAC pin operating voltage 1	V_{DAC1}	1	1	1	1	1	1	1	1	1	2	1	0	0	0	0	0	0	2	0	2	0	0	0	2	0	Ⓗ
DAC pin operating voltage 2	V_{DAC2}	1	1	1	1	1	1	1	1	1	2	2	0	0	0	0	0	0	2	0	2	0	0	0	0	0	Ⓗ
Suction current at I²C BUS ACK	I_{ACK}	1	1	1	1	1	1	1	1	1	1	—															Ⓖ
SCL and SDA pin input high level	V_{IHI}	1	1	1	1	1	1	1	1	1	1	—															Ⓔ Ⓕ
SCL and SDA pin input low level	V_{ILO}	1	1	1	1	1	1	1	1	1	1	—															Ⓔ Ⓕ

●Data setting methods

(1) I^{2}C BUS timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency range	F_{SCL}	0	—	100	kHz
The HIGH period of the clock	t_{HIGH}	4	—	—	µs
THe LOW period of the clock	t_{LOW}	4.7	—	—	µs
SCL rise time	t_r	—	—	1	µs
SCL fall time	t_f	—	—	0.3	µs
Set-up time for start condition	t_{su}; STA	4.7	—	—	µs
Hold time for start condition	t_{HD}; STA	4	—	—	µs
Set-up time for stop condition	t_{su}; STO	4.7	—	—	µs
Time bus must be free before a new transmission can start	t_{BUF}	4.7	—	—	µs
Set-up time DATA	t_{su}; DAT	250	—	—	ns



^{t}SU; STA = start code set-up time.
^{t}HD; STA = start code hold time.
^{t}SU; STO = stop code set-up time.
^{t}BUF = bus free time.
^{t}SU; DAT = data set-up time.
^{t}HD; DAT = data hold time.

Fig.2 Timing requirements for I^{2}C BUS

The above characteristics are logical values in the IC design, and are not guaranteed based on the shipping inspection. Any problems that may arise will be handled through mutual discussion in good faith.

(2) I^{2}C BUS format

	MSB LSB		MSB LSB		MSB LSB		
S	Slave Address	A	Selected Address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

- S = Start condition (recognition of start bit)
- Slave Address = Recognition of IC. First 7 bits may consist of any data. The last bit must be LOW for writing purposes.
- A = Acknowledge bit (recognition of recognition response)
- Selected Address = Selection of volume, bass, treble, or matrix surround.
- Data = Various items of volume and sound quality data.
- P = Stop condition (recognition of stop bit)

(3) Interface protocol

1) Basic format

S	Slave Address	A	Selected Address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Auto increment (the selected address is incremented (+ 1) by the number of data)

S	Slave Address	A	Selected Address	A	Data 1, Data 2, ..., Data N	A	P
	MSB LSB		MSB LSB		MSB LSB		

(Examples) ① Data 1 is set as the data of the address specified by the "Selected Address" parameter.
② Data 2 is set as the data of the address specified by the "Selected Address" parameter + 1.
③ Data 3 is set as the data of the address specified by the "Selected Address" parameter + N.

3) Configuration which cannot be transmitted (in this case, only selected address 1 is set)

S	Slave Address	A	Selected Address 1	A	Data	A	Selected Address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

CAUTION: If Selected Address 2 was sent as data following the data parameter,
the contents will be recognized as data, and not as Selected Address 2.

(4) BH3866AS slave address

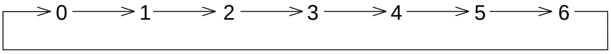
MSB							LSB
A6	A5	A4	A3	A2	A1	A0	R / W
1	0	0	0	0	0	1	0

The above slave address has been registered with Philips Corporation.

(5) Selected addresses

Set item		MSB			Selected address				LSB
		A7	A6	A5	A4	A3	A2	A1	A0
0	Lch volume	0	0	0	0	0	0	0	0
1	Rch volume	0	0	0	0	0	0	0	1
2	Cch volume	0	0	0	0	0	0	1	0
3	Tone (bass)	0	0	0	0	0	0	1	1
4	Tone (treble)	0	0	0	0	0	1	0	0
5	Surround	0	0	0	0	0	1	0	1
6	AGC	0	0	0	0	0	1	1	0

When sending continuous data, the auto increment function moves through the selected addresses in the following sequence.



(6) Data

Selected address		MSB			Data				LSB
Set item		A7	A6	A5	A4	A3	A2	A1	A0
00H	Lch volume	Lch Vol							
01H	Rch volume	Rch Vol							
02H	Cch volume	Cch Vol							
03H	Tone (bass)	✻	L / R / C Bass						
04H	Tone (treble)	✻	L / R / C Treble						
05H	Surround	SON	SSTE	SMON	LOOP	Surround effect			
06H	AGC	✻	✻	DAC	BASS	CSEL	CON	MUTE	AGC

Selected address	Contents		
00H │ 02H	Volume: all H: ATT 0dB all L: – ∞ (95dB) 1.0dB step level		
03H │ 04H	Bass / Tre: all H: Max. (FULL BOOST) all L: Min. (FULL CUT)		
05H	Surr effect: (Broad gain adjustment) all H: Max. (15dB) all L: Min. (0dB) 1dB step		
	· LOOP	H: on / L: off	Switch that varies the stage of the phase shift
	· SSTE	H: on / L: off	ON / OFF switch for (L – R) signal (stereo surround)
	· SMON	H: on / L: off	ON / OFF switch for (L + R) signal (pseudo-stereo)
	· SON	H: on / L: off	ON / OFF switch for surround effect
06H	· Mute	H: on / L: off	Muting switch
	· AGC	H: on / L: off	AGC ON / OFF switch
	· BASS	H: mix on / L: mix off	Low-pitch range mixing switch
	· CSEL	H: C on / L: C off	Selector switch for CIN input of COUT output or (L + R) signal
	· CON	H: H out / L: L off	Switch that selects whether or not COUT is output
	· DAC	H: H out / L: L out	0V or 5V output switch

(7) Volume and amount of attenuation (reference examples)

ATT (dB)	DATA (HEX)
0	FF
– 1	C4
– 2	AD
– 3	9F
– 4	93
– 5	8A
– 6	82
– 7	7B
– 8	75
– 9	6F
– 10	6A
– 11	66
– 12	61
– 13	5D
– 14	5A
– 15	56
– 16	53
– 17	50
– 18	4D

ATT (dB)	DATA (HEX)
– 19	4A
– 20	48
– 22	43
– 24	3E
– 26	3A
– 28	36
– 30	33
– 32	30
– 34	2D
– 36	2A
– 38	27
– 40	25
– 42	23
– 44	21
– 46	1F
– 48	1D
– 50	1B
– 52	19
– 54	18

ATT (dB)	DATA (HEX)
– 56	16
– 58	15
– 60	14
– 62	13
– 63	12
– 67	10
– 68	0F
– 70	0E
– 73	0D
– 76	0C
– 78	0B
– 84	09
– ∞	00

CAUTION: The settings in the above table are reference values. When using them, make sure values are confirmed carefully before being set.

(8) Bass and treble gain settings (reference examples)

Step	I^2C DATA (HEX)	Bass Gain (dB)	Treble Gain (dB)
15	7F	15.9	12.0
14	36	15.2	11.2
13	34	14.3	10.4
12	32	13.0	9.2
11	31	12.2	8.5
10	30	11.3	7.6
9	2F	10.4	6.8
8	2E	9.3	5.8
7	2D	8.0	4.8
6	2C	6.7	3.8
5	2B	5.3	2.9
4	2A	4.0	2.0
3	29	2.9	1.4
2	28	1.8	0.8
1	27	1.1	0.4
0	20	0.0	0.0

Step	I^2C DATA (HEX)	Bass Gain (dB)	Treble Gain (dB)
– 1	18	– 1.5	– 0.8
– 2	17	– 2.4	– 1.3
– 3	16	– 3.4	– 2.0
– 4	15	– 4.6	– 2.8
– 5	14	– 5.8	– 3.7
– 6	13	– 7.1	– 4.7
– 7	12	– 8.3	– 5.7
– 8	11	– 9.5	– 6.6
– 9	10	– 10.6	– 7.5
– 10	0F	– 11.5	– 8.3
– 11	0E	– 12.3	– 9.0
– 12	0D	– 13.0	– 9.6
– 13	0B	– 14.2	– 10.6
– 14	09	– 15.0	– 11.3
– 15	00	– 15.6	– 11.8

Table 5: Tone microcomputer data (the gain value is given as a guide).

CAUTION:

(1) The gain values given in the table above for treble and bass data are the data when the filter constant is specified such that the peak and bottom values on the frequency characteristic diagram will be at the maximum and minimum gain levels.

(2) The settings in the above table are reference values. When using them, make sure values are confirmed carefully before being set.

●Application example

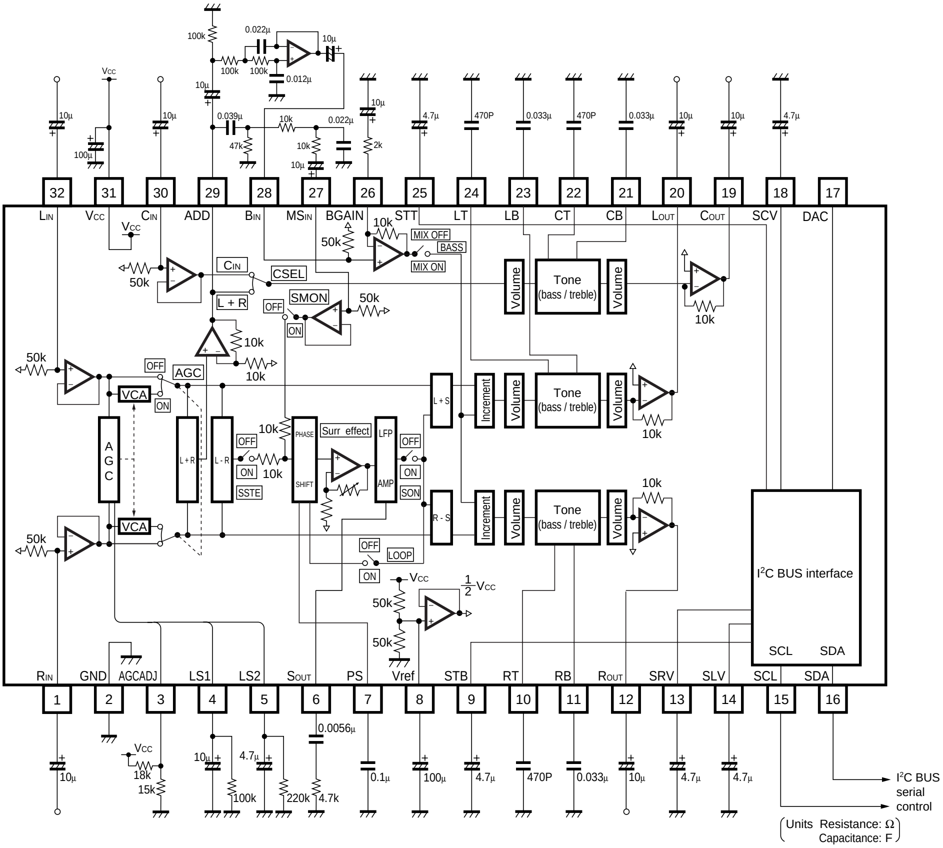


Fig.3

●Operation notes

(1) Operating power supply voltage range

Within the operating power supply voltage range, operation of the basic circuit functions is guaranteed for the ambient operating temperature, but when using the product, be sure that settings for constants and elements, voltage settings, and temperature settings are carefully confirmed.

(2) Operating temperature

Within the recommended operating voltage range, operation of the circuit functions is guaranteed for the operating temperature range. Be aware that power dissipation conditions are related to the temperature. Also, except for conditions determined by electrical characteristics within this range, the rated values for electrical characteristics cannot be guaranteed, but the essential functions are maintained.

(3) Application example

We guarantee the application circuit design, but recommend that you thoroughly check its characteristics in actual use. If you change any of the external component values, check both the static and transient characteristics of the circuit, and allow sufficient margin in your selections to take into account variations in the components and ICs.

Note that Rohm has not fully investigated patent rights regarding this product.

(4) Bass filter for tone control

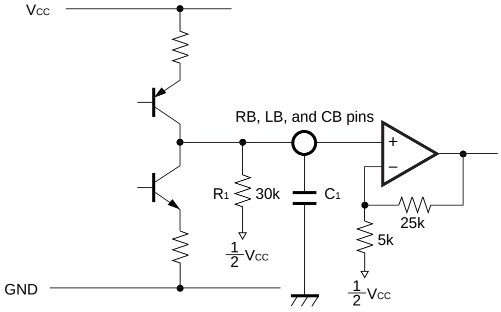


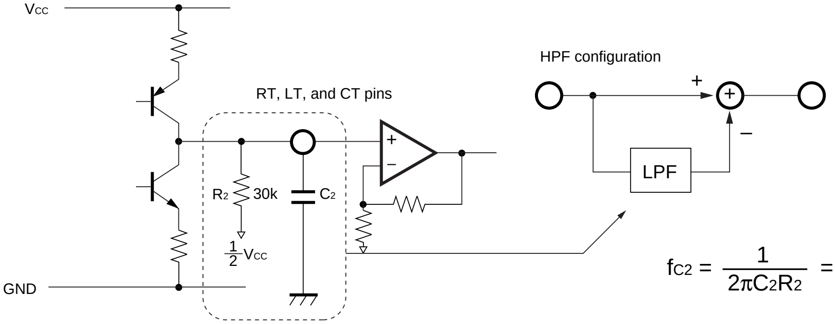
Fig.4

· Determining cutoff frequencies

$$f_{C1} = \frac{1}{2\pi C_1 R_1} = \frac{1}{2\pi C_1 \times 30k}$$

At a frequency of f_{C1}, the LPF will be –3dB.

(5) Treble filter for tone control



$$f_{C2} = \frac{1}{2\pi C_2 R_2} = \frac{1}{2\pi C_2 \times 30k}$$

Fig.5

(6) Setting the AGC level

The AGC level is set by the voltage divider between voltage VCC and GND. A gain of 0dB voltage should be used in the range of 100mVrms to 400mVrms.

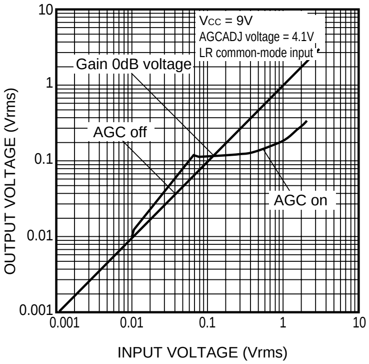


Fig. 6 (Reference data)
AGC characteristic

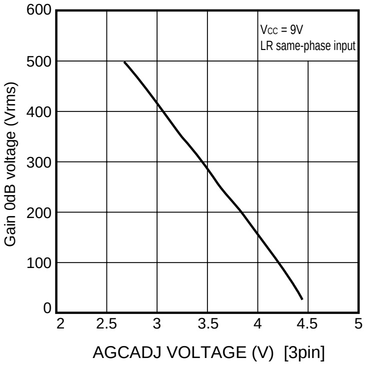


Fig. 7 (Reference data) Relation between AGCADJ voltage and gain 0dB voltage

(7) Determining the external LS1 (pin 4) and LS2 (pin 5) for the AGC

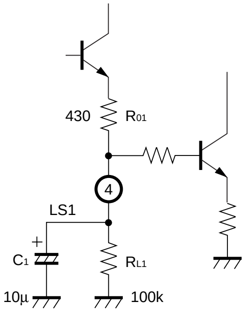


Fig.8 Suppressing phase detecting circuit

- Attack time: $R_{01} \times C_1$
- Recovery time: $R_{L1} \times C_1$

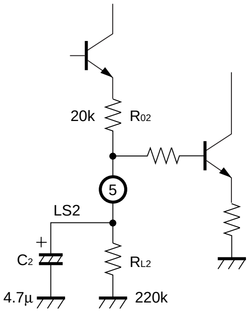


Fig.9 Amplifying phase detection circuit

- Attack time: $R_{02} \times C_2$
- Recovery time: $R_{L2} \times C_2$

The attack and recovery times should be determined based on the internal resistors in the IC and on the external capacitor and resistor. The internal resistors are R_{01} = 430Ω and R_{02} = 20kΩ (Typ.). Reducing the constant of the C_2 capacitor of LS2 shifts the point where amplification begins in the direction of a lower input voltage. The distortion ratio changes as well, in the direction of worse distortion. Reducing the constant of the C_1 capacitor of LS1 causes worse distortion. Increasing the resistance value of RL_1 causes the amount of suppression to decrease.

(8) Attachment of external SOUT (pin 6) of surround section L.P.F.

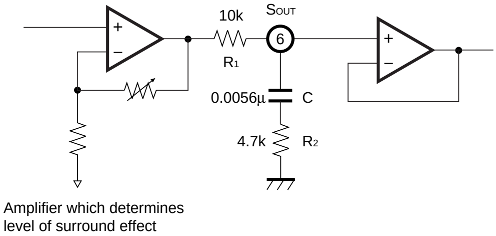


Fig.10

$$f_1 = \frac{1}{2\pi C R_2}$$

$$f_2 = \frac{1}{2\pi C\,(R_1 + R_2)}$$

$$A_1 = \frac{R_2}{R_1 + R_2}$$

$$A_2 = 1$$

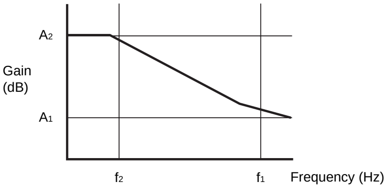


Fig.11

(9) External PS (pin 7) of the phase shifter

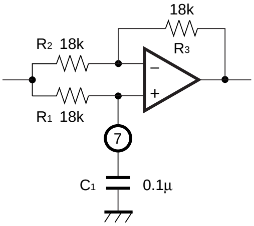


Fig.12

The resistance in the IC is 18kΩ (Typ.).
$\phi = -2\tan^{-1}(2\pi f R_1 C_1)$

(10) Surround and pseudo-stereo effects

1) Surround

Δt: Time of delay caused by phase shifter

P: Amount attenuated at phase shifter stage

E: Amount of surround effect

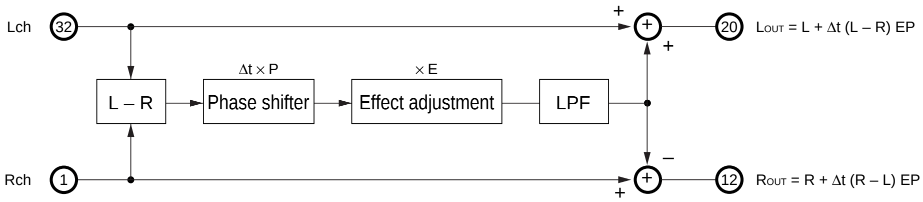


Fig.13

2) Pseudo-stereo effect

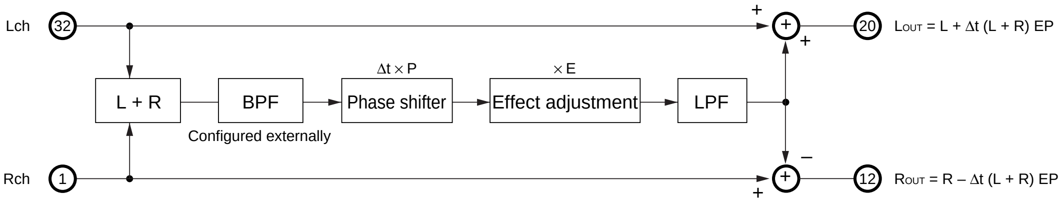


Fig.14

The internal blocks in the IC for the surround and pseudo-stereo effects are configured as shown above. The feeling of the surround location and the stereo feeling of the pseudo-stereo effect can be changed by varying the amount of the effect. Also, the loop switch can be turned on to create a pseudo-increase in the number of phase shifter stages. Raising the gain of the effect level with the loop switch on causes instability, however, so the level of the effects should be kept at around 6dB or below. In order to prevent a popping sound when switching between the surround and pseudo-stereo effects, the switch on the stereo surround side of the SSTE should be left in the ON position.

(11) The level of the surround effect

The level of the surround effect can be varied between 0 and 15dB, using I^{2}C BUS data. Please be aware, however, that this gain is not the total gain between input and output. In precise terms, it specifies the effect level control range of the surround signal for the SOUT pin. (With single-side input and the stereo / surround effects: V_{CC} = 9V, f = 1kHz, V_{IN} = 100mVrms, Ta = 25°C.)

(12) Pin 17 (DAC) output

Setting the DAC command for the I^{2}C BUS to HIGH enables 5V output, and setting it to LOW enables 0V output.

(13) BASS command

Creating an external LPF with the signals (L + R) output from ADD (pin 29) and inputting those signals to BIN (pin 28) enables configuration of a low-pitch amplification circuit. This switch serves as the I^{2}C BUS bass command. The gain for the amplifier can be set through the external resistance, using BGAIN (pin 26).

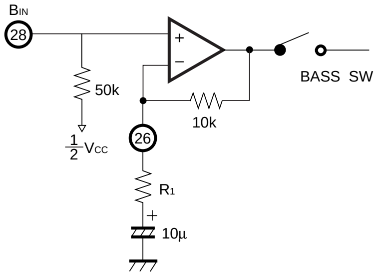


Fig.15

$$\text{Gain} = 20\log\frac{10k + R_1}{R_1}$$

(14) The necessity for Cch and the application

If there are only a left and right speaker, moving slightly to the left or right of the television set causes a difference in the sound paths, and a characteristic trough from 500Hz to 2kHz is created by the ensuing interference, producing a muffled or contained sound. Also, listeners positioned to the left or right hear the sounds from the closest speaker causing the positions of the image and sound to not match. Due to their setup, low-pitched sounds are produced more easily from the left and right speakers. However, in front of the speakers, because the placement of the speakers directs the sound in a cone-shaped direction, traveling along the sides of the television, a "port" effect results and the sound becomes muffled. To solve this problem, a center speaker is provided, and assuming this speaker is attached directly to the center grille, the orientation and clarity are improved significantly. Also, as a center channel application, this can be used to adjust the microphone mixing level, enabling use of the set as a karaoke set.

(15) Noise when the step is switched

In the application circuit example, using the SRV, SLV, SCV, STB, and STT pins as an example, constants are provided for each. These constants change depending on the signal level setting, the mounting wiring pattern, and other factors. Careful consideration should be given to the constants before they are determined. An internal equivalent circuit is shown below. (A primary integration circuit is set, so that changes are implemented slowly.)

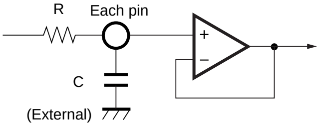


Fig.16

	R value (kΩ)
SRV, SLV, SCV, STB, STT	30

(16) Level settings for volume and tone

In this databook, values are noted for the control serial data in relation to the amount of attenuation or gain, as reference values. Since the internal D / A converter is configured on the R-2R system, data exists in locations where there are no continuous changes between one item of data and the next. This can be used where detailed settings are required. However, <u>the volume must be set within eight bits (256 steps), and the tone within seven bits (64 + 1 step).</u>

(17) I^{2}C BUS control

High-frequency digital signals are input to the SCL and SDA pins, so the wiring and wiring patterns must be arranged in such a way that they do not interfere with the analog signal system line.

(18) Power On Reset

When the power supply is turned on, an internal circuit carries out an initialization within the IC. When the power supply is turned on, the volume levels of the left, right, and center channels are set to – ∞, and the DAC output (pin 17) is set to 0V. Once it has been turned on, if the power supply is turned off and then immediately turned on again, if there is any residual load on the capacitor, there may be cases when the status described above does not occur. If this happens, operation should be carried out with the muting function on, until an I^{2}C BUS command is transmitted.

(19) Vref (pin 8) capacitor

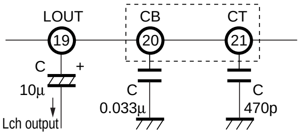
A capacitance of 100µF is recommended for the power supply filter attached to V$_{REF}$. If this capacitance is set too low, the minimum attenuation level of the volume deteriorates. Crosstalk also tends to deteriorate. The IC contains internal pre-charge and discharge circuits for the capacitor attached to Vref.

(20) Excessive input

Steps have been taken with this product to avoid a situation in which, if a signal is input which exceeds the maximum input voltage for the LIN, RIN, and CIN pins, a rebound waveform is produced even if hard clipping of the output signal is implemented. Consequently, there is no need to worry that the listener will hear distorted sound because of a rebound waveform.

(21) Request concerning the fundamental design

Due to its pin layout, it is difficult to remove crosstalk from the left channel to the center channel in this IC. This is because the output signal at LOUT (pin 20) overlaps the capacitance coupling of CB (pin 21) and CT (pin 22). This should be given adequate consideration in the fundamental design of the set, when the pattern is laid out. The following illustration shows an example of countermeasures.



(22) Relation with the BH3865S

The BH3866AS and BH3865S are pin compatible, and share some of the same selected address and data parameters for the I^2C BUS. Therefore, the same substrates and software can be shared at the product planning stage.

●Electrical characteristic curves

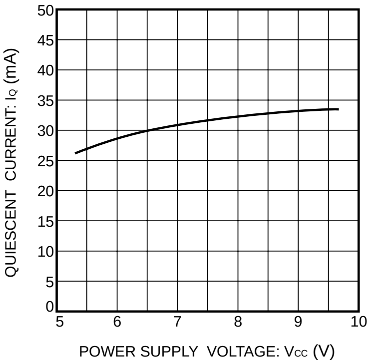


Fig. 17 Quiescent current vs. power supply voltage

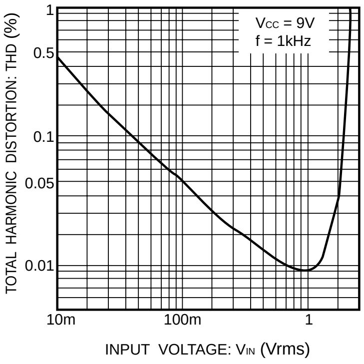


Fig. 18 Total harmonic distortion vs. input voltage

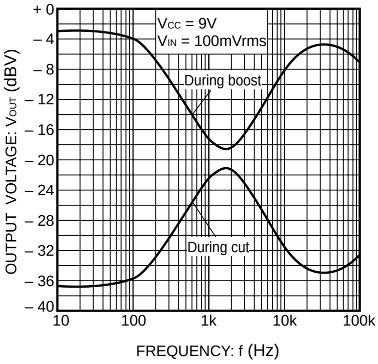
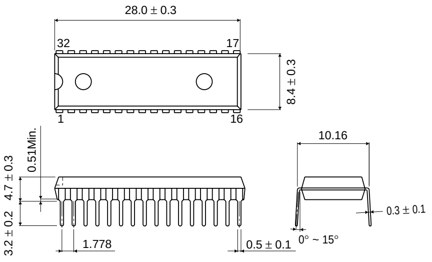


Fig. 19 Output gain vs. frequency

●External dimensions (Units: mm)



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