2.0 POW-R-BLOK™ Module Mounting

When mounting POW-R-BLOK™ modules to a heatsink, care should be taken to avoid applying uneven torque to the baseplate due to one sided tightening. It is recommended that the mounting screws be tightened in the fashion shown in Figure 2.1. The device data sheet lists the maximum torque rating for both the mounting screws and, where applicable, the terminal screws.

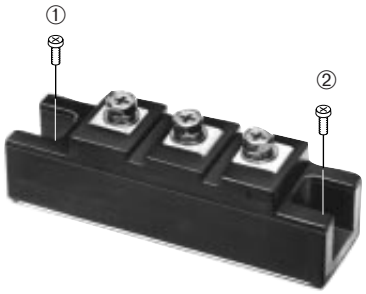
The use of thermal compounds when mounting POW-R-BLOK™ modules to heatsinks is highly recommended to prevent hot spots due to voids between the package and the heatsink surface. It is important to select a thermal compound which has a stable characteristic over the operating temperature range and the lifetime of the equipment.

The compound should be applied in a very thin layer, applying a thin coating with a spatula or lintless brush and wiping lightly to remove excess material. Another method is to place a predetermined minimal amount at or along the center of the contact area. Then in mounting, rotation and pressure will force the compound over the contact area and experience will indicate whether the quantity is sufficient as excess will appear around the edges of the contact area. Excess compound may be wiped away using a cloth wetted with acetone or alcohol. The use of thick consistency thermal compounds should be avoided, particularly with larger modules, since it may not compress evenly when the module is torqued.

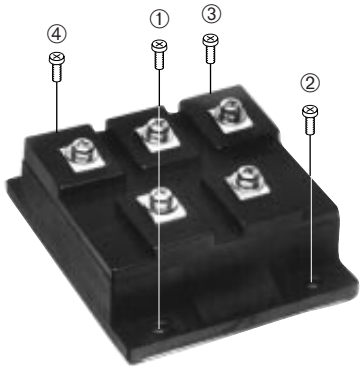
A number of manufacturers supply a wide variety of thermal grease and fluid type compounds. Among these are Wakefield, Dow-Corning, Alcoa, and Thermalloy. In addtion, some manufacturers offer alternative thermal interface pads which avoid the application problems of greases. These materials, such as THERMSTRATE™, are often available in pre-cut shapes that accommodate many POW-R-BLOK™, module packages.

It is recommended that heatsink surfaces be flat within ±1 mil/inch over the mounting area and have a surface finish of less than 64 microinches. It is also important to properly prepare the heatsink mounting surface just prior to module mounting. The heatsink surface should be thoroughly cleaned to remove any foreign material, oxides, or films. A satisfactory cleaning technique is to polish the mounting area with No. 000 fine steel wool, followed by an alcohol or acetone rinse.

Figure 2.1 Mounting Screw Fastening Pattern



Two-point mounting type
temporary tightening ① → ②
final tightening ② → ①



Four-point mounting type
temporary tightening ① → ② → ③ → ④
final tightening ④ → ③ → ② → ①

2.1 Gate Drive Recommendations

SCRs have extraordinarily high power gain. For example, a 90 Ampere, 1000 Volt SCR is guaranteed to turn on if a 100 mA, 3 Volt gate drive is applied. This is a power gain of 3 x 10^5. The power gain is further magnified as the required gate controlled signal is a pulse only a few microseconds wide.

To achieve reliable performance of the SCR, a gate drive signal greater than the minimum specified I_{GT} and V_{GT} values is required. Because of the diverse range of SCR applications, a DC gate test condition with a resistive load was established for the basic gate parameters, I_{GT} and V_{GT}, found on a typical data sheet.

These DC gate trigger parameters are not intended to reflect operational application requirements.

The reason for the gate overdrive requirement is the finite time required to achieve full area conduction in the SCR. This di/dt problem, is especially critical in the first few microseconds of turn-on, when only a very small percentage of the total device area will be in conduction. The initial conduction area is highly dependent upon gate-to-cathode geometry and the amount of gate current overdrive.

Most POW-R-BLOK™ modules utilize SCRs with di-namic gate designs. The di-namic gate design provides an integrated pilot SCR connected from anode to gate of the main SCR. The pilot SCR provides rapid turn on of a significant portion of the main SCR section of the device. Di-namic gate devices allow the use of soft gate drive for most applications. However, applications still exist even with di-namic gate devices which require hard gate drive.

Figure 2.2 illustrates soft and hard gate drive waveforms and provides recommended gate current and voltage levels. Note that gatetrigger parameters are temperature dependent, with the required gate parameters increasing in magnitude as temperature decreases. Thus, the selection of drive levels should be made for the lowest operating temperature anticipated for the equipment. Hard gate drive is required for high repetitive di/dt applications typical of capacitive loads, heavy industrial phase control operation with inductive load, and systems where electrical noise is troublesome requiring gate signal suppression circuitry.

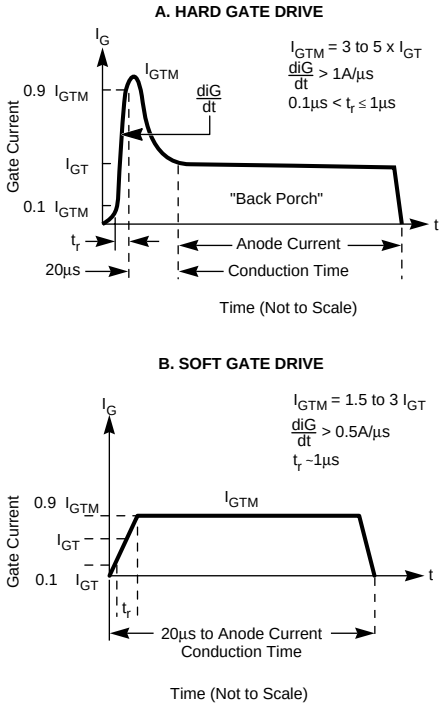
It is also necessary to increase the gate drive amplitude for pulse width less than 20 microseconds. This is due to the need for the SCR to receive a finite amount of charge to turn-on. Additional gate drive recommendations and precautions are enumerated here:

A. GENERAL CONSIDERATIONS

- Gate the SCR when the anode voltage is positive. Allowing a positive gate while the SCR becomes reverse biased limits device reliability.

- Design the gate firing sequence such that the snubber network across the SCR is charged prior to gate triggering. This gives good di-namic gate action.

Figure 2.2 Hard and Soft Gate Drive Waveforms

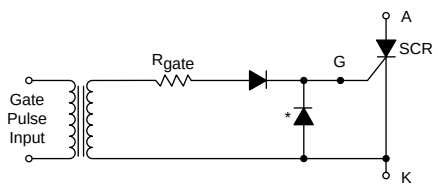


- If a DC gate signal is used in a multi-phase system a soft gate drive signal does not give good di-namic gate action. No snubber discharge is possible after time zero which results in poor di-namic gate action. In addition, POW-R-BLOK™ modules have high noise immunity characteristics, meaning they do not false trigger at very low gate currents. For this particular application, hard gate drive is required.

- The gate drive circuitry should have a 1 to 2 Amp average. 100 Volt diode in series with the gate and across the gate to cathode terminals as shown in Figure 2.3. These will eliminate two possible SCR failure modes. The diode in series will prevent negative gate current flow while the diode across the gate-to-cathode limits the reverse gate voltage by clamping.
- Minimize average gate power dissipation. Do not use excessive gate drive or excessively long gate pulses.

- Remember that SCRs require more gate current to trigger under narrow pulse width and

Figure 2.3 Diode Protected Gate Circuit



*May also employ a zener diode of appropriate rating to provide protection against excessive forward gate voltage transients in addition to the reverse voltage protection.

low junction temperature operating conditions, refer to Figure 2.4.

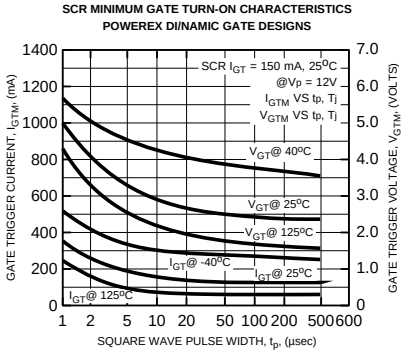
- Both excessive overdrive or weak underdrive can defeat the operation of the di-namic amplifying gate.

- Inductive loads can be troublesome if the gate drive is insufficient in amplitude or width. Recommended practice is the use of "picket fence" or hard gate drive. A picket fence is a high frequency gate signal varying from 1 to 15kHz, 20 to 50 microseconds wide, within a 60Hz envelope such that the SCR is continuously gated. The average gate current rating is maintained within device rating. In hard gate drive circuits, the "back porch" anticipates worse case power factor; making the gate pulse width wide enough to insure SCR latching and holding.

- Prevent noise pickup in the gate signal connections twisting together the gate and the cathode potential leads to the SCR and use either twisted pair wire from the gate pulse amplifier or a coax type shielded cable. Locate the gate wires as close as possible to the SCR but away from magnetics and high current carrying members of the power circuits. Of course, the gate signal leads should be as short as possible.

- Minimize delta delay time between SCRs using hard gate drive with as high a gate current rise time, (di_G/dt), as possible.

Figure 2.4 Minimum Pulsed Gate Trigger Parameters for a Typical SCR



- Always use a resistor in series with each gate lead if triggering more than the SCR from the same source. Generally, 10 to 25 ohms is used to diminish input gate cathode impedance variations.

- Use single point triggering if gating more than one device from the same source.

B. HIGH di/dt OPERATION

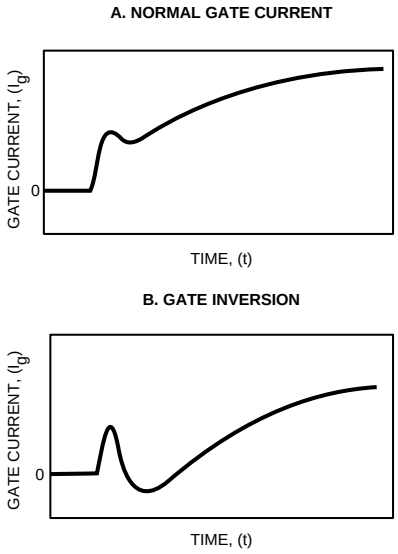
- Design for worst case di/dt and include all capacitance and snubber discharge currents in determining the SCR di/dt stress level.

- Treat SCR data sheet di/dt ratings like voltage ratings. Good engineering application practice dictates a 2 to 1 safety factor for reliable operation.

- Minimize gate drive rise time.

- Minimize or eliminate shunt capacitance and series inductance in the gate circuit

Figure 2.5 Normal Gate Current and Gate Inversion Waveforms



to prevent gate current inversion and resultant di/dt stress.

- Be aware that high di/dt can require open circuit gate source voltage upward of 40 Volts to prevent gate current inversion and assure reliable operation. Gate current inversion or gate drive extinction occurs when high anode di/dt causes the instantaneous gate cathode voltage to exceed the gate-to-source voltage. Refer to Figure 2.5.

C. LOW di/dt OPERATION

- Use DC gate drive when possible to minimize turn-on delay time.

- When using repetitive pulse/picket fence gate drive, maximize duty cycle to reduce

turn-on delay time and latching current effects.

D. VERY LOW ANODE VOLTAGE OPERATION

- Be aware that the SCR amplifying gate structure may not function at very low anode voltage. Observe turn-on behavior if anode voltage is less than 10 Volts.

- Assure adequate trigger current by driving with peak gate current in excess of five times the I_{GT} specification of the SCR.

2.2 Determining Power Losses

Proper application of SCRs, GTOs, and diodes requires that users determine device power losses and provide adequate cooling to keep junction temperatures within rated values.

For standard phase control applications, this process is greatly simplified by using the data sheet curves of power dissipation and maximum allowable case temperature versus average current. Use of these curves and explanations of the components of device power dissipation were explained in the Ratings and Characteristics section.

It is often required to calculate the root mean square (RMS) and/or average value of a waveform from peak currents, pulse widths, phase angles, etc., in order to determine device power losses. Figure 2.6 provides definitions and formulas for calculating RMS and average values of typical power control waveforms.

In some practical applications, the power waveform is a short pulse at a low duty cycle or some other irregular shape. In many of these situations it is not adequate to determine the average power dissipation and average junction temperature. Proper application requires that the peak operating junction temperature does not exceed the maximum allowable junction temperature.

The procedure for determining the peak junction temperature is to plot device power dissipation versus time by multiplying instantaneous current values by corresponding forward voltage values obtained from the device data sheet on-state current voltage characteristic curve. The peak junction temperature is then calculated using the transient thermal impedance curve.

For irregular waveforms, this procedure is tedious. For the purpose of calculating peak junction temperature, the irregular power waveshape can be approximated by a rectangular waveshape having an identical value of peak power and with a pulse width such that the average power is also identical. Figure 2.7 illustrates this square wave approximation technique. Translation into rectangular power pulses of power ensures a worst case approximation since a rectangular waveform will always have an equal or greater effect on temperature as an arbitrary waveform of equal peak and average values. After determination of the equivalent rectangular power waveform, the transient thermal impedance curve can be used along with the equations presented in Figure 2.8 to determine the peak junction temperature.

2.3 Voltage Ratings and Overvoltage Suppression

The voltage rating of an SCR, GTO, or diode must be selected high enough to withstand anticipated voltage transients as well as the repetitive peak forward and reverse voltages imposed upon the device by the application circuit. It is common practice with SCRs and diodes to provide a voltage safety factor of two times the maximum high line condition circuit voltage. Table 2.1 provides device voltage rating recommendations for common circuit voltages.

Table 2.1 Recommended Device Voltage Ratings

Supply Voltage ($V_{AC(RMS)}$)	Recommended Device Voltage Rating (V_{RRM}, V_{DRM})
120	400
240	800
480	1600
575	2000

Unanticipated voltage transients which exceed the blocking voltage ratings are probably the most frequent failure mode for SCRs and diodes. Because voltage breakdown tends to occur at the surface of the device, the energy required to cause damage can be

quite small. Techniques to protect against voltage transients include:

1. Redesign the circuit operation and/or physical layout to remove or minimize the source of the transient.
2. Suppress the transient by absorbing the energy in an appropriately designed RC snubber circuit located across the device or across the source of the transient. Design of a snubber for a specific device and application involves trade offs between many conflicting requirements. Figure 2.9 illustrates an RC snubber used with an SCR and provides general recommended snubber component values. Care must be taken in selecting the actual RC snubber component values to insure their capability to handle peak currents without overheating or adding additional transients to the circuit.
3. Use nonlinear resistive elements such as selenium transient suppressors, zener diodes, or metal oxide varistors (MOVs) in shunt with the device being protected. Maintain short leads between the transient suppressor and the device.
4. Occasional severe transients can sometimes be best limited by a solid-state crowbar circuit which shorts the line and absorbs the transient energy until a fuse or circuit breaker can be opened.

2.4 Typical Applications

POW-R-BLOK™ modules are utilized in a wide variety of applications. The circuit configurations and critical parameters for a number of common phase control applications are given Figure 2.10.

Figure 2.6 Definitions and Formulas for Calculating RMS and Average Values of Typical Power Control Waveforms

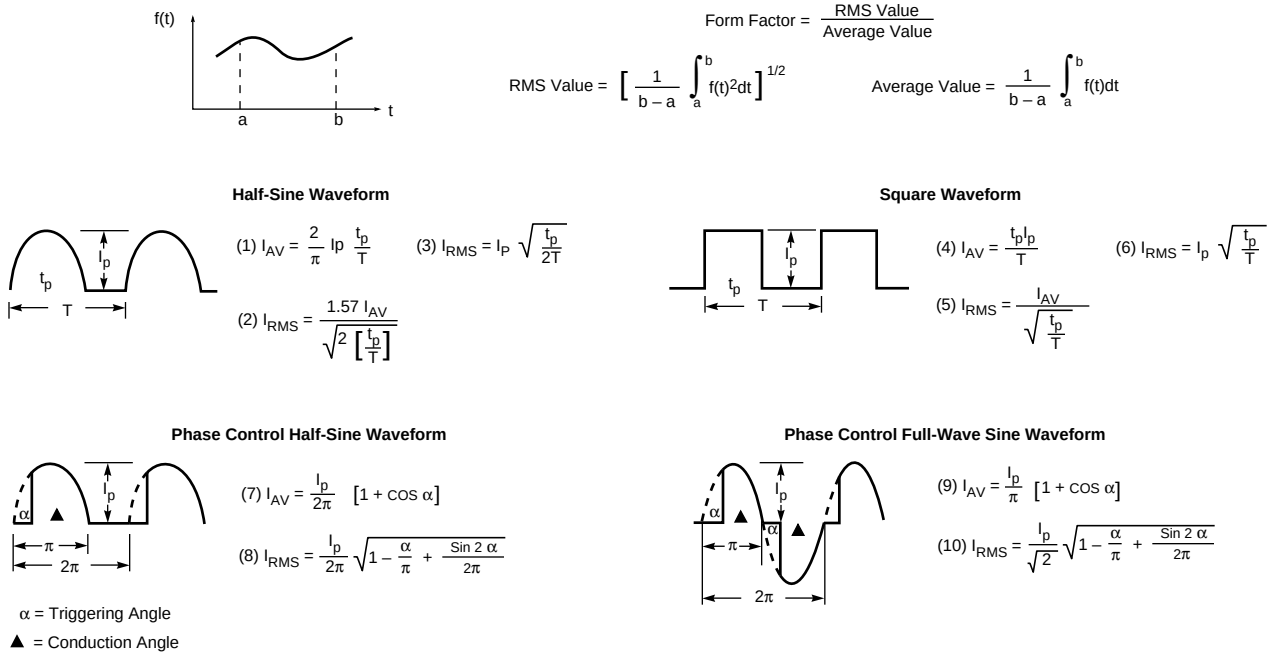


Figure 2.7 Square Wave Approximation of Irregular Power Waveforms

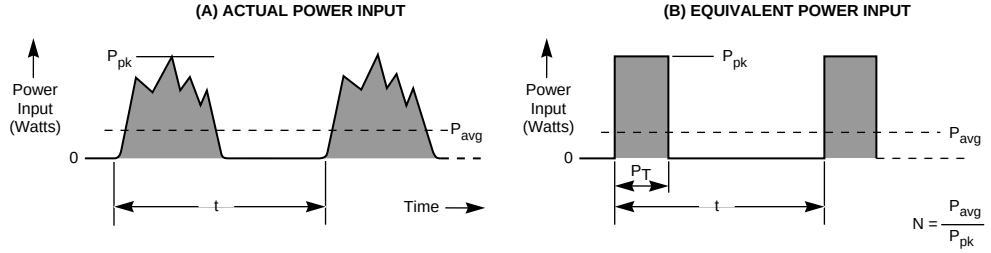


Figure 2.8 Basic Load Current Rating Equations

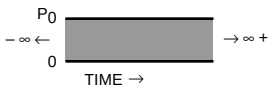
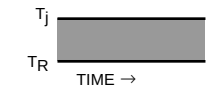
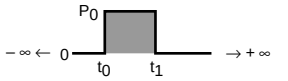
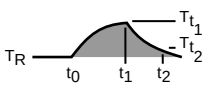
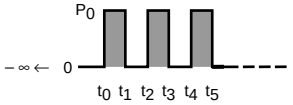
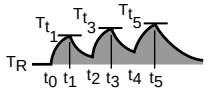
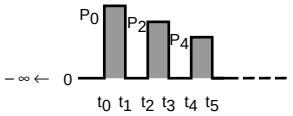
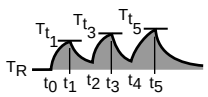
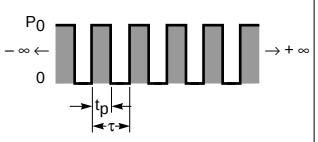
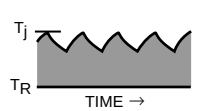
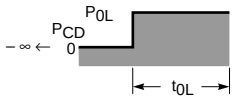
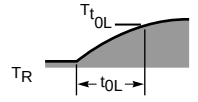
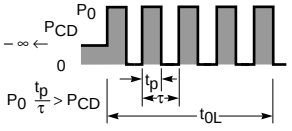
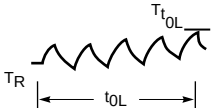
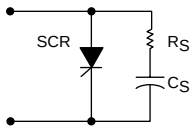
Load Condition	Waveform of Power Loss at Junction	Waveform of Junction Temperature Rise (T_R = Reference Temp.)	Solution for Juction Temperature R_θ= Steady-State Thermal Resistance $R_{\theta(t_1)}$ = Transient Thermal Impedance at Time t_1 $R_{\theta(t_2-t_1)}$ = Transient Thermal Impedance at Time ($t_2 - t_1$), etc.
Continuous Load			$T_j - T_R = P_0 R_\theta$ $P_0 = \frac{T_j - T_R}{R_\theta}$
Single Load Pulse			$T_{t_1} - T_R = P_0 Z_{\theta(t_1)}$ $T_{t_2} - T_R = P_0 [Z_{\theta(t_2)} - Z_{\theta(t_2-t_1)}]$ $P_0 = \frac{T_{t_1} - T_R}{Z_{\theta(t_1)}}$
Short Train of Load Pulses (Equal Amplitude)			$T_{t_1} - T_R = P_0 Z_{\theta(t_1)}$ $T_{t_3} - T_R = P_0[Z_{\theta(t_3)} - Z_{\theta(t_3-t_1)} + Z_{\theta(t_3-t_2)}]$ $T_{t_5} - T_R = P_0[Z_{\theta(t_5)} - Z_{\theta(t_5-t_1)} + Z_{\theta(t_5-t_2)}]$, etc.
Train of Unequal Amplitude Load Pulses			$T_{t_1} - T_R = P_0 Z_{\theta(t_1)}$ $T_{t_3} - T_R = P_0 Z_{\theta(t_3)} - P_0 Z_{\theta(t_3-t_1)} + P_2 Z_{\theta(t_3-t_2)}$ $T_{t_5} - T_R = P_0 Z_{\theta(t_5)} - P_0 Z_{\theta(t_5-t_1)} + P_2 Z_{\theta(t_5-t_2)} - P_2 Z_{\theta(t_5-t_3)} + P_4 Z_{\theta(t_5-t_4)}$
Long Train of Equal Amplitude Load Pulses (Approx. Solution)			$T_j - T_R = P_0[\frac{t_p R_\theta}{\tau} + (1-\frac{t_p}{\tau}) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)}]$ $P_0 = \frac{T_j - T_R}{\frac{t_p R_\theta}{\tau} + (1-\frac{t_p}{\tau}) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)}}$
Overload Following Continuous Duty (Non-Pulsed)			$T_{t_{OL}} - T_R = P_{CD} R_\theta + (P_{OL} - P_{CD}) Z_{\theta(t_{OL})}$ $P_{OL} = \frac{T_{t_{OL}} - T_R - P_{CD} R_\theta}{Z_{\theta(t_{OL})}} + P_{CD}$
Overload Following Continuous Duty (Pulsed) (Approx. Solution)			$T_{t_{OL}} - T_R = P_{CD} R_\theta + P_0 \left\{ [\frac{t_p}{\tau} - \frac{P_{CD}}{P_O}] Z_{\theta(t_{OL})} + (1-\frac{t_p}{\tau}) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)} \right\}$ $P_0 = \frac{T_{t_{OL}} - T_R + P_{CD}(R_\theta - Z_{\theta(t_{OL})})}{\frac{t_p}{\tau} Z_{\theta(t_{OL})} + (1-\frac{t_p}{\tau}) Z_{\theta(\tau+t_p)} - Z_{\theta(\tau)} + Z_{\theta(t_p)}}$

Figure 2.9 RC Snubber Circuit and Recommended Snubber Component Values



Recommended Snubber Circuit Values

Module Current Rating (A)	R_S (Ω)	C_S (μF)
25-60	10	0.1
90-130	10	0.2

Figure 2.10 Circuit Configurations and Critical Parameters for Common Phase Control Applications

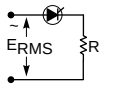
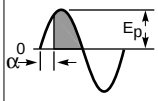
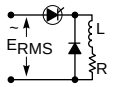
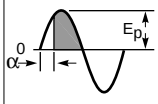
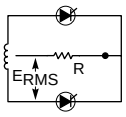
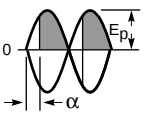
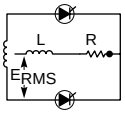
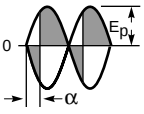
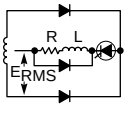
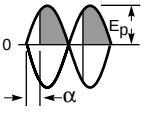
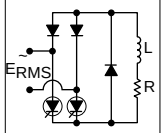
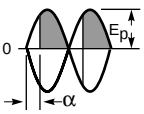
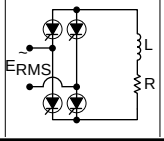
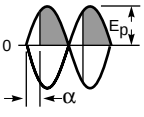
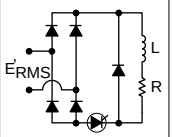
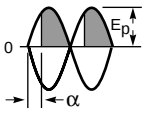
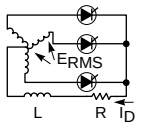
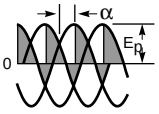
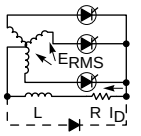
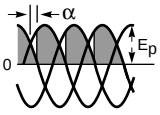
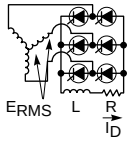
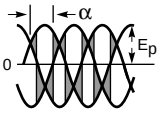
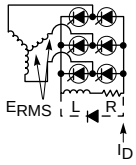
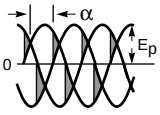
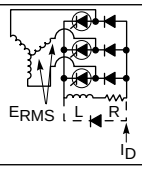
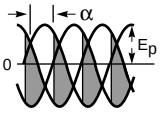
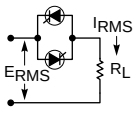
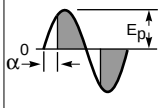
Circuit Notation	Circuit Schematic	Waveforms	Max. SCR Voltage	Peak Reverse Voltage SCR	Peak Reverse Voltage Diode	Max. Load Voltage E_d = Avg. E_a = RMS	Load Voltage with Delayed Firing	Max. Average SCR Current Avg. Amps.	Max. Average SCR Current Cont. Period	Max. Average Diode Current Avg. Amps.	Max. Average Diode Current Cont. Period
1-1-1-H			1.4 E_{RMS}	E_p	—	$E_d = \frac{E_p}{\pi}$ $E_a = \frac{E_p}{2}$	$E_d = \frac{E_p}{2\pi}(1 + \text{Cos}\alpha)$ $E_a = \frac{E_p}{2\sqrt{\pi}}\sqrt{(\pi - \alpha + 1/2\text{Sin } 2\alpha)}$	$\frac{E_p}{\pi R}$	180°	—	—
1-1-1-H With Free-Wheeling Diode			1.4 E_{RMS}	E_p	E_p	$E_d = \frac{E_p}{\pi}$	$E_d = \frac{E_p}{2\pi}(1 + \text{Cos}\alpha)$	Very Ind. Load $\frac{E_p}{2\pi R}$ Conventional $\frac{E_p}{\pi R}$	180°	$0.54\frac{(E_p)}{pR}$	210°
2-1-1-C			2.8 E_{RMS}	$2E_P$	—	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{\pi}(1 + \text{Cos}\alpha)$	$\frac{E_p}{\pi R}$	180°	—	—
2-1-1-C			2.8 E_{RMS}	$2E_p$	—	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{\pi}(1 + \text{Cos}\alpha)$ (I_{dc} = K)	$\frac{E_p}{\pi R}$	180°	—	—
2-1-1-C With Thyristor in D C Circuit			1.4 E_{RMS}	0	2.8 E_{RMS}	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{\pi}(1 + \text{Cos}\alpha)$	$\frac{2E_p}{\pi R}$	360°	$\frac{E_p}{\pi R}$ for 2-1-1-C $\frac{0.5(E_p)}{\pi R}$	180° <180° FWD
Half Control 4-1-1-B and FWD			1.4 E_{RMS}	E_p	E_p	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{\pi}(1 + \text{Cos}\alpha)$	$\frac{E_p}{\pi R}$	180°	$\frac{E_p}{\pi R}$ for 4-1-1-B $\frac{0.26(2E_p)}{\pi R}$	180° <180° FWD
Full Control 4-1-1-B			1.4 E_{RMS}	E_p	—	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{\pi}(1 + \text{Cos}\alpha)$ (I_{dc} = K)	$\frac{E_p}{\pi R}$	180°	—	—

Figure 2.10 Circuit Configurations and Critical Parameters for Common Phase Control Applications (Continued)

Circuit		Waveforms	Max. SCR Voltage	Peak Reverse Voltage		Max. Load Voltage E_d = Avg. E_a = RMS	Load Voltage with Delayed Firing	Max. Average SCR Current		Max. Average Diode Current	
Notation	Schematic			SCR	Diode			Avg. Amps.	Cont. Period	Avg. Amps.	Cont. Period
4-1-1-B With Thyristor and FWD.			1.4 E_{RMS}	E_p	E_p	$E_d = \frac{2E_p}{\pi}$	$E_d = \frac{E_p}{\pi}(1 + \text{Cos}\alpha)$	$\frac{2E_p}{\pi R}$	360°	$\frac{E_p}{\pi pR}$ $\frac{.5E_p}{\pi R}$	180° <180°
3-1-1-Y			2.45 E_{RMS}	2.45 E_{RMS}	—	$E_d = \frac{3\sqrt{3E_p}}{2\pi}$ (I_{dc} = K)	$E_d = \frac{3\sqrt{3E_p}}{2\pi}(\text{Cos}\alpha)$	0.33 I_D	120°	—	—
3-1-1-Y With Free-Wheeling Diode			2.45 E_{RMS}	2.45 E_{RMS}	E_p	$E_d = \frac{3\sqrt{3E_p}}{2\pi}$	$E_d = \frac{3\sqrt{3E_p}}{2\pi}(\text{Cos}\alpha)$ (0<α<30°) $E_d = \frac{3E_p}{2\pi}[1 + \text{Cos}(\alpha + 30°)]$ (30°<α<150°)	0.33 I_D	120°	Size to 0.33 I_D	<120° FWD
6-1-1-B With Full Control			2.45 E_{RMS}	2.45 E_{RMS}	—	$E_d = \frac{3\sqrt{3E_p}}{\pi}$	$E_d = \frac{3\sqrt{3E_p}}{\pi}(\text{Cos}\alpha)$	0.33I_D	120°	—	—
6-1-1-B With Full Control and FWD			2.45 E_{RMS}	2.45 E_{RMS}	2.45 E_{RMS}	$E_d = \frac{3\sqrt{3E_p}}{\pi}$	$E_d = \frac{3\sqrt{3E_p}}{\pi}(\text{Cos}\alpha)$ (0<α<60°) $E_d = \frac{3\sqrt{3E_p}}{2\pi}(1 + \frac{\text{Cos}\alpha}{2} - \frac{3}{2}\text{Sin}\alpha)$ (60°<α<120°)	0.33 I_D	120°	Size to 0.33 I_D	<120° FWD
6-1-1-B Half Control and FWD			2.45 E_{RMS}	2.45 E_{RMS}	2.45 E_{RMS}	$E_d = \frac{3\sqrt{3E_p}}{\pi}$	$E_d = \frac{3\sqrt{3E_p}}{\pi}(1 + \text{Cos}\alpha)$	0.33 I_D	120°	0.33 I_D Size to 0.33 I_D	120° <120° FWD
AC Switch			1.4 E_{RMS}	E_p	—	$E_a = \frac{E_p}{1.4}$	$E_a = \frac{E_p}{\sqrt{2\pi}}\sqrt{(\pi - \alpha + 1/2\text{Sin}\,2\alpha)}$	$\frac{E_p}{\pi R}$	180°	—	—