Powerex, Inc., 200 Hillis Street, Youngwood, Pennsylvania 15697-1800 (412) 925-7272

Darlington Transistor Modules Ratings and Characteristics

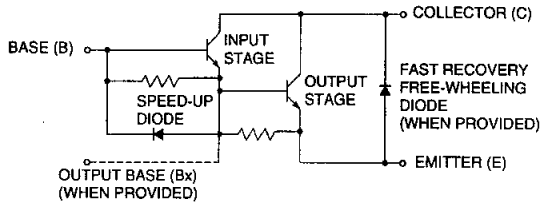
1.0 Transistor Module Construction

The most basic element of a

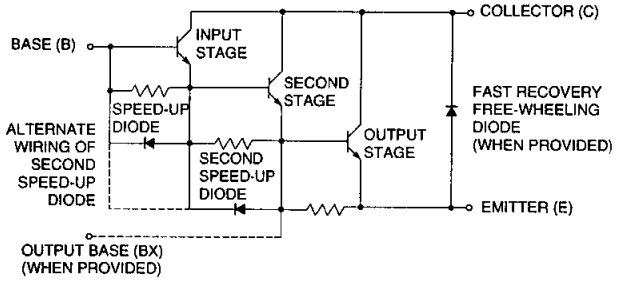
state-of-the-art fine line emitter patterns, resulting in excellent gain and safe operating area performance. High blocking

and molybdenum. This assembly is next soldered to a copper collector electrode along with a free-wheeling diode chip. The

Figure 1.3 Schematic Representation of Darlington Transistor Configurations



(A) DARLINGTON



(B) THEE TRIPLE DARLINGTON

1.1 Darlington Configurations

The basic Darlington configuration is shown schematically in Figure 1.3 (A). The input and output stages, along with their associated base emitter resistors, comprise the transistor chip. Most Powerex modules include discrete fast recovery free-wheeling diodes and speed-up diodes around the input stage as shown in Figure 1.3 (A). Some modules provide a Bx terminal, which is useful when paralleling modules.

At 1000 volts and above, most Powerex modules employ the triple Darlington configuration shown schematically in Figure 1.3 (B). The triple Darlington maintains high gain to allow simple base drive circuits. Both $V_{CE(sat)}$ and $V_{BE(sat)}$ are increased by the triple Darlington configuration.

Again, most Powerex modules include discrete fast recovery free-wheeling diodes. Speed-up diodes are provided around both the input and the second stages. The cathode of the second stage speed-up diode may be connected to the input stage emitter, or to the external base connection. Again, some modules provide a Bx terminal.

1.2 The Device Data Sheet

The proper application of power semiconductors requires an understanding of their maximum ratings and electrical characteristics, information which is presented within the device data sheet. Good design practice employs data sheet limits and not information obtained from small sample lots.

A *rating* is a maximum or minimum value that sets a limit on device capability. Operation in excess of a rating can result in irreversible degradation or device failure. Maximum ratings represent extreme capabilities of a device. They are not to be used as design conditions.

A *characteristic* is a measure of device performance under specified operating conditions expressed by minimum, typical, and/or maximum values, or shown graphically.

Table 1.1 illustrates the major ratings and characteristics of a typical Powerex bipolar Darlington transistor module data sheet. Table 1.2 lists the symbols and definitions of the major device parameters.

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Darlington Transistor Modules
Ratings and Characteristics

Table 1.1 Typical Bipolar Transistor Data Sheet

Absolute Maximum Ratings, T_j = 25 °C unless otherwise specified

Ratings	Symbol	KS621K30	Units
Junction Temperature	T_j	-40 to 150	°C
Storage Temperature	T_{stg}	-40 to 125	°C
Collector-Emitter Sustaining Voltage, V_{BE} = -2V	$V_{CEV(sus)}$	1000	Volts
Collector-Base Voltage	V_{CBO}	1000	Volts
Emitter-Base Voltage	V_{EBO}	7	Volts
Collector-Emitter Voltage	V_{CEV}	1000	Volts
Continuous Collector Current	I_C	300	Amperes
Diode Forward Current	I_{FM}	300	Amperes
Continuous Base Current	I_B	16	Amperes
Diode Surge Current	I_{FSM}	3000	Amperes
Power Dissipation	P_t	1980	Watts
Max. Mounting Torque M6 Terminal Screws (E, C)	–	26	in.-lb.
Max. Mounting Torque M4 Terminal Screws (B, Bx)	–	12	in.-lb.
Max. Mounting Torque M6 Mounting Screws	–	26	in.-lb.
Modular Weight (Typical)	–	17	oz.
	–	470	Grams
V Isolation	V_{RMS}	2500	Volts

Electrical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics		Symbol	Test Conditions	Min.	Typ.	Max.	Units
Collector Cutoff Current		I_{CEV}	V_{CE} = 1000V, V_{BE} = -2V	–	–	4	mA
			V_{CE} = 1000V, V_{BE} = -2V, T_C = 125°C	–	–	40	mA
Emitter Cutoff Current		I_{EBO}	V_{EB} = 7V	–	–	800	mA
DC Current Gain		h_{FE}	I_C = 300A, V_{CE} = 2.8V	75	–	–	–
			I_C = 300A, V_{CE} = 5.0V	100	–	–	–
Diode Forward Voltage		V_{FM}	I_{FM} = 300A	–	–	1.8	Volts
Collector-Emitter Saturation Voltage		$V_{CE(sat)}$	I_C = 300A, I_B = 6.0A	–	–	2.5	Volts
Base-Emitter Saturation Voltage		$V_{BE(sat)}$	I_C = 300A, I_B = 6.0A	–	–	32.5	Volts
Resistive	Turn-on	t_{on}	V_{CC} = 600V	–	–	3.0	µs
Load	Storage Time	t_s	I_C = 300A	–	–	15	µs
Switch Times	Fall Time	t_f	I_{B1} = 4A, I_{B2} = -6A	–	–	3.0	µs

Thermal and Mechanical Characteristics, T_j = 25 °C unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Thermal Resistance, Case-to-Sink	$R_{\theta(c-s)}$	–	–	–	0.04	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta(j-c)}$	Transistor Part	–	–	0.063	°C/W
Thermal Resistance, Junction-to-Case	$R_{\theta(j-c)}$	Diode Part	–	–	0.3	°C/W

Table 1.2 Symbols and Definitions of Major Bipolar Transistor Module Parameters

Symbol	Parameter	Definition/Description
$V_{CEV(sus)}$	Collector-Emitter Sustaining Voltage	With a reverse biased base-emitter, it is the sustained collector-emitter voltage for a specified collector current. (Measurement is made using a clamped inductive load circuit).
V_{CEV}	Collector-Emitter Voltage	With a reverse biased base-emitter, indicates maximum DC voltage between the collector and emitter.
V_{CBO}	Collector-to-Base Voltage	With an open emitter, indicates maximum DC voltage between the collector and base.
V_{EBO}	Emitter-to-Base Voltage	With an open collector, indicates maximum DC voltage between the emitter and base.
I_C	Collector Current	Maximum continuous collector current.
I_B	Base Current	Maximum continuous base current.
P_T	Power Dissipation	Maximum power dissipation at T_C = 25°C.
I_{CBO}	Collector Cut Off Current	With an open emitter, indicates the collector current when a specified reverse voltage is applied between the emitter and base.
I_{EBO}	Emitter Cut Off Current	With an open collector, indicates the emitter current when a specified reverse voltage is applied between the emitter and base.
I_{CEV}	Collector Cut Off Current	With a specified reverse voltage between the base and emitter. Indicates collector current when a specified voltage is applied between the collector and emitter.
h_{FE}	DC Forward Current Transfer Ratio	With a specified voltage and current, indicates the ratio between DC output current and DC input current (emitter grounded).
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	Under specified base and collector current conditions, indicates the DC voltage between the collector and emitter (emitter grounded).
$V_{BE(sat)}$	Base-Emitter Saturation Voltage	Under specified base and collector current condition, indicates the DC voltage between the base and emitter.
t_{on}	Turn-on Time	Indicates the time between the point that the rising edge of a pulse input has risen to 10% of its peak amplitude, and the rising edge of the output pulse has risen to 90% of its peak amplitude.
t_s	Storage Time	Indicates the time between the point where the falling edge of a pulse input has fallen to 90% of its peak amplitude, and the falling edge of the output pulse has fallen to 90% of its peak amplitude.
t_f	Fall Time	Indicates the time taken by a pulse output to fall from 90% to 10% of its peak amplitude.
I_{FSM}	Diode Surge Current	Maximum sinusoidal 60Hz single cycle diode surge current.
I_F	Diode Forward Current	Maximum continuous diode current.
V_{FM}	Diode Forward Voltage	Under specified diode forward current condition, indicates the DC voltage across diode anode-cathode.
V_{RMS}	V Isolation	Maximum AC RMS voltage withstand capability from isolated base plate to all terminals connected together.
$R_{\theta(j-a)}$	Junction-to-Ambient Thermal Resistance	The steady state thermal resistance between the junction and ambient.
$R_{\theta(j-c)}$	Junction-to-Case Thermal Resistance	The steady state thermal resistance between the junction and surface of the case.
$R_{\theta(c-s)}$	Contact Thermal Resistance	The steady state thermal resistance between the surface of the case and the heatsink mounting surface.
$Z_{\theta(j-a)}$	Junction-to-Ambient Transient Thermal Impedance	The transient thermal impedance between the junction and ambient.
$Z_{\theta(j-c)}$	Junction-to-Case Transient Thermal Impedance	The transient thermal impedance between the junction and the surface of the case.

Table 1.2 Symbols and Definitions of Major Bipolar Transistor Module Parameters (continued)

Symbol	Parameter	Definition/Description
$Z_{\theta(j\text{-}s)}$	Junction-to-Sink Transient Thermal Impedance	The transient thermal impedance between the junction and the heatsink mounting surface.
T_A	Ambient Temperature	When used in the natural cooling or forced air cooling it is the temperature of the surrounding atmosphere of a device which is dependent on geographical location and season, and is not influenced by heat dissipation of the device.
T_S	Sink Temperature	The temperature at a specified point on the device heatsink.
T_C	Case Temperature	The temperature at a specified point on the device case.
T_j	Junction Temperature Rating	The device junction temperature rating. Indicates the maximum and minimum allowable operation temperatures.
T_{stg}	Storage Temperature Rating	The device storage temperature (with no electrical connection). Indicates the maximum and minimum allowable temperatures.
—	Mounting Torque Mounting Screw	The maximum allowable torque specification for mounting a device to a heatsink with the specified mounting screw.
—	Mounting Torque Terminal Screw	The maximum allowable torque specification for tightening the specified electrical terminal screws.

1.3 Voltage Ratings

The specified voltages are defined by the maximum rating voltages that can be applied between collector, emitter and base. The transistor ***maximum voltage ratings should never be exceeded.*** Exceeding the maximum voltage ratings can be detrimental to the transistor, resulting in instant failure or a decrease in the life of the device.

1.3.1 Collector-emitter Breakdown Voltages

It is the collector base junction which supports the applied voltage during the off-state of a transistor. Because of the gain of the transistor, the collector-emitter breakdown characteristics are a function of base-emitter bias as shown in Figure 1.4.
The base open condition, V_{CEO}, is the most limiting. At large currents, after breakdown, the voltage drops to a lower sustaining voltage, $V_{CEO(sus)}$. This voltage determines the lowest value of rated collector emitter voltage.

1.3.2 Emitter-base Breakdown Voltage

The emitter base voltage rating, V_{EBO}, is a rating specified at low values of I_{EB} and with the collector open. The V_{EBO} rating is established to prevent avalanching the emitter base junction of the transistor. Repetitive emitter base avalanche may result in degradation of low current h_{FE}.

1.4 Safe Operating Areas

Safe operating areas define the allowable values of collector current and collector-emitter voltage under which a transistor may be safely operated.

1.4.1 Forward Bias Safe Operating Area (FBSOA)

Forward Bias Safe Operating Area (FBSOA) curve defines the ability of a power transistor to dissipate power when its base is forward biased. Figure 1.5 illustrates an FBSOA curve for a 300 amp, 1000 volt Darlington transistor.

Figure 1.4 Collector-emitter Breakdown Voltage Characteristics

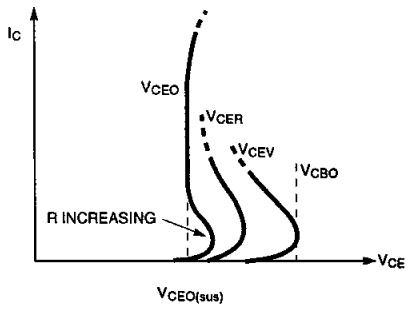
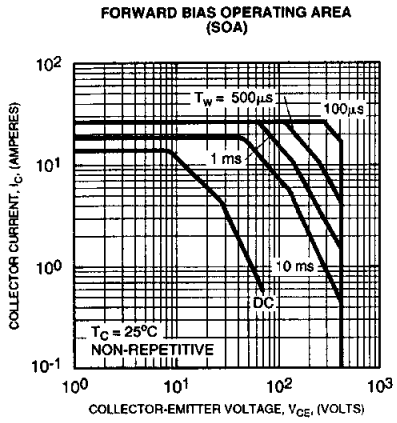


Figure 1.5 Typical Darlington Transistor Forward Bias Safe Operating Area (FBSOA) Curve



The FBSOA curve contains limits for both continuous (DC) and pulsed operating conditions. The upper horizontal line defines the maximum allowable current, regardless of power dissipation, beyond which operation becomes unsafe because of possible damage to bonding wires to the transistor chip and/or to the package. Next, the curve slopes downward in the constant power (V_{CE} • I_C) region. This region arises due to the device's thermal limitation defined by the thermal resistance and the maximum junction temperature plotted on a log-log scale, the FBSOA thermal limit is a straight line with a -1 slope.

Power transistors are very sensitive to voltage stress. This is the reason for the second break in the FBSOA curve. The second breakdown ($I_{S/B}$) limit lies below the FBSOA thermal limit and refers to the maximum current allowed prior to occurrence of forward second breakdown. Operation at currents greater than the maximum limit in the $I_{S/B}$ region will cause destruction of the transistor as a result of localized heating. The second breakdown portions of the FBSOA curve is that portion in which allowable power dissipation is decreasing with increased voltage. This is because, as voltage rises current is focused at the edges of the emitter, increasing current density and decreasing the area in which power dissipation occurs.

The limit at the right hand side of the FBSOA curve is $V_{CEO(sus)}$. Operation above $V_{CEO(sus)}$ with forward base current will result in instantaneous destruction of the transistor.

1.4.2 Forward Bias Safe Operating Area Derating

Powerex Darlington Transistor modules are designed for switching applications. They are usually not used in linear applications. In circuits which subject a transistor to both voltage and current simultaneously, leading to high power dissipation, the FBSOA curve must be closely examined. Proper use of the FBSOA curve requires adherence to both thermal and second breakdown limits.
The 25°C FBSOA curves must be derated for actual operating conditions. The derating curves indicate how much to derate the current at a constant voltage in the dissipation limited and forward second breakdown limited portions of the FBSOA curves. The curves do not derate the specified value of $I_{C(max)}$.

The procedure for derating FBSOA is:

1. Determine the maximum allowable power by reading current off the FBSOA curve at the given voltage.

2. Determine the Second Breakdown Derating factor from the Derating curve to derate maximum power at given temperature. Use this derating factor on the maximum power determined in Step 1 to determine the derated maximum allowable power.

3. Determine the derated maximum allowable current by dividing the given voltage into derated maximum allowable power found in Step 2.

4. Check to make sure the thermal limit is not exceeded.

Figure 1.6 illustrates an FBSOA Derating Curve and includes examples of its use.

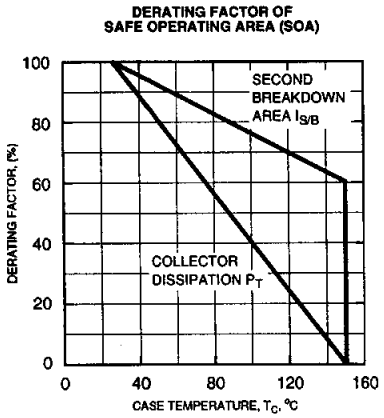
1.4.3 Reverse Bias Safe Operating Area (RBSOA)

Reverse Bias Safe Operating Area (RBSOA) indicates the ability of a transistor to handle voltage and current stress with its base emitter reverse biased. The RBSOA curve provides the boundary for allowable turn-off load lines. RBSOA is measured in an inductive switching circuit using a collector emitter voltage clamp as shown in Figure 1.7.

Figure 1.8 illustrates a typical RBSOA curve. The curve

represents the peak collector emitter voltage and collector current limits for the device. These are instantaneous limits. The turn-off load line should not go outside the RBSOA curve. The amount of reverse base current used has a strong effect upon RBSOA performance. Higher reverse base current reduces the RBSOA capability because the higher base current creates an internal voltage that causes current crowding under the center of the emitter fingers.

Figure 1.6 Forward Bias Safe Operating Area Derating Curve and Examples of its use



$I_{S/B}$ Derating Factor = -0.32 T + 108
P_T Derating Factor = -0.8 T + 120
T = Case Temperature in °C.
Equations valid over 25°C to 150°C range.

Thermal Limitations Example
Assume it is desired to operate the KS621K30 at 20 volts with a case temperature of 90°C.

1. Current from the FBSOA curve at 20 volts = 99 amps, yielding 1980 watt maximum power.
2. From Second Breakdown Derating Curve, $I_{S/B}$ derating at 90°C = 78%. Thus derated maximum power = 1980 • 0.78 = 1544 watts.
3. Maximum allowable current at 90°C case temperature = 1544/20 = 77 amps.
4. From Collector Dissipation Curve, thermal derating = 48% at 90°C. Thus maximum power = 1980 • 0.48 = 950 watts and maximum current = 950/20 = 47.5 amps. In this example the thermal derating is the limiting factor on device current.

Second Breakdown Limitation Example
Assume it is desired to operate the KS621K30 at 150 volts with a case temperature of 90°C.

1. Current from the FBSOA curve at 150 volts = 4.3 amps, yielding 645 watts maximum power.
2. From Second Breakdown Derating Curve, $I_{S/B}$ derating at 90°C = 78%. Thus derated maximum power = 645 • 0.78 = 503 watts.
3. Maximum allowable current at 90°C case temperature = 503/150 = 3.4 amps.
4. From Collector Dissipation Curve, thermal derating = 0.48% at 90°C. Thus maximum power = 1980 • 0.48 = 950 watts and maximum current = 950/150 = 6.3 amps. In this example the second breakdown derating is the limiting factor on device current.

1.5 On Characteristics

Powerex data sheets provide a number of characteristic curves that apply to the transistor in the on or saturated condition.

Figure 1.7 $V_{CE(sus)}$, Reverse Bias Safe Operating Area (SOA) Measurement Circuit and Waveform

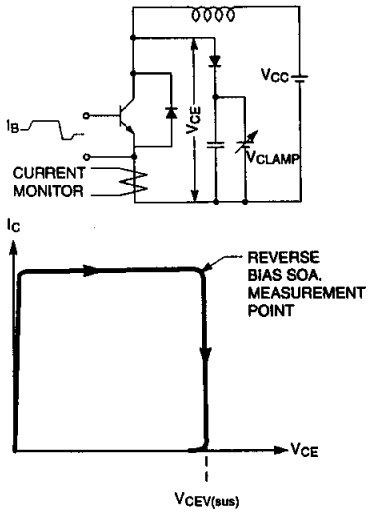


Figure 1.8 Typical Reverse Bias Safe Operating area (SOA) Curve

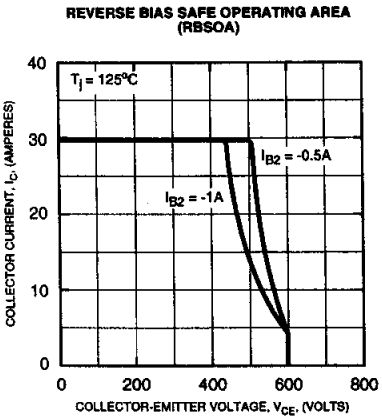


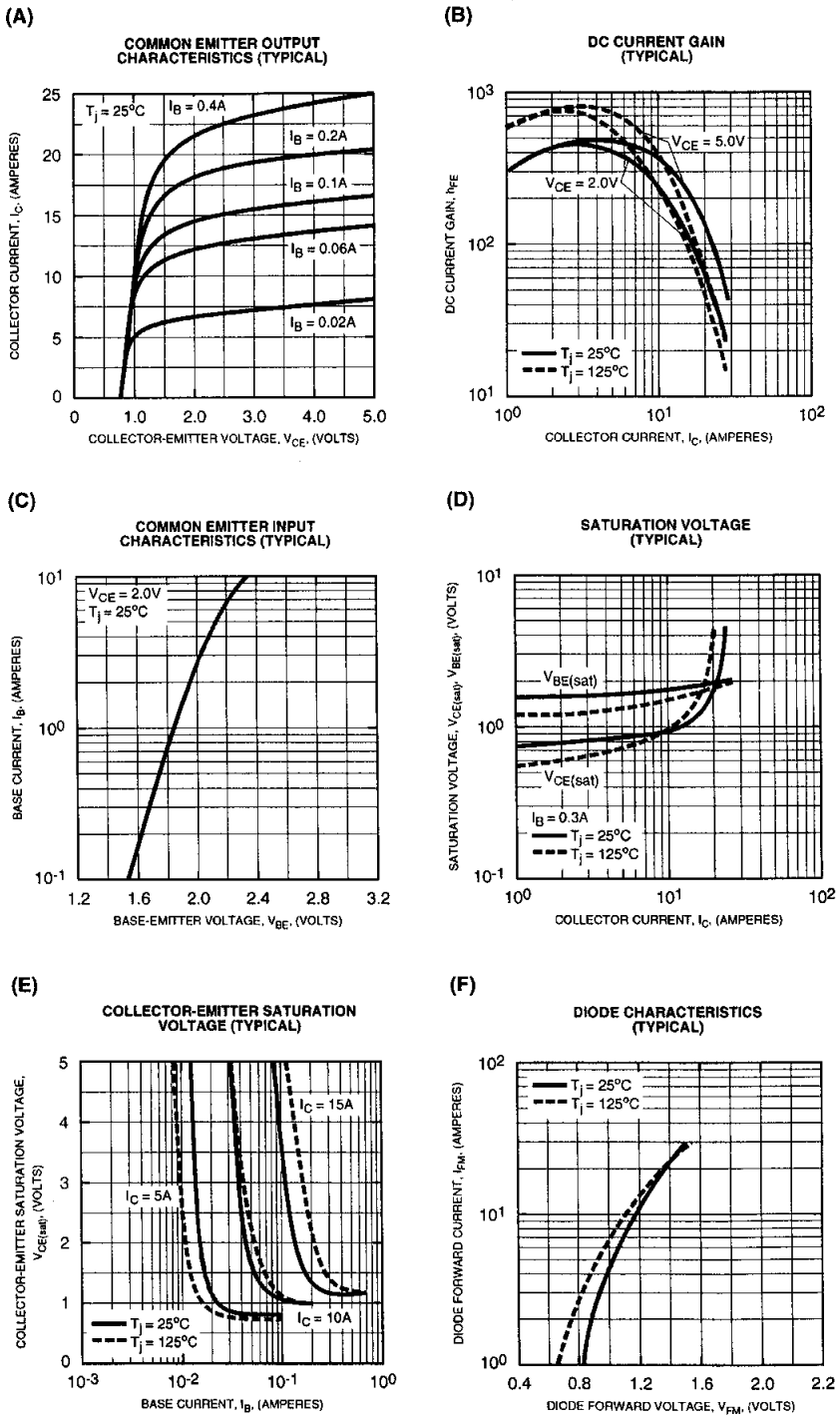
Figure 1.9 (A) illustrates an output characteristic curve which plots the collector emitter voltage vs. collector current for different values of base current. The region in which the curves converge into a single vertical line represents hard saturation of the transistor. Hard saturation provides the lowest achievable $V_{CE(sat)}$, as further increases in base current will not decrease $V_{CE(sat)}$.

To the right of the hard saturation region, the transistor operates in the quasi-saturation region. In quasi-saturation, for a fixed base current, the collector current decreases as collector emitter voltage decreased, which means the gain decreases. At higher collector emitter voltages, the curves become horizontal with little change in collector current for a fixed base current as collector emitter voltage changes. This linear region of the output characteristic is not shown on the data sheet curves.

For efficiency, it is desirable to control large collector currents with small values of base current. The common emitter current gain, h_{FE}, is the ratio of collector current to base current at a fixed V_{CE}.

Figure 1.9 (B) shows a typical data sheet curve for Gain vs. Collector Current as a function of V_{CE} and temperature. Gain increases with voltage and increases with temperature at low currents. At high currents, gain decreases with temperature. Gain hold-up is defined as the change in h_{FE} as a function of collector current. Powerex Darlington Transistors have excellent gain hold-up to

Figure 1.9 Typical On-state Transistor Characteristics



rated current allowing low values of $V_{CE(sat)}$ with reasonable forced gains.

Figure 1.9 (C) illustrates an input characteristic curve which plots base emitter voltage, V_{BE}, as a function of base current, I_B, at a fixed collector emitter voltage, V_{CE}. This curve is used when designing base drive circuits. Darlington transistors, especially triple Darlingtons, have significant base emitter voltages which must be allowed for when choosing drive circuit source voltage.

Figure 1.9 (D) and (E) illustrate saturation voltage curves. The saturation voltages are specified as a function of base current, collector current, and temperature. Saturation voltages are important in calculating device power dissipation.
For transistor modules which include integral fast recovery free-wheeling diode(s) a forward voltage vs. forward current curve such as Figure 1.9 (F) is provided.

1.6 Switching Characteristics

The switching times of power transistors are measured with respect to the collector current. This is because in power switching the load is generally inductive and the collector emitter voltage waveform is circuit dependent.

Figure 1.10 shows the switching time curves provided on Powerex data sheets and shows the switching time test circuit. Switching time measurements are made using a resistive load to insure test repeatability. For inductive switching, the switching times are shorter than those for resistive switching. Note the reduction in storage and turn-off time obtained by increasing the reverse base current I_{B2}.

For transistor modules which include integral fast recovery free-wheeling diode(s), the diode surge current ratings and reverse recovery characteristics are provided on curves such as illustrated in Figure 1.11. The diode reverse recovery is characterized in an inductive switching circuit as shown in Figure 1.11.

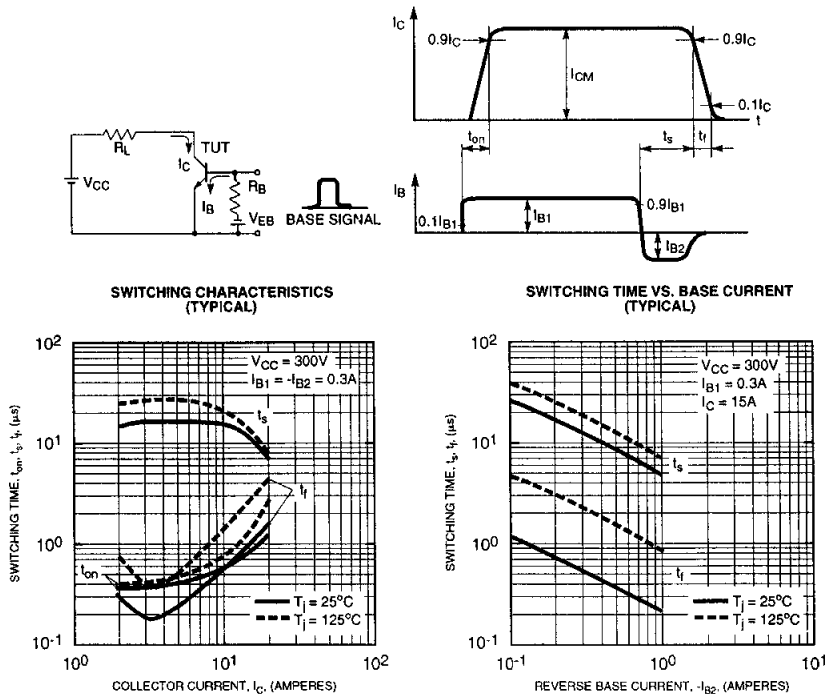
1.7 Power Dissipation and Thermal Ratings

Successful application of power transistors requires adherence to power dissipation and thermal ratings. Transistor failure rate is directly proportional to junction temperature. Derating junction temperature below data sheet maximum is recommended to enhance reliability.

1.7.1 Power Dissipation vs. Temperature

The maximum power dissipation in Watts is specified at a case temperature of 25°C. If the case temperature is higher than 25°C, the derating curve shown in Figure 1.12 must be used. Total power dissipation, or losses, dissipated in a transistor consist of off-state, conduction, and drive power dissipation.

Figure 1.10 Switching Characteristics



1.7.2 Thermal Resistance

Temperature calculations are simplified by using thermal resistance concepts. The flow of heat through a thermal path as a result of power dissipation is analogous to the flow of current through a conductive path as a result of a voltage source. Hence, knowing the power being dissipated in a device, and the ambient temperature, the resulting junction temperature can be calculated using the total thermal resistance and the following equation:

$$T_j = T_A + P_T \bullet R_{\theta(j\text{-}s)}$$

where:

$R_{\theta(j\text{-}a)}$ = Total thermal resistance junction-to-ambient (°C/Watt)
P_T = Total power dissipation (Watts)
T_j, T_A = Junction, ambient temperature (°C)

The total thermal resistance is given by:

$$R_{\theta(j\text{-}a)} = R_{\theta(j\text{-}c)} + R_{\theta(c\text{-}s)} + R_{\theta(s\text{-}a)}$$

where:

$R_{\theta(j\text{-}c)}$ = Junction-to-case thermal resistance specified on data sheet (°C/Watt)
$R_{\theta(c\text{-}s)}$ = Lubricated case-to-sink thermal resistance specified on data sheet (°C/Watt)
$R_{\theta(s\text{-}a)}$ = Sink-to-ambient thermal resistance (°C/Watt)

Figure 1.11 Diode Surge and Reverse Recovery Characteristics and Test Circuit

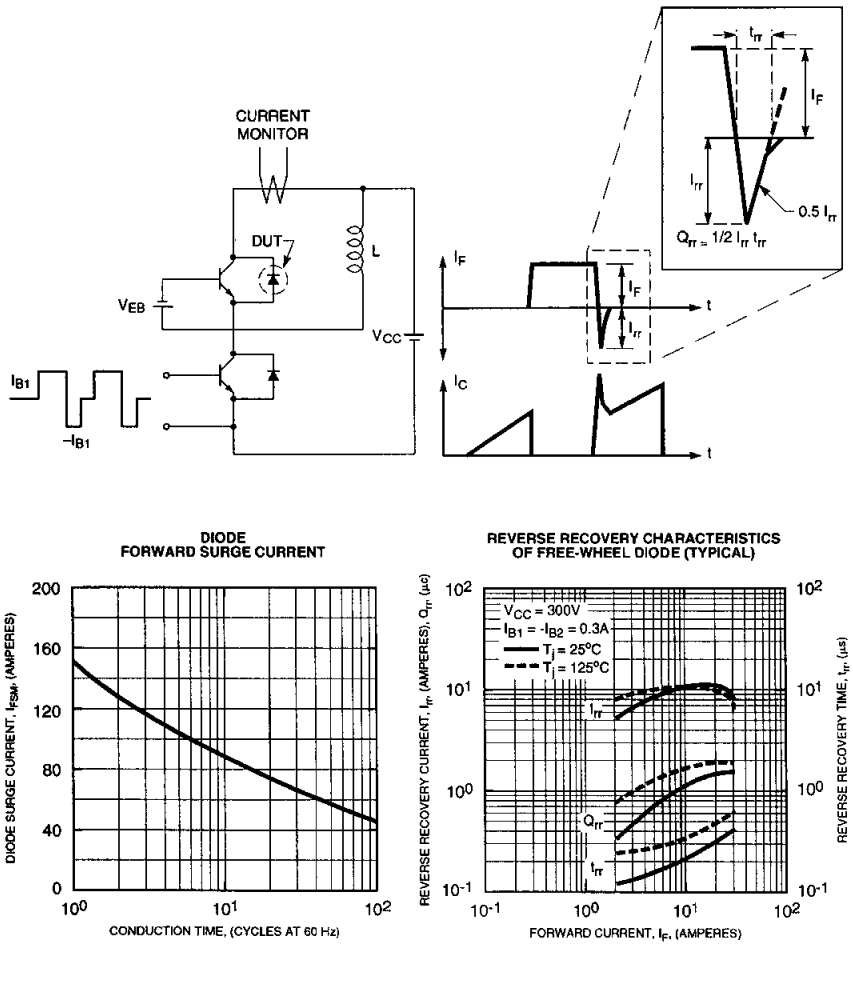
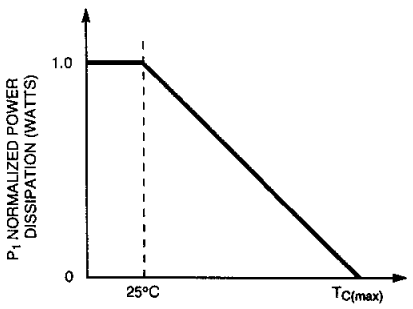


Figure 1.12 Power Dissipation Thermal Derating Curve.



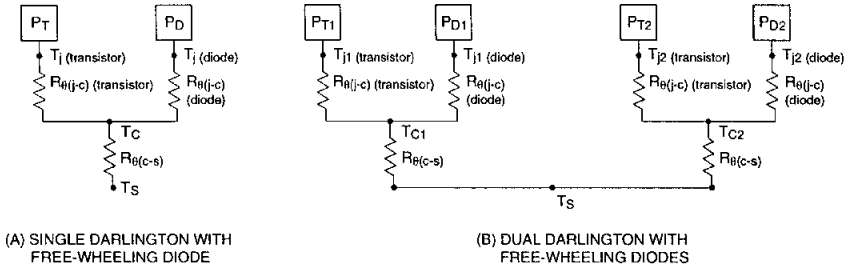
The thermal resistance ($R_{\theta(j-c)}$) specified for a transistor is always a maximum value, with a safety margin included to allow for production variations from lot to lot. The interface case-to-sink thermal resistance ($R_{\theta(c-s)}$) can be significant and the data sheet value specified is for a baseplate properly lubricated with thermal compound.

Figure 1.13 provides the thermal resistance models for both single and dual Darlington modules with free-wheeling diodes. Note that $R_{\theta(c-s)}$ value specified on the device data sheet for a dual Darlington module is applied per half module.

1.7.3 Transient Thermal Impedance

For short or low duty power pulses, using the steady state thermal resistance will give conservative junction temperatures. In addition, using the average value of power dissipation will underestimate the peak junction temperature. The solution is use of the transient thermal impedance curves (Figure 1.14 illustrates typical transient thermal impedance curves). For a power device subjected to single or very low duty cycle, short duration power pulses, the maximum allowable power dissipation during the transient period can be substantially greater than the steady state dissipation capability.

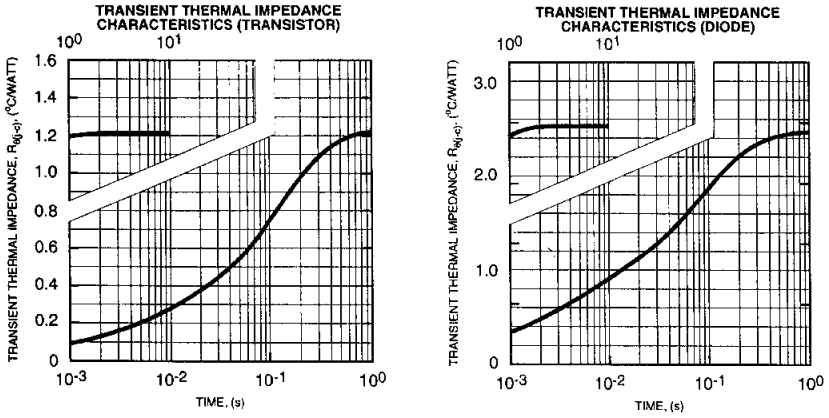
Figure 1.13 Transistor Module Thermal Resistance Models



(A) SINGLE DARLINGTON WITH FREE-WHEELING DIODE

(B) DUAL DARLINGTON WITH FREE-WHEELING DIODES

Figure 1.14 Transient Thermal Impedance Curves



The peak voltages across the transistor must be minimized. Line filters and/or voltage snubbers/clamps must be used on the DC rail to eliminate or, at least, minimize all transients. The maximum transient voltage across a transistor is usually the turn-off voltage spike shown in Figure 2.2.

This spike of voltage during turn-off can be reduced, but it cannot be totally eliminated. The spike voltage is reduced by minimizing the parasitic circuit and wiring inductance, and by using turn-off voltage snubbers. Adding voltage snubbers/clamps directly across the DC rail near the transistors will reduce the spike.

Voltage safety margin is defined as the difference between the rated transistor voltage and the peak value of the rectified AC, (or rail), voltage plus the maximum spike voltage. Voltage safety margin is dependent on the circuit and especially the snubbing and voltage clamping. The following voltage safety margins are suggested:

when:

$V_{CEO(sus)}/V_{CEV}$ =
600 volts or less, use a
50 volt safety margin.

or when:

$V_{CEO(sus)}/V_{CEV}$ =
700 to 1200 volts, use a
100 volt safety margin.

The load line during turn-on must always be within the FBSOA curve and during turn-off within the RBSOA curve. The circuit load line also determines when to use the $V_{CEO(sus)}$ rating or the V_{CEV} rating.

For example, when using a current and voltage snubber as shown in Figure 2.3, the transistor safety margin would be calculated from the maximum V_{CEV} rating. If a transistor which is rated at V_{CEV} = 1000 volts is used, then 900 volts would be the maximum peak rail voltage, including turn-off spike voltage, resulting in a 100 volt safety margin. The collector current should be less than the rated leakage current, usually less than 10 mA at the $V_{CEO(sus)}$ rating, with the voltage increasing to V_{CEV} minus 100 volts while maintaining this low leakage current level.

Although the RBSOA curve indicates that turn-off can be accomplished with higher collector currents between the $V_{CEO(sus)}$ and V_{CEV} voltages, keeping the collector current below the 10 mA level during this period will result in better reliability because the transistors are not heavily stressed in this turn-off mode. At turn-on, the inductor in the turn-on snubber of Figure 2.3 supports the rail voltage keeping the transistor within its FBSOA curve.

Figure 2.3 Snubbed Load Line, Turn-on and Turn-off to 900 Volt using a 1000 Volt Transistor

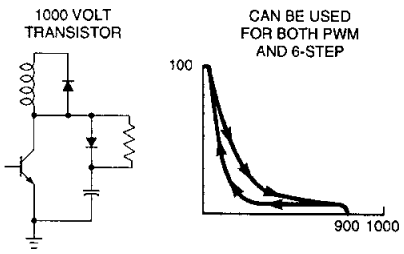
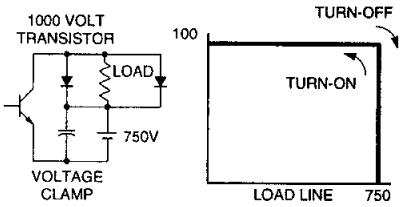


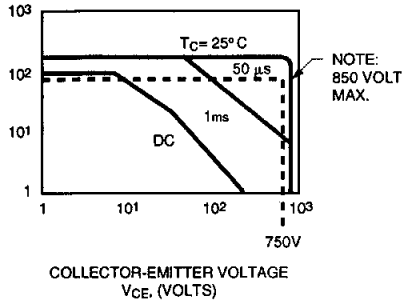
Figure 2.4 Turn-on Load Line, PWM Operation Using a 1000 Volt Transistor



As a second example, the load line for a PWM switching circuit is shown in Figure 2.4. As the transistor is pulsing on and off at a high duty cycle, there is a current flowing in a free-wheeling diode during the off period. When the transistor is on, the sudden transfer of current from the free-wheeling diode to the transistor gives the transistor a turn on load line that is very similar to a capacitive load, i.e., the current rises to its maximum before the voltage falls. Since all circuits are slightly inductive during turn-off, the turn-off load line follows the normal inductive load line, that is, the voltage rises to its maximum before the current begins to fall to zero.

Figure 2.5 continues this example with the load line drawn on the FBSOA curve. This FBSOA curve is for the KS221K10 Darlington transistor which is rated for 1000 volts $V_{CEV(sus)}$ and I_C =100 amps. Since there is no turn-on snubber in this example, to keep the load line within the FBSOA curve, voltage safety margin must be calculated based upon the $V_{CEO(sus)}$ rating and not the V_{CEV} rating. Note that although this transistor is rated for V_{CEV} = 1000 volts, the FBSOA curve is terminated at 850 volts.

Figure 2.5 Turn-on Load Line Superimposed on Forward Bias Safe Operating Area Curve



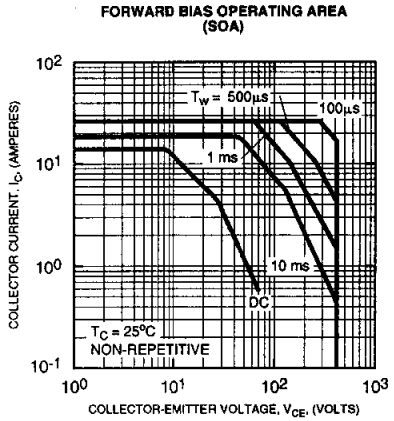
This voltage is the $VC_{EO(sus)}$ rating. The load line drawn here is 750 volts and with the addition of the 100 volt safety margin, the result is equal to the 850 volts $V_{CEO(sus)}$ rating of this transistor.

2.2 Current Ratings

Although the maximum voltage ratings should never be exceeded, exceeding the maximum collector current can be done safely for certain conditions. Figure 2.6 is the FBSOA curve for the KS621K30. For the DC curve, the maximum current is limited to 300 amps and therefore, the RMS current limit is 300 amperes. The internal transistor wires are the limiting factor.

The 600 ampere maximum current limit is set on the one millisecond curve and according to JEDEC guidelines, the transistor must be capable of operating with one millisecond pulses at 50% duty cycle. It is possible to operate this transistor with a smaller pulse, less than 50% duty cycle and not exceed the RMS bonding wire limit and also not exceed the maximum

Figure 2.6 Forward Bias Safe Operating Area Curve Provides Device Current Ratings



junction temperature. Therefore, it is safe under certain conditions to exceed the maximum collector current ratings.

2.3 Base Drive

The factors which determine the choice of forward base current, I_{B1}, are the gain, saturation voltage, switching speed and short circuit capability.The lower limit of I_{B1} is determined by the gain of the the device. To minimize conduction losses, it is desirable to increase I_{B1} to lower $V_{CE(sat)}$. The practical upper limitation on I_{B1} occurs when further increases of I_{B1} do not significantly reduce $V_{CE(sat)}$ at the maximum operating collector current, i.e. hard saturation. Increasing I_{B1} has the disadvantages that storage time is lengthened and short circuit capability is compromised.

The choice between operating in hard saturation or quasi-saturation depends upon operating frequency. At low frequencies, conduction losses dominate favoring operation in hard saturation. At higher frequencies, quasi-saturation operation provides improved switching performance. The baker clamp circuit and proportional transformer drive are two popular circuits for quasi-saturation operation.

When using the transistor in a switching mode the forward base current is generally selected by the following equation.

$$I_{B1} = (1.5 \text{ to } 2.0) \bullet (I_C/h_{FE})$$

In this equation, h_{FE} is the minimum gain specification at the desired operating $V_{CE(sat)}$.

The open circuit voltage of the forward base drive circuit must be sufficient to overcome the $V_{BE(sat)}$ which can be in the 3 or 4 volt range for triple Darlingtons.

The switching performance of power Darlingtons depends on a correctly shaped base drive circuit. Turn-on depends on the rise time and magnitude of I_{B1}. Turn-on time and turn-on switching losses can be significantly reduced by using a high rise time, high initial magnitude base current, i.e. base peaking. Base peaking also reduces the dynamic saturation effect, (discussed later in power dissipation section). Circuits which employ turn-on snubbers that limit turn-on di/dt do not benefit from base peaking. Base peaking is also undesirable in an application that could turn on into a short circuit.

For high frequency operation, turn-off time should be as short as possible to minimize circuit dead time and reduce turn off switching losses. Reduction of storage and current fall times can be obtained by increasing the magnitude of the reverse base drive current, I_{B2}.

However, too high a value of I_{B2} can cause current fall time to increase. Thus, hard turn-off, i.e. switching the base emitter directly to a stiff reverse voltage source is not recommended. Increasing I_{B2} has the disadvantage that the device RBSOA capability is reduced.

When using the transistor in a switching mode, I_{B2} is generally made equal in magnitude to I_{B1} unless limited to a lesser value by the RBSOA curve. A reverse base to emitter voltage of 5 volts is recommended.

Figure 2.7 illustrates the typical base drive current waveform recommendation. As noted above, this waveform is not optimum for all situations.

Figure 2.8 provides an example of a basic drive circuit for a Darlington transistor. A complete base drive circuit will often include extra circuits such as desaturation monitoring, overcurrent shutdown, bias supply undervoltage, and minimum/maximum on/off time circuits.

One aspect of base drive design often overlooked by beginners is provision for fail safe operation. A well designed base drive circuit will always default to an off-bias condition in the absence of a control signal and it will not allow an on condition until bias power supplies are in a stable condition with sufficient voltage to supply adequate base current to the power transistor. Note in Figure 2.8 that a forward base current cannot be supplied until a control current is supplied to the optocoupler illustrating the principle of fail safe design.

Figure 2.7 Typical Recommended Base Drive Current Waveform

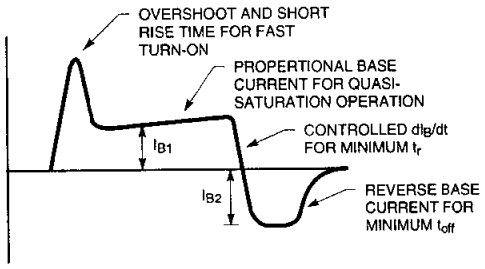
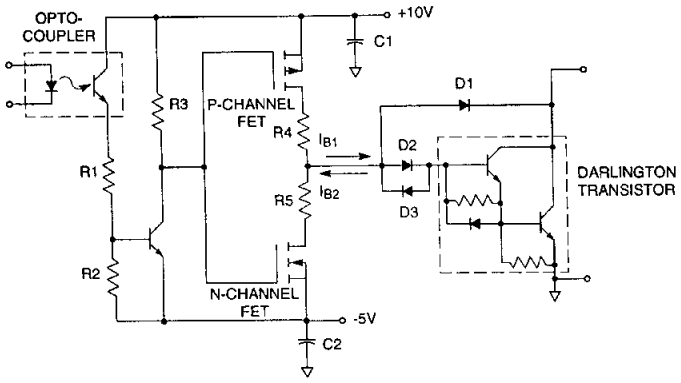
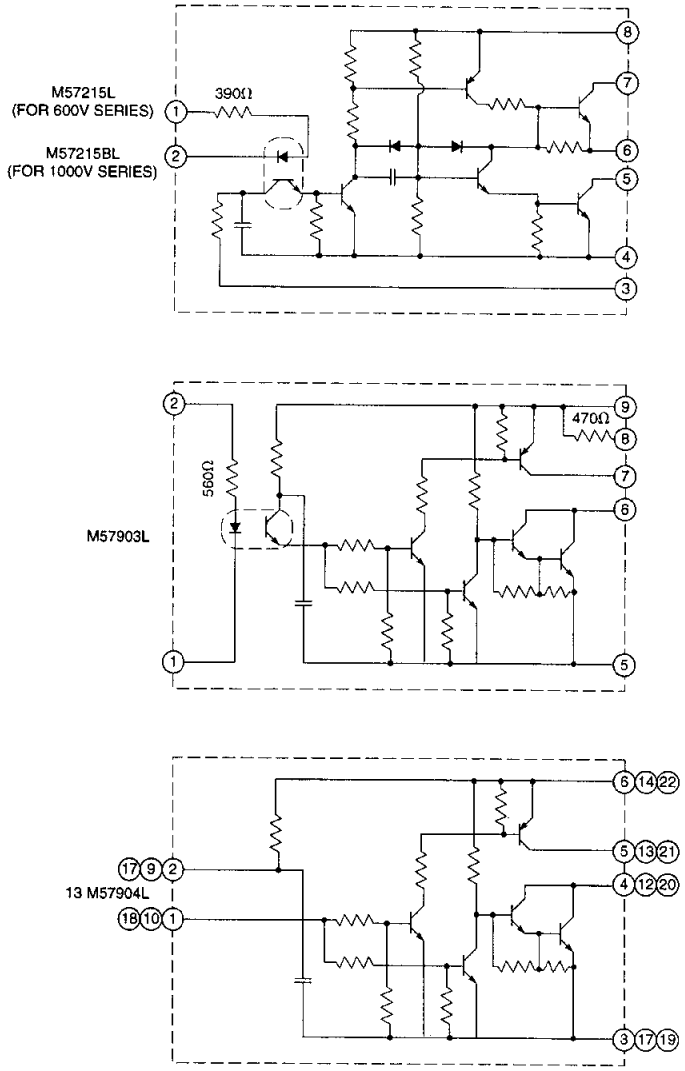


Figure 2.8 Typical Base Drive Circuit for Power Darlingtons



D1 & D2- BAKER CLAMP DIODES
D3- REQUIRED TO SHUNT I_{B2} AROUND D2
R4- SETS VALUE OF I_{B1}
R5- SETS VALUE OF I_{B2}
C1 & C2- LOCAL DECOUPLING OF BASE DRIVE SUPPLIES
OPTO COUPLER- ISOLATES DRIVE CIRCUIT FROM CONTROL ELECTRONICS

Figure 2.9 Schematic Representations of Powerex Hybrid Base Drive ICs



2.4 Hybrid Base Drive IC

Powerex offers a series of hybrid base drive integrated circuits (ICs) which can directly interface TTL level logic signals to the base of a power Darlington module. These hybrid ICs can speed design in time of power Darlingtons while providing a base drive solution with proven reliability in a compact, economical package with low power consumption. Figure 2.9 illustrates schematically three different types of hybrid base drive ICs available.

The M57215L is a dual power supply type with an internal optocoupler for isolation of control circuits from the base drive circuit. The M57215BL is identical to the M57214L, except it has a higher isolation voltage rating suited for application with 1000 volt rated Darlingtons. The M57903L is a single power supply type with an internal optocoupler. The M57903L does include a pull down transistor which when used in conjunction with an external capacitor can supply a transient reverse base current at turn-off. The M57904L is similar to the M57903L except it does not include an internal optocoupler. The M57904L contains three independent identical circuits and is suitable for operating transistor modules in a three phase inverter. Figure 2.10 illustrates application of the M57903L and M57904L and Figure 2.11 illustrates application of the M57215L and M57950L.

Figure 2.10 Application of the M57903L and M57904L Hybrid Base Drive ICs

	Module Rating			
	20A	30A	50A	Unit
V_{CC}	10	10	10	Volts
V_{IN}	4 ~ 5	4 ~ 5	4 ~ 5	Volts
R_{ext}	20	15	8.7	Ω
C_{ext}	22	33	47	μF
C_1	2200	3300	4700	μF
f	2	2	2	kHz

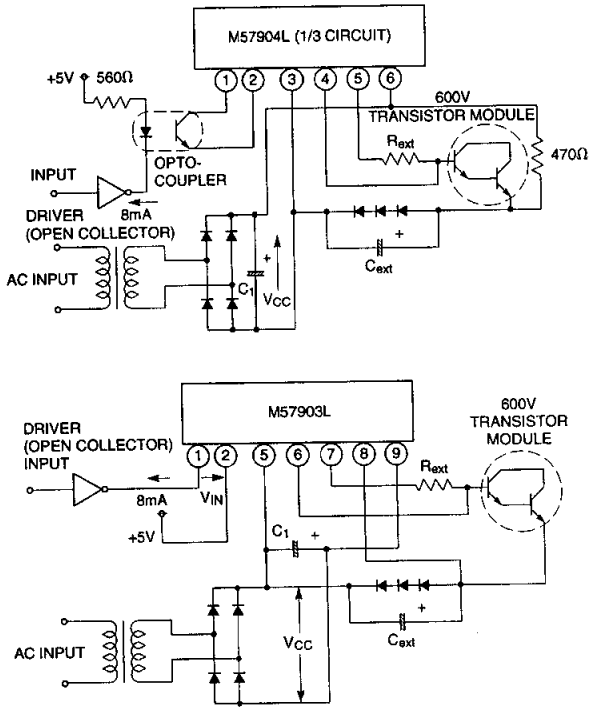
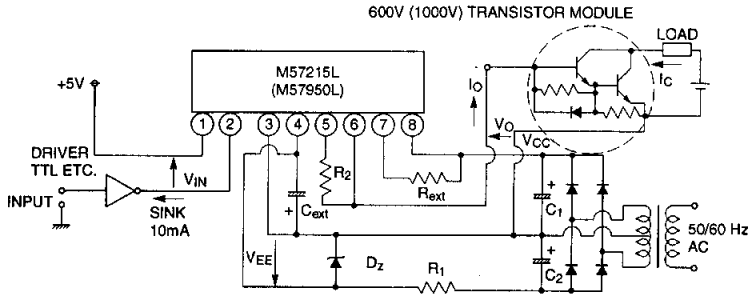


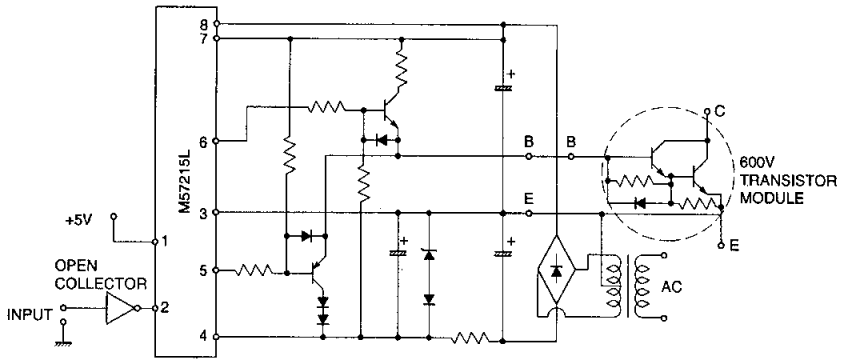
Figure 2.11 Application of the M57215L and M57215BL Hybrid Base Drive ICs

(A) Circuit configuration for 20-75 Aamp 600 and 1000 Volt Darlingtons
Note: This circuit and circuit value can be used for 1000V transistor modules with the M57215BL.

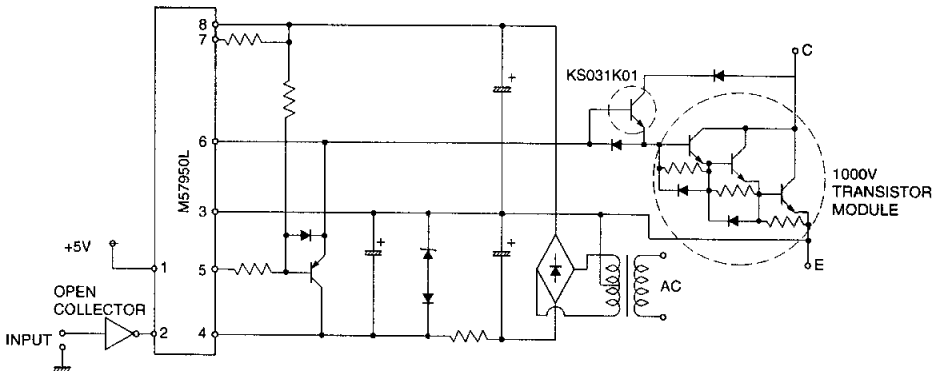


	Module Rating				
	20A	30A	50A	75A	Unit
V_{CC}	10	10	10	10	Volts
V_{EE}	-3	-3	-3	-3	Volts
V_{IN}	4~5	4~5	4~5	4~5	Volts
R_{ext}	27	20	12	9	Ω
R_2	3.3	2.2	1	1	Ω
f	2	2	2	2	kHz
R1	150	150	150	150	Ω
DZ	IN4372A	IN4372A	IN4372A	IN4372A	IN4372A
C_{ext}	10	22	22	47	μF
C_1	2200	3300	4700	4700	μF
C_2	470	470	470	470	μF

(B) Circuit configuration for 100-300 Amp 600 Volt Darlingtons



(C) Circuit configuration for 100-300 Amp 1000 Volt Darlingtons



2.5 Determining Power Losses

Proper application of Darlington transistors requires that users determine device power losses and provide adequate cooling to keep junction temperatures within rated values. The single largest cause of Darlington transistor application problems is the failure of equipment designers to properly determine device power losses, especially switching losses, and provide adequate cooling and/or mounting. Power losses can be grouped into three categories:

1. Switching Losses
   - Turn-on Losses
   - Turn-off Losses

2. Conduction Losses
   - On-state Losses
   - Dynamic Saturation Losses

3. Off-state Losses

Off-state losses in high power electronic circuits are generally a very small portion of the total losses and are considered negligible. The relative magnitudes of the switching and conduction losses are greatly dependent on the type of circuit in which the transistors are used, operating frequency, type of load, the turn-on and turn-off snubbers used and certain characteristics of the transistor itself.

In most power applications, transistors are operated at switching frequencies which are high enough that junction temperature can be calculated based upon average power dissipation. Thermal design must be based upon the worse case operating conditions. For example, in a motor drive application, a locked rotor condition may be a short term transient to the motor but it is usually well beyond the transient thermal time constant of the transistor. Such an operating condition is a steady state condition for the transistor and would determine the thermal design of the equipment.

Average power for a repetitive waveform is determined in the general case by integrating the instantaneous power, (product of I_C and V_{CE}), over a switching cycle and dividing by the period. That is:

$$P_{AVE} = 1/T \bullet \int_O^T I_C \bullet V_{CE}$$

$$dt = f \bullet \int_O^T i_C \bullet V_{CE}\, dt$$

where:

P_{AVE} = Average power dissipated
T = Period of one switching cycle
I_C = Instantaneous value of collector current
V_{CE} = Instantaneous value of collector to emitter voltage
f = Switching frequency

The most accurate method to determine P_{AVE} in switching application is to plot I_C and V_{CE} waveforms, multiply them together to obtain an instantaneous power waveform, and graphically integrate the area under the instantaneous power waveform. The availability of waveform processing digital storage oscilloscopes has made this process relatively simple.

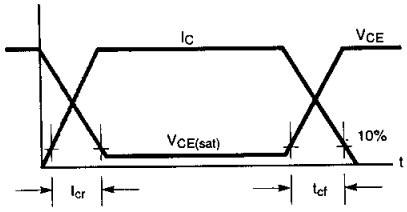
Due to the high peak values of instantaneous power dissipation during turn-on and turn-off switching, care must be taken when integrating instantaneous power waveforms to provide adequate time base resolution. For example, a digital scope cannot provide an accurate average power calculation when the time base is set to capture an entire switching cycle.

It is possible to provide equations for calculating switching and conduction losses if the switching waveforms are linearly approximated. This method is discussed below and is useful for initial design work. A completed design should always be based upon power calculations derived form actual waveforms at worse case operating conditions.

2.5.1 Switching Losses

Turn-on and turn-off switching losses occur during the transition from the off to on-state and the on to off-state respectively. Figure 2.12 shows a typical switching waveform for a resistive load.

Figure 2.12 Resistive Switching Waveforms



Assuming linear switching transitions and integrating the product of current and voltage over the interval yields switching energy:

$W_{SW(on)}$ =
1/6 ($V_{CE(max)}$ • $I_{C(max)}$ • t_{cr})
(Watt Seconds/Pulse)

$W_{SW(on)}$ =
1/6 ($V_{CE(max)}$ • $I_{C(max)}$ • t_{cf})
(Watt-Seconds/Pulse)

Switching losses are next determined by multiplying the switching energies per pulse by the operating switching frequency:

$$P_{SW(on)} = W_{SW(on)} \bullet f \text{ (Watts)}$$

$$P_{SW(off)} = W_{SW(off)} \bullet f \text{ (Watts)}$$

The instantaneous product of current and voltage result in large values of instantaneous power dissipation. These values of instantaneous power change significantly for an inductive load as show in Figure 2.13.

During turn-on, current rises slowly in the transistor and since the inductance supports the supply voltage initially, the voltage across the transistor falls very quickly and the instantaneous product of voltage and current is negligible. On the other hand, during turn-off, the voltage across the transistor starts to rise and reaches its maximum value before the collector current starts to fall and generates a larger peak power than for the resistive load. For inductive loads, the time from 10% of maximum voltage to 10% of the falling current (crossover time, t_{cf}) is longer than the fall time.

Again assuming linear switching transitions, the switching energy for an inductive load without a turn-off snubber is:

$W_{SW(off)}$ =
1/2 ($V_{CE(max)}$ • $I_{C(max)}$ • t_{cf})
(Watt Seconds/Pulse)

where:

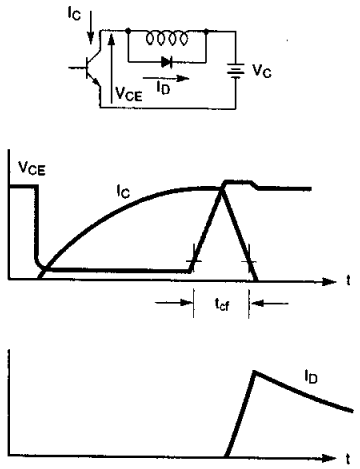
$V_{CE(max)}$ = Maximum voltage across transistor at turn-off (supply + spike)

$I_{C(max)}$ = Maximum load current

t_{fc} = Turn-off crossover time

When the transistor is turned off, current that was flowing in the inductor continues to flow through a diode placed across the inductor to keep the induced voltage from creating a voltage spike that can destroy the transistor.

Figure 2.13 Inductive Switching Waveform (Low Duty Cycle)



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Diode current rises to the
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L/R where L and R are the
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inductor.

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Figure 2.13 is turned on a
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in Figure 2.14. This is the
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the diode is still conducti
full supply voltage, minus
diode forward voltage dro
applied across the transis
causing a high instantane
power dissipation in the tr

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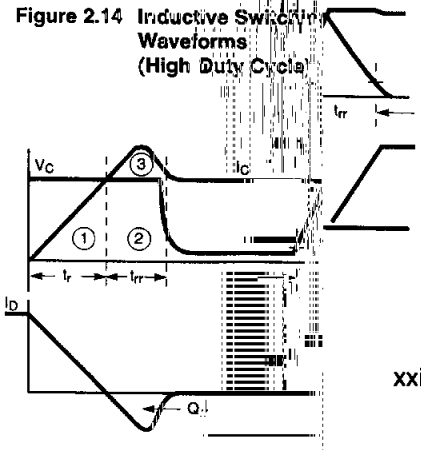
Figure 2.14 Inductive Switching Waveforms (High Duty Cycle)



After the diode current passes through zero, it still continues to conduct momentarily, until the stored charge in the diode is swept away. Current that is flowing in the reverse direction through the diode during the diode reverse recovery time, (t_{rr}), is added to the transistor collector current and causes additional turn-on switching losses. Turn-on switching energy during turn-on into an existing current is:

$$W_{SW(on)} = 1/2\ (V_{CE(max} \bullet I_{C(max)} \bullet t_r) + V_{CE(max)} \bullet I_{C(max)} \bullet t_{rr} + V_{CE(MAX)} \bullet Q_{rr}$$

where:

$V_{CE(max)}$	= Maximum supply voltage
$I_{C(max)}$	= Maximum turn-on load current
t_r	= Transistor rise time
t_{rr}	= Diode reverse recovery time
Q_{rr}	= Diode reverse recovery charge

It can be seen that it is very important to use fast recovery diodes in order to keep t_{rr} and Q_{rr} as small as possible in order to reduce turn-on losses.

As in the resistive load case, inductive load switching losses are determined by multiplying the switching energies per pulse by the operating switching frequency:

$$P_{SW(on)} = W_{SW(on)} \bullet f \text{ (Watts)}$$

$$P_{SW(off)} = W_{SW(off)} \bullet f \text{ (Watts)}$$

2.5.2 Conduction Losses

Conduction loss calculations are fairly straightforward, in that they are the product of the on-state voltage and the collector current of the transistor during the time it is on.

$$P_{on} = V_{CE(satT)} \bullet I_C \bullet (\text{Duty Cycle}).$$

Transistor saturation voltage is not reached immediately after turning on a transistor. There is a finite time, after the initial drop of off-state voltage, that it takes the transistor to fall to the final fully on condition.

This period of time is called the dynamic saturation time (t_{ds}) and it is dependent on the transistor design, base drive impedance, base drive magnitude and open circuit voltage and also on the type of load. Figure 2.15 shows this time as being measured from 10% of V_{CE} peak at turn-on to 110% of the final $V_{CE(sat)}$ value.

Depending on the type of transistor and base drive conditions, t_{ds} can range from 1 to 10 microseconds. Dynamic saturation is a strong function of forward base current, t_{ds} increases as I_{B1} decreases. If the total on time of the transistor is large in comparison to the dynamic saturation time, the additional losses can be neglected, but as switching frequency increases, t_{ds} becomes a significant portion of the total on time and conduction losses are much greater than the values calculated by using the value of $V_{CE(satT)}$ given on the device data sheet. In reality, the voltage falls from 10% $V_{CE(max)}$ to 110% $V_{CE(sat)}$ exponentially, but a safe approximation for calculation purposes is to assume a linear fall as shown in Figure 2.15. Conduction losses, when it is necessary to account for dynamic saturation, can be approximated by the expression:

$$P_{on} = [V_{CE(sat)} \bullet t_{on} + 1/2 \bullet (0.1 \bullet V_{CE(max)} - 1.1 \bullet V_{CE(sat)}) \bullet t_{ds}] \bullet I_{C(max)} \bullet f \text{ (Watts)}$$

for t_{on} greater than t_{ds}, and

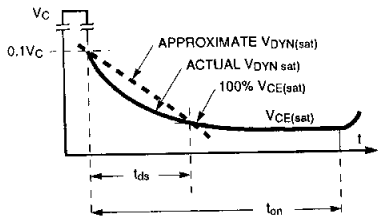
$$P_{on} = [0.1 \bullet V_{CE(max)} - 1/2 \bullet (1.0 \bullet V_{CE(max)} - 1.1 \bullet V_{CE(satT)}) \bullet t_{on}/t_{ds}] \bullet I_{C(max)} \bullet t_{on} \bullet f \text{ (Watts)}$$

for t_{on} less than t_{ds}.

where:

$V_{CE(max)}$	= Maximum supply voltage
$V_{CE(sat)}$	= Transistor saturation (On-state) voltage
t_{on}	= Transistor on time
t_{ds}	= Dynamic saturation Time
f	= Switching frequency

Figure 2.15 Dynamic Saturation Voltage



Since t_{ds} is so dependent on base drive and load conditions and typical values of tds are not a standard parameter shown on device data sheets, it is wise to determine t_{ds} by experimentally using your own base drive and load conditions.

2.6 Parallel Operation

Operating Darlington transistors in parallel is an effective method to obtain higher operating currents than possible with a single module. When paralleling Darlington transistors, the total conducting time, i.e. the turn-on, turn-off and the on-state must be considered for the paralleled transistors to share current equally.

In the on-state, Darlington transistors tend to inherently share current due to the gain fall off at high currents preventing excessive current hogging by a single transistor and due to the negative feedback effect created by the increase in base to emitter voltage with an increase in collector current acting to reduce base current. The degree of static current sharing depends upon whether the transistors are operated in quasi-saturation ($V_{CE} \geq V_{BE}$) or hard saturation ($V_{CE} < V_{BE}$).

In quasi-saturation operation, current sharing is determined by gain. Typical gain bands for Powerex Darlington transistors are illustrated in Figure 2.16. The Baker clamp, shown in Figure 2.17, is a very effective circuit to achieve quasi-saturation operation and it is often used in parallel applications. It is usually sufficient to use a single series diode in the base lead instead of two as shown in Figure 2.17.

Gain Class	h_{FE} Range
A	75 to 105
B	95 to 125
C	110 to 150
D	130 to 170
E	155 to 205
F	170 to 230
G	210 to 270
H	245 to 315
J	280 to 360

Gain mismatch effects can be minimized by operating the transistors in hard saturation. When hard saturation operation is used it is not relevant to specify gain matching. For hard saturation operation, current sharing is determined by saturation resistance, and matching should be on $V_{CE(sat)}$. Tests have shown that if transistors are overdriven into hard saturation, the $V_{CE(sat)}$ can be matched to within 0.1 volt. A base current overdrive of two times the base current at minimum gain is necessary to achieve this overdrive.

With quasi-saturation or hard saturation operation, V_{BE} should be matched to eliminate any base current mismatch. Some articles recommend using individual base resistors for paralleled transistors fed from voltage sources significantly higher than $V_{BE(sat)}$. This and similar constant current drives are not recommended for paralleling Darlingtons because this type of base drive tends to oversaturate high gain transistors and leads to

Figure 2.16 Gain Matching and Typical Gain Bands for Darlington Transistors

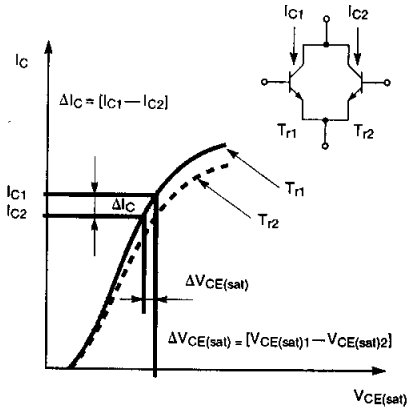
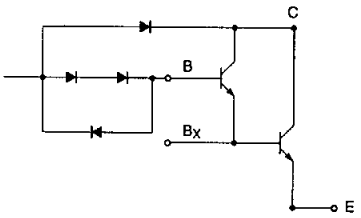


Figure 2.17 Baker Clamp Circuit



increasing the spread of storage time between the paralleled devices. Directly tieing the bases together of paralleled transistors causes the base current to divide among the transistors based upon gain. When V_{BE} is matched, equal base currents will flow.

Often, articles on paralleling transistors recommend using emitter resistors to force static current sharing. Emitter resistors work well in theory and in small signal applications. In high current Darlington applications, emitter resistors improve performance minimally at the expense of large power dissipation. Emitter resistors also increase the parasitic inductance

in the emitter circuit which creates oscillation and dynamic sharing problems that are much worse than static mismatch. A similar recommendation is to use emitter inductors wound in opposition on a common core to provide static and dynamic current sharing. Again, in high current Darlington applications, emitter inductors create oscillation problems and usually deteriorate turn-off switching waveforms. Thus, emitter resistors and/or inductors are not recommended for paralleling high current Darlingtons.

The most critical aspect of paralleling Darlingtons is insuring dynamic current sharing. Turn-on sharing is generally not a problem if the bases are tied together and adequate base drive is provided. Turn-off sharing is the major problem area. The transistor with the longest storage time will be forced to turn off the entire load current which is most likely subjecting it to a turn-off load line that is outside the device RBSOA limit.

At first glance it appears that one should match device storage times. But due to the large variation of storage time over temperature, it is not practical to match storage times. The best method to minimize storage time variations is to operate the devices in quasi-saturation using an anti-saturation circuit such as a Baker clamp. For paralleled Darlingtons, the Baker clamp circuit should be connected with individual series base diodes for each transistor and a single collector feedback diode for the entire paralleled set.

If the additional on-state losses inherent in quasi-saturation operation can not be tolerated and hard saturation operation is used, storage time differences can be minimized by high levels of I_{B2}.

Since high I_{B2} reduces RBSOA capability a turn-off voltage snubber should be used to limit the collector to emitter voltage rise until after the collector current has reached a low value. The use of a turn-off voltage snubber is recommended in all cases when paralleling Darlingtons because even if one transistor does end up turning off the entire load current the turn-off snubber will prevent it from seeing high voltage when it is conducting high current.

Dynamic current sharing is also improved if the bases of the output transistors in the Darlington are connected together. Many Powerex Darlington transistors provide a Bx terminal which allows this connection. With the Bx terminals connected, the Darlington transistor which turns on first provides additional base current to the outputs of the remaining paralleled Darlingtons through the Bx connection, eliminating the delay in turn-on between the transistors.

The Bx connection also forces the transistors to share current during storage time, eliminating storage time differentials. The major portion of the storage time is in the input stage because the output stage is kept out of saturation by the Darlington connection. With the Bx terminals connected together none of the outputs begins to turn off until all of the input stages have turned off, making the transistors function as if the storage times were matched.

Although matching transistor parameters is important, subtle factors of base drive design and layout are more critical to successful paralleling of Darlington transistors. Devices must be mounted on a common heat sink in close thermal coupling with cooling applied evenly to maintain equal operating temperatures. Circuit layout should be such that emitter circuit inductance is minimized and symmetry, especially for powerleads, is maximized. The drive circuit common should be connected to the common emitter terminals as close as possible to the packages to keep inductive and resistive drops in the high current wiring out of the drive circuit.

Due to their high gain, Darlingtons connected in parallel tend to develop parasitic high frequency oscillations. This is especially true when the bases of the paralleled device are connected directly together as recommended above. High values of parasitic inductance in the emitter and base circuits and high levels of I_{B2} also tend to promote oscillation. These parasitic oscillations can often be eliminated by adding ferrite beads in the base leads. The series diodes of a Baker clamp circuit may also help to eliminate oscillations.

2.7 Reverse Transistor Action and dv/dt Turn-on

A problem that occurs with the half-bridge circuit configuration fed by a voltage source, especially in pulse width modulated inverters with inductive loads, is that of reverse transistor action. This is a condition where the transistor actually conducts in the reverse direction due to a reverse voltage applied across the transistor.

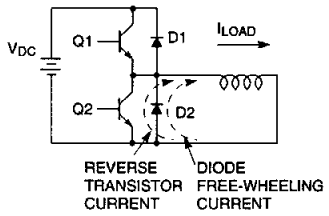
A typical half-bridge circuit driving an inductive load is shown in Figure 2.18. This circuit is a basic building block in power electronics.

Transistor Q1 turns on to establish current in the inductive load. When Q1 is turned off, the load inductance produces a voltage kick such that the load current is maintained through D2. The forward voltage drop across D2 creates a reverse voltage across Q2 in the range of 1-2 volts causing reverse current to flow through the transistor from emitter to collector. The magnitude of this current is controlled by the reverse gain of the transistor. Reverse gain is usually only a fraction of the forward gain of the transistor, and occurs due to the symmetry of the NPN construction that allows the collector and emitter to exchange their functions. That is, the collector acts as an emitter and the emitter acts as the collector. The transistor will not be as efficient as it is when used correctly, but it will in fact, operate backward.

The major problem occurs when transistor Q1 is again turned on after or when Q2 is carrying reverse current. The collector-base junction capacitance of Q2 has a charge that must be removed before it can block voltage. The high dv/dt applied to Q2 by the turn on of Q1 causes a large current to flow through the collector-base junction capacitance of Q2 which continues until this charge is removed. This recovery current of Q2 is in addition to, and can be significantly greater in duration and magnitude than, the reverse recovery current spike of the free-wheeling diode D2. The uninitiated often mistake a dv/dt current spike problem for a poor free-wheeling diode reverse recovery performance. This dv/dt current spike can easily take the transistor load line outside of the device FBSOA curve leading to catastrophic device failure at turn-on. At best, the dv/dt current spike will significantly increase turn on switching losses. The dv/dt problem is particularly acute with Darlingtons because even a small base current generated by capacitive dv/dt current is amplified by the input and output stages of the Darlington.

There are several methods for eliminating the reverse transistor action and its resultant dv/dt switching spike, including blocking diodes in the collector or emitter circuits, Schottky blocking diodes in series with the base-emitter

Figure 2.18 Half-bridge Darlington Transistor Circuit with Inductive Load



resistance, turn-on snubber consisting of an inductor and diode in the collector circuit, and reverse bias base-to-emitter on the transistor.

Most of these solutions cannot be physically realized when using power modules due to inaccessibility of internal connection points. The only foolproof solution is the use of a maintained reverse bias base-to-emitter on the transistor during its off period. In applications where a maintained reverse bias cannot be provided it is possible to use reverse bias only during defined periods. That is, during turn-off to improve switching and during turn-on of the opposite half-bridge pair to avoid dv/dt turn-on.

Figure 2.19 illustrates the effect of base emitter reverse bias on the dv/dt induced current spike.

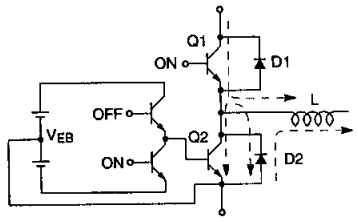
2.8 Shoot-through Protection

Power switching applications utilizing the half-bridge configuration in voltage fed inverters are prone to shoot-through failures. A shoot-through condition exists when both the upper and lower transistors in the half-bridge configuration are on, creating a short circuit across the DC supply. A properly designed inverter must include a lock-out circuit to prevent the upper and lower transistors from being turned on at the same time.
This lock-out logic must also function properly as bias and main power cycles on and off. Since, due to storage time, transistors take longer to turn-off than to turn-on, the lock out logic must provide a fixed delay time between turn off of one transistor and turn on of the other half-bridge transistor leg. This delay time must be greater than the longest possible storage time determined from the worse case application base drive, load and temperature conditions. The delay time for Darlington power modules is typically in the tens of micro-seconds.

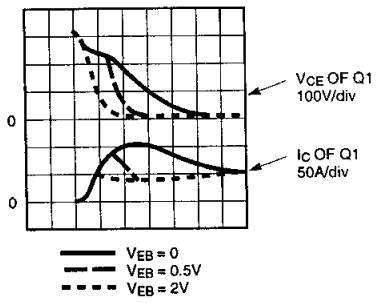
2.9 Turn-off Snubbers

Turn-off of high currents can produce large L • di/dt surge voltages across a transistor due to parasitic wiring inductances. To keep the transistor within its RBSOA rating some form of turn-off voltage snubber will be required.

Figure 2.19 Elimination of dV/dt Induced Turn-on Spike with Base-to-emitter Reverse Bias



(A) EXPLANATION OF dv/dt CURRENT FLOW



(B) RELATION BETWEEN V_{EB} AND TURN-ON WAVEFORMS

Figure 2.20 Shoot-through Protection with Lock Out Logic

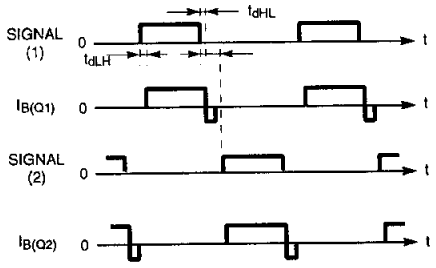


Figure 2.21 Turn-off Voltage Snubbers

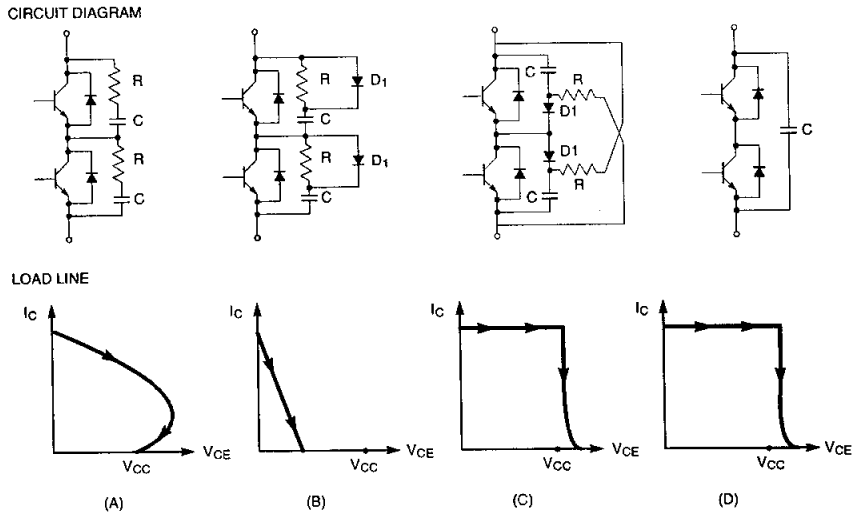


Figure 2.22 Basic Design Equations for R-C-D Turn-off Snubber

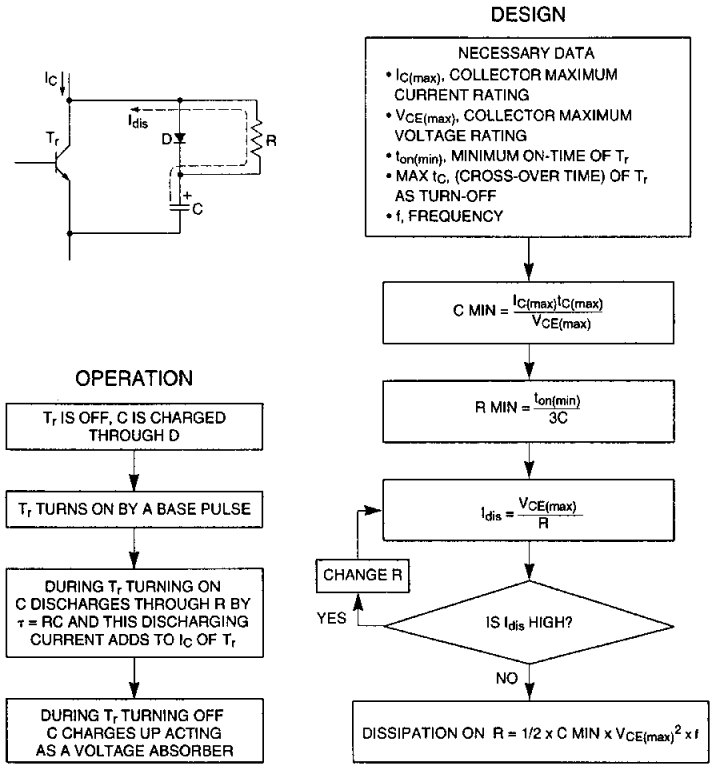


Figure 2.21 provides examples of typical voltage snubbers and illustrates the load line shaping each provides. Circuits 2.21 (C) and (D) are voltage clamps which only act to clip voltage spikes. The simple capacitor across the DC rail of Figure 2.21 (D) can oscillate with the main voltage source and the parasitic line inductance of the DC rail. The circuit of Figure 2.21 (C) adds resistance to avoid the oscillation while still providing voltage clamping. Circuits 2.21 (A) and (B) provide dv/dt control and can significantly reduce turn-off losses in the transistor.

The R-C-D snubber circuit of Figure 2.21 (B) is by far the most effective turn-off snubber and details of its design are provided in Figure 2.22. The R-C-D snubber imposes a minimum on-time to the transistor of three times the RC time constant to insure that the snubber capacitor is fully discharged prior to transistor turn off for effective snubbing. R-C-D snubbers can create problems in bridge circuits because when all transistors are off the snubber capacitors charge to intermediate voltages. When a transistor is then turned on a high spike is created due to the charge of the snubber capacitor in the opposite leg of the half-bridge.

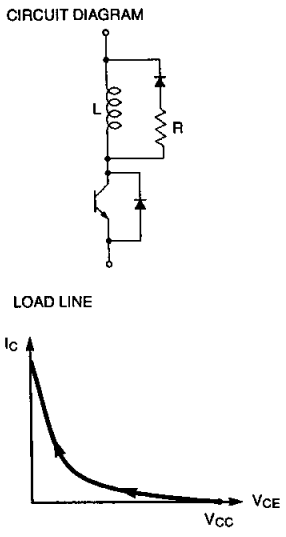
In all cases, a turn-off snubber is only effective if the snubber components are located in close physical proximity to the power module they are meant to protect. Capacitors should be of the high

frequency type with good RMS ripple current capability, low ESR and ESI. Often a number of smaller capacitors in parallel will provide better performance than a single large capacitor. Diodes should be fast recovery types and resistors should be non-inductive types, specifically not wirewound resistors. Properly designed snubbers are also sized based upon the worse case fault current the transistor will have to turn off.

2.10 Turn-on Snubber

The turn-on snubber shown in Figure 2.23 may be used to keep a transistor within its FBSOA limit at turn-on. The turn-on snubber limits the rate of rise of collector current, (di/dt), and significantly reduces transistor turn-on losses. The energy stored in the inductor during transistor turn-on must be dissipated in the resistor when the transistor is turned off. This sets a minimum off-time requirement on the transistor of three times the L/R time constant to insure that the inductor energy is dissipated before the transistor is again turned on. The energy storage in the inductor can be minimized by using a saturable inductor.

Figure 2.23 Turn-on Current Snubber



2.11 Short Circuit Endurance

When the load is suddenly shorted in a transistor circuit, the full DC rail voltage appears across the transistor and the current is limited by the transistor gain. Since power dissipation under these conditions is many times the device rated power, the transistor will fail catastrophically unless reverse base drive is quickly applied to turn-off the device.

The gain of a Darlington transistor increases substantially as the collector to emitter voltage increases, as shown in Figure 2.24. At the high current levels associated with overload operation the gain decreases with increasing temperatures. This gain reduction with temperature is more significant in high voltage Darlingtons, 1000 volt and above, which utilize the triple Darlington configuration. The gain curves at 25°C and 125°C of the standard two stage Darlington, typical of 600 volts and below, tend to merge at high voltages.

Figure 2.24 Collector Current vs. Collector-to-emitter Voltage for Various Base Drives and Temperatures

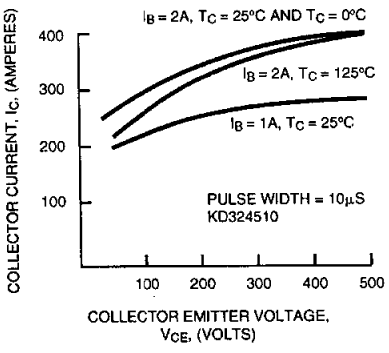


Figure 2.25 V_{CE} and I_C During Shorted Load

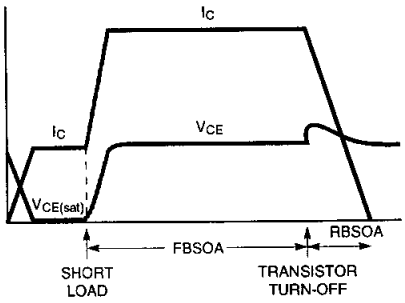


Figure 2.25 shows the waveforms prior to and during overload operation. At the time the load is shorted, the transistor quickly comes out of saturation and the collector-to-emitter voltage rises to the rail voltage less the small voltage drops in the connecting wires. The collector current rises to a value that is dependent on the base drive and the gain of the transistor. Even at recommended forward base drive levels, selected to achieve reasonable saturation voltages, the resulting gain limited short circuit current can reach destructively high levels. During this period the transistor is

Figure 2.26 Typical Short Circuit Endurance Curve and Test Circuit

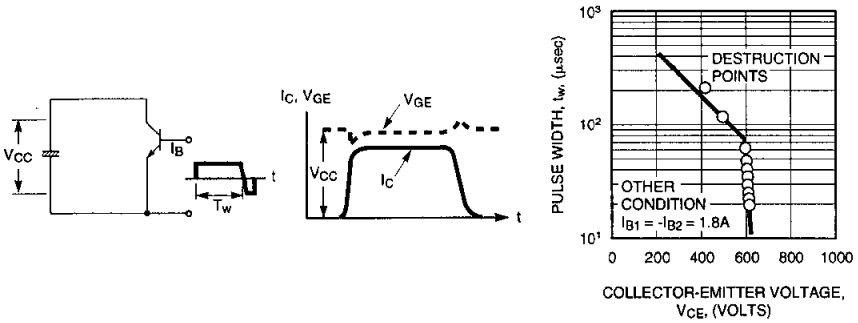
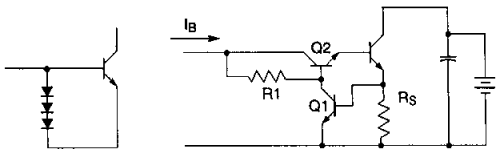


Table 2.2 Short Circuit Withstand of Powerex Darlingtons (100 Pulses, T_{CASE} = 100°C)

Transistor Type	Max. I_{B1}	Max. V_{CC}	Max. T_W	Approx. $I_{C(sat)}$	Emitter Wire I^2t
KD224503	0.6A	400V	50μs	100A	$0.7 \cdot 10^3$
KD224505	0.6A	400V	50μs	160A	$1.5 \cdot 10^3$
KD224575	1.0A	400V	50μs	230A	$2.0 \cdot 10^3$
KD224510	1.5A	400V	50μs	300A	$3.5 \cdot 10^3$
KD224515	1.8A	400V	50μs	450A	$4.0 \cdot 10^3$
KS324520	2.5A	400V	50μs	550A	$6.0 \cdot 10^3$
KS624530	3.5A	400V	50μs	800A	$8.0 \cdot 10^3$
KD221K03	0.6A	580V	30μs	100A	$1.5 \cdot 10^3$
KD221K05	0.6A	580V	30μs	175A	$2.1 \cdot 10^3$
KD221K75	1.0A	580V	30μs	250A	$3.4 \cdot 10^3$
KD421K10	1.5A	580V	30μs	350A	$4.2 \cdot 10^3$
KD421K15	1.8A	580V	30μs	500A	$6.5 \cdot 10^3$
KS621K20	2.5A	580V	30μs	700A	$8.0 \cdot 10^3$
KS621K30	3.5A	580V	30μs	1000A	$13.0 \cdot 10^3$

Figure 2.27 V_{BE} Clamp and Active Base Control Overload Protection



operating in an FBSOA condition. It must be turned off before it exceeds the FBSOA boundaries.

When the transistor is turned off, the RBSOA curves must be observed. Note that the voltage of the RBSOA curve must never be exceeded, but the current in both the FBSOA and the RBSOA operating areas can be exceeded, provided that the maximum junction temperature is not exceeded. This maximum junction temperature is 150°C for repetitive pulses. For pulse operation, similar to surge in a diode, the transistor can be pulsed to 250°C or even greater than 300°C for a limited number of pulses.

Figure 2.26 illustrates typical short circuit endurance capabilities and the test conditions for Powerex Darlington transistors. There are two important points to note from this data. First, the short circuit current must be minimized by limiting base current. This insures that the transistor power dissipation is kept within bound. Second, there is a critical voltage level above which the transistor has no short circuit endurance capability. At this critical voltage level device destruction occurs just at the instant when I_C reaches its peak value. This failure mechanism is different than the pulse width limited thermal dissipation failure mechanism. Thus, one needs to consider the absolute voltage level in determining short circuit endurance of a given application.

Table 2.2 provides additional data on short circuit endurance capabilities of Powerex Darlington transistors. Any protection scheme should be designed to sense a short circuit and turn the device off in a period less than that of the transistor short circuit withstand capability. The best short circuit protection scheme adds an inductor in series with the transistor that acts to control the rate-of-rise of current and support voltage during the load short circuit. Of course, this inductor must be properly clamped to prevent it from creating damaging voltage spikes. V_{BE} limiting clamps and active base drive limiting, illustrated in Figure 2.27, are two solutions that may provide limiting of collector current during overload without a limiting inductor.

When a short appears across an interphase load as shown in Figure 2.28, the total rail voltage is impressed across both transistors. If Q1 and Q4 are on during a short, the rail voltage does not divide equally across the transistors but the division of the voltage depends on the gains of the transistors. The worse case voltage division must be applied to the short circuit withstand investigation.

2.12 Typical Applications

Powerex Darlington transistor modules are provided in a number of different circuit configurations. Figure 2.29 illustrates typical applications for some of the different module configurations.

Figure 2.28 Interphase Short and Resulting Rail Voltage Division

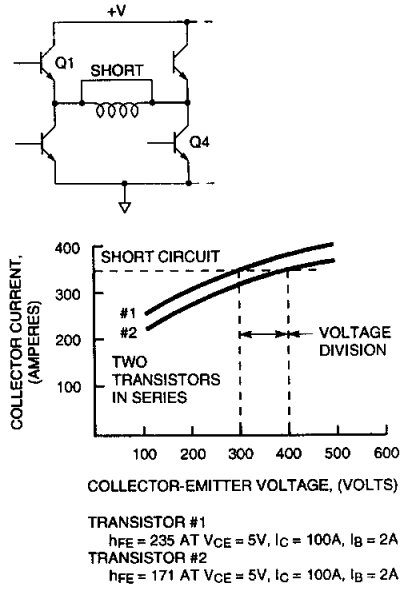


Figure 2.29 Typical Applications for Darlington Modules