2.5 Determining Power Losses

Proper application of Darlington transistors requires that users determine device power losses and provide adequate cooling to keep junction temperatures within rated values. The single largest cause of Darlington transistor application problems is the failure of equipment designers to properly determine device power losses, especially switching losses, and provide adequate cooling and/or mounting. Power losses can be grouped into three categories:

1. Switching Losses
   - Turn-on Losses
   - Turn-off Losses

2. Conduction Losses
   - On-state Losses
   - Dynamic Saturation Losses

3. Off-state Losses

Off-state losses in high power electronic circuits are generally a very small portion of the total losses and are considered negligible. The relative magnitudes of the switching and conduction losses are greatly dependent on the type of circuit in which the transistors are used, operating frequency, type of load, the turn-on and turn-off snubbers used and certain characteristics of the transistor itself.

In most power applications, transistors are operated at switching frequencies which are high enough that junction temperature can be calculated based upon average power dissipation. Thermal design must be based upon the worse case operating conditions. For example, in a motor drive application, a locked rotor condition may be a short term transient to the motor but it is usually well beyond the transient thermal time constant of the transistor. Such an operating condition is a steady state condition for the transistor and would determine the thermal design of the equipment.

Average power for a repetitive waveform is determined in the general case by integrating the instantaneous power, (product of I_C and V_{CE}), over a switching cycle and dividing by the period. That is:

$$P_{AVE} = 1/T \bullet \int_O^T I_C \bullet V_{CE}$$

$$dt = f \bullet \int_O^T i_C \bullet V_{CE}\, dt$$

where:

P_{AVE} = Average power dissipated
T = Period of one switching cycle
I_C = Instantaneous value of collector current
V_{CE} = Instantaneous value of collector to emitter voltage
f = Switching frequency

The most accurate method to determine P_{AVE} in switching application is to plot I_C and V_{CE} waveforms, multiply them together to obtain an instantaneous power waveform, and graphically integrate the area under the instantaneous power waveform. The availability of waveform processing digital storage oscilloscopes has made this process relatively simple.

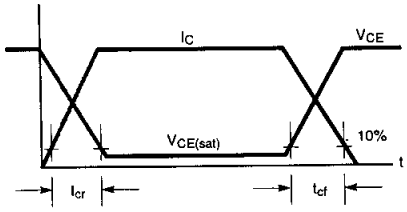
Due to the high peak values of instantaneous power dissipation during turn-on and turn-off switching, care must be taken when integrating instantaneous power waveforms to provide adequate time base resolution. For example, a digital scope cannot provide an accurate average power calculation when the time base is set to capture an entire switching cycle.

It is possible to provide equations for calculating switching and conduction losses if the switching waveforms are linearly approximated. This method is discussed below and is useful for initial design work. A completed design should always be based upon power calculations derived form actual waveforms at worse case operating conditions.

2.5.1 Switching Losses

Turn-on and turn-off switching losses occur during the transition from the off to on-state and the on to off-state respectively. Figure 2.12 shows a typical switching waveform for a resistive load.

Figure 2.12 Resistive Switching Waveforms



Assuming linear switching transitions and integrating the product of current and voltage over the interval yields switching energy:

$W_{SW(on)}$ = 1/6 ($V_{CE(max)}$ • $I_{C(max)}$ • t_{cr}) (Watt Seconds/Pulse)

$W_{SW(on)}$ = 1/6 ($V_{CE(max)}$ • $I_{C(max)}$ • t_{cf}) (Watt-Seconds/Pulse)

Switching losses are next determined by multiplying the switching energies per pulse by the operating switching frequency:

$$P_{SW(on)} = W_{SW(on)} \bullet f \text{ (Watts)}$$

$$P_{SW(off)} = W_{SW(off)} \bullet f \text{ (Watts)}$$

The instantaneous product of current and voltage result in large values of instantaneous power dissipation. These values of instantaneous power change significantly for an inductive load as show in Figure 2.13.

During turn-on, current rises slowly in the transistor and since the inductance supports the supply voltage initially, the voltage across the transistor falls very quickly and the instantaneous product of voltage and current is negligible. On the other hand, during turn-off, the voltage across the transistor starts to rise and reaches its maximum value before the collector current starts to fall and generates a larger peak power than for the resistive load. For inductive loads, the time from 10% of maximum voltage to 10% of the falling current (crossover time, t_{cf}) is longer than the fall time.

Again assuming linear switching transitions, the switching energy for an inductive load without a turn-off snubber is:

$W_{SW(off)}$ = 1/2 ($V_{CE(max)}$ • $I_{C(max)}$ • t_{cf}) (Watt Seconds/Pulse)

where:

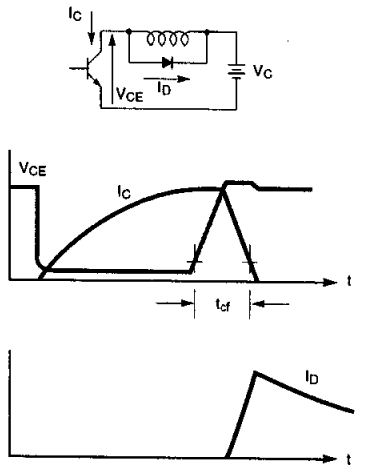
$V_{CE(max)}$ = Maximum voltage across transistor at turn-off (supply + spike)

$I_{C(max)}$ = Maximum load current

t_{fc} = Turn-off crossover time

When the transistor is turned off, current that was flowing in the inductor continues to flow through a diode placed across the inductor to keep the induced voltage from creating a voltage spike that can destroy the transistor.

Figure 2.13 Inductive Switching Waveform (Low Duty Cycle)

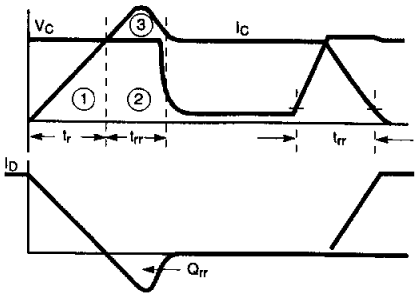


Diode current rises to the maximum value of load current when the transistor current reaches zero and then decays exponentially with a decay time of L/R where L and R are the inductance and resistance of the inductor.

If the transistor in the circuit of Figure 2.13 is turned on again before the current in the diode can decay to zero, significant changes occur in the transistor switching losses. The transistor now turns on into an existing current as shown in Figure 2.14. This is the typical condition found in voltage fed inverters.

When the transistor is turned on, the collector current starts to rise to the value of the load current. Current in the diode starts to fall at the same rate I_C rises, but since the diode is still conducting, the full supply voltage, minus the diode forward voltage drop, is applied across the transistor causing a high instantaneous power dissipation in the transistor.

Figure 2.14 Inductive Switching Waveforms (High Duty Cycle)



After the diode current passes through zero, it still continues to conduct momentarily, until the stored charge in the diode is swept away. Current that is flowing in the reverse direction through the diode during the diode reverse recovery time, (t_{rr}), is added to the transistor collector current and causes additional turn-on switching losses. Turn-on switching energy during turn-on into an existing current is:

$$W_{SW(on)} = 1/2\ (V_{CE(max} \bullet I_{C(max)} \bullet t_r) + V_{CE(max)} \bullet I_{C(max)} \bullet t_{rr} + V_{CE(MAX)} \bullet Q_{rr}$$

where:

$V_{CE(max)}$	= Maximum supply voltage
$I_{C(max)}$	= Maximum turn-on load current
t_r	= Transistor rise time
t_{rr}	= Diode reverse recovery time
Q_{rr}	= Diode reverse recovery charge

It can be seen that it is very important to use fast recovery diodes in order to keep t_{rr} and Q_{rr} as small as possible in order to reduce turn-on losses.

As in the resistive load case, inductive load switching losses are determined by multiplying the switching energies per pulse by the operating switching frequency:

$$P_{SW(on)} = W_{SW(on)} \bullet f \text{ (Watts)}$$

$$P_{SW(off)} = W_{SW(off)} \bullet f \text{ (Watts)}$$

2.5.2 Conduction Losses

Conduction loss calculations are fairly straightforward, in that they are the product of the on-state voltage and the collector current of the transistor during the time it is on.

$$P_{on} = V_{CE(satT)} \bullet I_C \bullet (\text{Duty Cycle}).$$

Transistor saturation voltage is not reached immediately after turning on a transistor. There is a finite time, after the initial drop of off-state voltage, that it takes the transistor to fall to the final fully on condition.

This period of time is called the dynamic saturation time (t_{ds}) and it is dependent on the transistor design, base drive impedance, base drive magnitude and open circuit voltage and also on the type of load. Figure 2.15 shows this time as being measured from 10% of V_{CE} peak at turn-on to 110% of the final $V_{CE(sat)}$ value.

Depending on the type of transistor and base drive conditions, t_{ds} can range from 1 to 10 microseconds. Dynamic saturation is a strong function of forward base current, t_{ds} increases as I_{B1} decreases. If the total on time of the transistor is large in comparison to the dynamic saturation time, the additional losses can be neglected, but as switching frequency increases, t_{ds} becomes a significant portion of the total on time and conduction losses are much greater than the values calculated by using the value of $V_{CE(satT)}$ given on the device data sheet. In reality, the voltage falls from 10% $V_{CE(max)}$ to 110% $V_{CE(sat)}$ exponentially, but a safe approximation for calculation purposes is to assume a linear fall as shown in Figure 2.15. Conduction losses, when it is necessary to account for dynamic saturation, can be approximated by the expression:

$$P_{on} = [V_{CE(sat)} \bullet t_{on} + 1/2 \bullet (0.1 \bullet V_{CE(max)} - 1.1 \bullet V_{CE(sat)}) \bullet t_{ds}] \bullet I_{C(max)} \bullet f \text{ (Watts)}$$

for t_{on} greater than t_{ds}, and

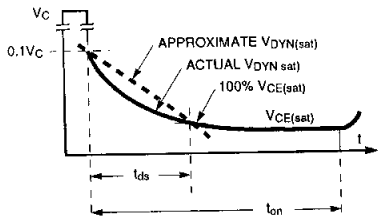
$$P_{on} = [0.1 \bullet V_{CE(max)} - 1/2 \bullet (1.0 \bullet V_{CE(max)} - 1.1 \bullet V_{CE(satT)}) \bullet t_{on}/t_{ds}] \bullet I_{C(max)} \bullet t_{on} \bullet f \text{ (Watts)}$$

for t_{on} less than t_{ds}.

where:

$V_{CE(max)}$	= Maximum supply voltage
$V_{CE(sat)}$	= Transistor saturation (On-state) voltage
t_{on}	= Transistor on time
t_{ds}	= Dynamic saturation Time
f	= Switching frequency

Figure 2.15 Dynamic Saturation Voltage



Since t_{ds} is so dependent on base drive and load conditions and typical values of tds are not a standard parameter shown on device data sheets, it is wise to determine t_{ds} by experimentally using your own base drive and load conditions.

2.6 Parallel Operation

Operating Darlington transistors in parallel is an effective method to obtain higher operating currents than possible with a single module. When paralleling Darlington transistors, the total conducting time, i.e. the turn-on, turn-off and the on-state must be considered for the paralleled transistors to share current equally.

In the on-state, Darlington transistors tend to inherently share current due to the gain fall off at high currents preventing excessive current hogging by a single transistor and due to the negative feedback effect created by the increase in base to emitter voltage with an increase in collector current acting to reduce base current. The degree of static current sharing depends upon whether the transistors are operated in quasi-saturation ($V_{CE} \geq V_{BE}$) or hard saturation ($V_{CE} < V_{BE}$).

In quasi-saturation operation, current sharing is determined by gain. Typical gain bands for Powerex Darlington transistors are illustrated in Figure 2.16. The Baker clamp, shown in Figure 2.17, is a very effective circuit to achieve quasi-saturation operation and it is often used in parallel applications. It is usually sufficient to use a single series diode in the base lead instead of two as shown in Figure 2.17.

Gain Class	h_{FE} Range
A	75 to 105
B	95 to 125
C	110 to 150
D	130 to 170
E	155 to 205
F	170 to 230
G	210 to 270
H	245 to 315
J	280 to 360

Gain mismatch effects can be minimized by operating the transistors in hard saturation. When hard saturation operation is used it is not relevant to specify gain matching. For hard saturation operation, current sharing is determined by saturation resistance, and matching should be on $V_{CE(sat)}$. Tests have shown that if transistors are overdriven into hard saturation, the $V_{CE(sat)}$ can be matched to within 0.1 volt. A base current overdrive of two times the base current at minimum gain is necessary to achieve this overdrive.

With quasi-saturation or hard saturation operation, V_{BE} should be matched to eliminate any base current mismatch. Some articles recommend using individual base resistors for paralleled transistors fed from voltage sources significantly higher than $V_{BE(sat)}$. This and similar constant current drives are not recommended for paralleling Darlingtons because this type of base drive tends to oversaturate high gain transistors and leads to

Figure 2.16 Gain Matching and Typical Gain Bands for Darlington Transistors

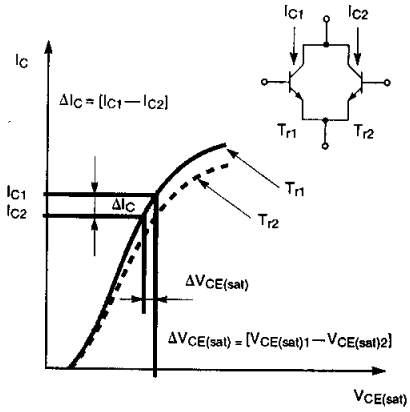
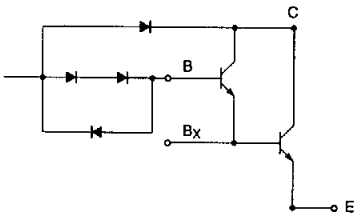


Figure 2.17 Baker Clamp Circuit



increasing the spread of storage time between the paralleled devices. Directly tieing the bases together of paralleled transistors causes the base current to divide among the transistors based upon gain. When V_{BE} is matched, equal base currents will flow.

Often, articles on paralleling transistors recommend using emitter resistors to force static current sharing. Emitter resistors work well in theory and in small signal applications. In high current Darlington applications, emitter resistors improve performance minimally at the expense of large power dissipation. Emitter resistors also increase the parasitic inductance

in the emitter circuit which creates oscillation and dynamic sharing problems that are much worse than static mismatch. A similar recommendation is to use emitter inductors wound in opposition on a common core to provide static and dynamic current sharing. Again, in high current Darlington applications, emitter inductors create oscillation problems and usually deteriorate turn-off switching waveforms. Thus, emitter resistors and/or inductors are not recommended for paralleling high current Darlingtons.

The most critical aspect of paralleling Darlingtons is insuring dynamic current sharing. Turn-on sharing is generally not a problem if the bases are tied together and adequate base drive is provided. Turn-off sharing is the major problem area. The transistor with the longest storage time will be forced to turn off the entire load current which is most likely subjecting it to a turn-off load line that is outside the device RBSOA limit.

At first glance it appears that one should match device storage times. But due to the large variation of storage time over temperature, it is not practical to match storage times. The best method to minimize storage time variations is to operate the devices in quasi-saturation using an anti-saturation circuit such as a Baker clamp. For paralleled Darlingtons, the Baker clamp circuit should be connected with individual series base diodes for each transistor and a single collector feedback diode for the entire paralleled set.

If the additional on-state losses inherent in quasi-saturation operation can not be tolerated and hard saturation operation is used, storage time differences can be minimized by high levels of I_{B2}.

Since high I_{B2} reduces RBSOA capability a turn-off voltage snubber should be used to limit the collector to emitter voltage rise until after the collector current has reached a low value. The use of a turn-off voltage snubber is recommended in all cases when paralleling Darlingtons because even if one transistor does end up turning off the entire load current the turn-off snubber will prevent it from seeing high voltage when it is conducting high current.

Dynamic current sharing is also improved if the bases of the output transistors in the Darlington are connected together. Many Powerex Darlington transistors provide a Bx terminal which allows this connection. With the Bx terminals connected, the Darlington transistor which turns on first provides additional base current to the outputs of the remaining paralleled Darlingtons through the Bx connection, eliminating the delay in turn-on between the transistors.

The Bx connection also forces the transistors to share current during storage time, eliminating storage time differentials. The major portion of the storage time is in the input stage because the output stage is kept out of saturation by the Darlington connection. With the Bx terminals connected together none of the outputs begins to turn off until all of the input stages have turned off, making the transistors function as if the storage times were matched.

Although matching transistor parameters is important, subtle factors of base drive design and layout are more critical to successful paralleling of Darlington transistors. Devices must be mounted on a common heat sink in close thermal coupling with cooling applied evenly to maintain equal operating temperatures. Circuit layout should be such that emitter circuit inductance is minimized and symmetry, especially for powerleads, is maximized. The drive circuit common should be connected to the common emitter terminals as close as possible to the packages to keep inductive and resistive drops in the high current wiring out of the drive circuit.

Due to their high gain, Darlingtons connected in parallel tend to develop parasitic high frequency oscillations. This is especially true when the bases of the paralleled device are connected directly together as recommended above. High values of parasitic inductance in the emitter and base circuits and high levels of I_{B2} also tend to promote oscillation. These parasitic oscillations can often be eliminated by adding ferrite beads in the base leads. The series diodes of a Baker clamp circuit may also help to eliminate oscillations.