Title	***Engineering Prototype Report 7*** ***12V @30W Universal Input Engineering Prototype (EP7)***
Recipients	
Customer	
Author	R.H.
Date	21-December-99

Abstract

This document details the specification and actual operation of a 12V, 30W universal input supply using the TOP234Y.

Power Integrations Inc
477 N. Mathilda Avenue, Sunnyvale, CA 94086 USA
Tel: +1 4085 523 9200 Fax: +1 408 523 9300
www: http://www.powerint.com

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1.0 Introduction

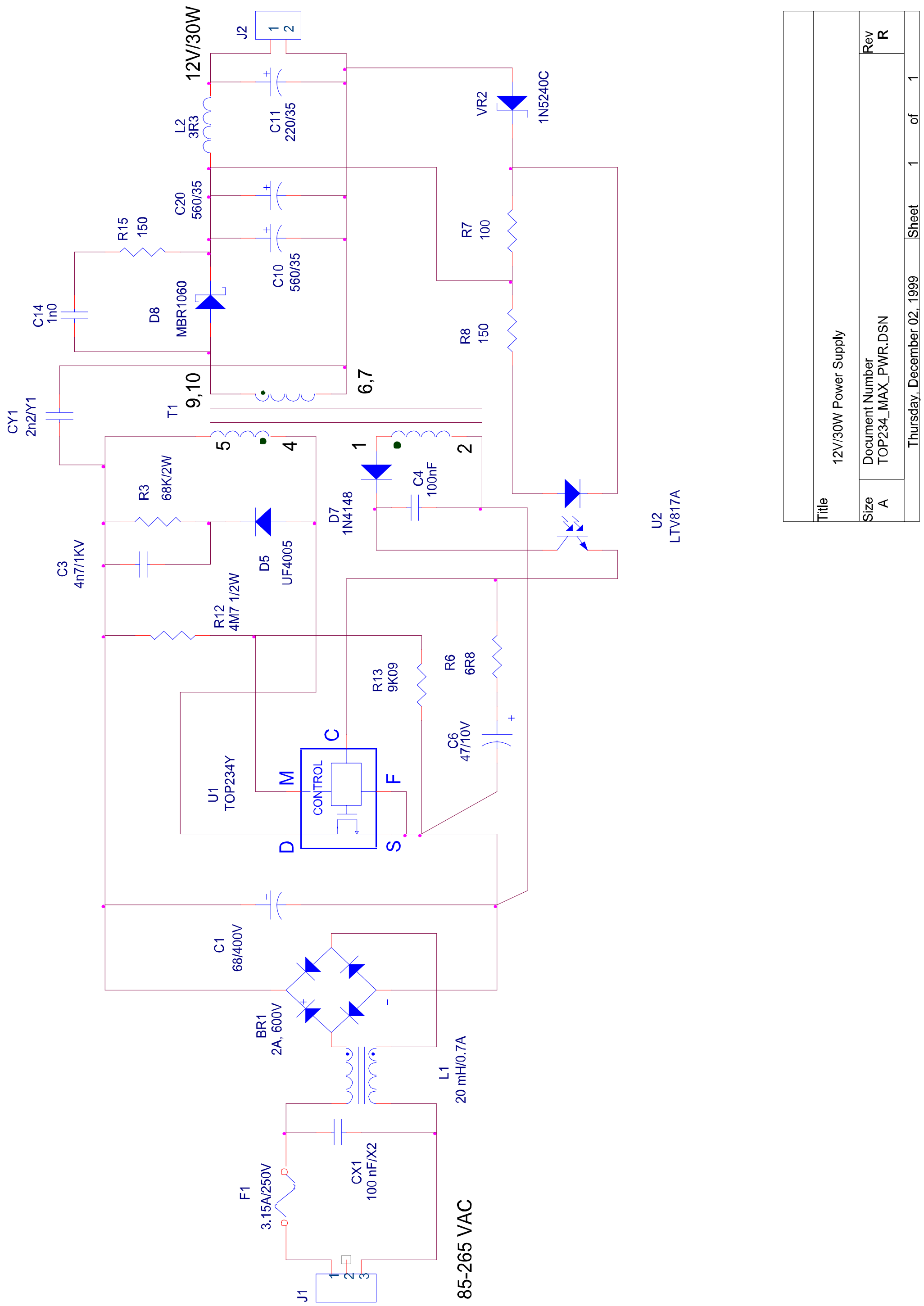
This document details specification, construction details, and testing of a 12V, 30W universal input power supply utilizing the TOP234Y.

2.0 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
INPUT						
Input Voltage	**Vin**	85	115/230	265	VAC	
Input Frequency		47	50/60	63	Hz	
OUTPUT						
Output Voltage	**Vout**	11.4	12	12.6	VDC	
Output Ripple	**Vout_ripple**		80	120	mV p-p	Measured at maximum load, 0-20 MHz bandwidth
Output Current	**Iout**	0		2.5	ADC	
Load Regulation		-1%		+3%	% of Nominal Voltage*	0-100% Load
				+2%	% of Nominal Voltage*	10-100% Load
Line Regulation		-1%		+2%	% of Nominal Voltage*	Minimum to maximum input voltage
Total Regulation		11.16	12	12.84	VDC	
Total Output Power	**Pout**			30	W	
ENVIRONMENTAL						
Ambient Temperature	**Tamb**	0	25	50	ºC	Open Frame, Free Convection
Efficiency	η	78	82		%	
Safety						Designed to meet IEC950
Conducted EMI						CISPR22B Conducted

*Nominal output voltage for purposes of determining regulation limits is measured at 115 VAC input voltage, 1.0 A output current.

3.0 Schematic



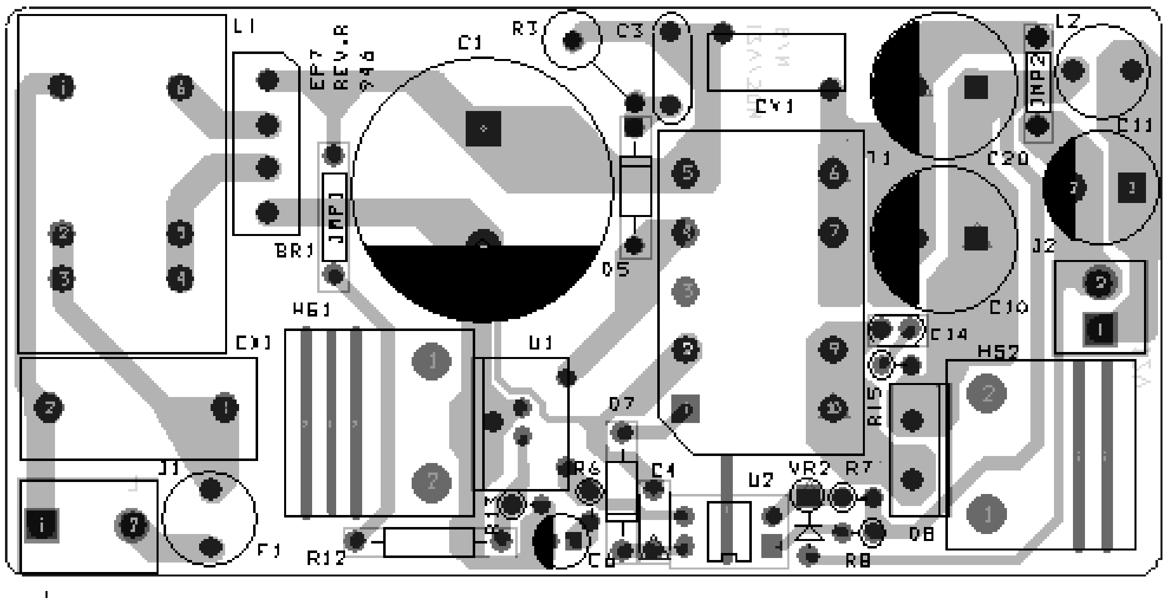
4.0 Circuit Description

The EP7 is a low-cost flyback switching power supply using the TOP234Y integrated circuit. The circuit shown in Figure 1 details a 12 V, 30 W power supply that operates from 85 to 265 VAC input voltage, suitable for applications requiring an open frame supply. The 12V output is directly sensed by optocoupler U2 and Zener diode VR2.
The output voltage is determined by the Zener diode (VR2) voltage and the voltage drops across the optocoupler (U2) LED and resistor R8. Other output voltages are also possible by adjusting the transformer turns ratios and value of Zener diode VR2.
AC power is rectified and filtered by BR1 and C1 to create the high voltage DC bus applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated high-voltage MOSFET within the TOP234Y. D5, R3, and C3 clamp the voltage spike caused by transformer leakage inductance to a safe value. The power secondary winding is rectified and filtered by D8, C10, C11, C20, and L2 to create the 12 V output voltage. C14 and R15 form a snubber circuit across D8 to reduce ringing. This improves conducted RFI performance of the supply at high frequency (15-20 MHz) and reduces leakage spikes, improving the reliability of D8. The combined voltage drops of VR2, U2 input LED, and R8 determine the output voltage of the supply. R7 provides bias current for Zener VR2 to improve regulation. The bias winding is rectified and filtered by D7 and C4 to create a bias voltage to power the TOP234Y. L1 and capacitor CY1 attenuate common-mode emission currents caused by high-voltage switching waveforms on the DRAIN side of the primary winding and the primary to secondary capacitance. L1 and CX1 attenuate differential-mode emission currents caused by the fundamental and harmonics of the primary current waveform. C6 filters internal MOSFET gate drive charge current spikes on the CONTROL pin, determines the auto-restart frequency, and together with R6 and R8, compensates the control loop.
The *TOPSwitch-FX* IC series provides new operating features and extended specifications. The EP7 demonstration supply is designed to exploit several of these features. R13, connected to the MULTIFUNCTION pin of TOPSwitch U1, can be used to adjust the current limit from 40% to 100% of its nominal value. This allows use of a smaller transformer core and/or higher transformer primary inductance for a given output power, reducing transformer size and *TOPSwitch* power dissipation, while at the same time avoiding transformer core saturation during startup conditions. The R13 value used in EP7 reduces the *TOPSwitch* current limit to approximately 70% of its nominal value. R12 provides a voltage feedforward signal to the MULTFUNCTION pin of U1, reducing the *TOPSwitch* current limit as an inverse function of input line voltage. This limits the maximum available power at high line, and along with the current limit reduction provided by R13, allows use of an RCD snubber circuit to limit the *TOPSwitch* drain voltage with adequate margin under worst-case operating conditions. *TOPSwitch-FX* provides extended maximum duty cycle (75% vs. 64% for *TOPSwitch-II*). This allows use of a smaller input capacitor (C1), and higher primary to secondary turns ratio for T1. This reduces the *TOPSwitch* peak operating current and the peak reverse voltage of

secondary rectifier D8. As a result, a 60V Schottky rectifier can be used for a 12V output with adequate operating margin.

The *TOPSwitch-FX* control circuit allows the switch to skip cycles at light or zero load conditions, in many cases eliminating the need for a preload resistor to control the output voltage at low/zero load.

5.0 Layout


L1
EP7
REV.A
9/98
C1
R3
C3
CY1
T1
C20
L2
JMP2
C11
J2
C10
BR1
JMP1
D5
HS1
CX1
U1
D7
C14
HS2
R15
J1
F1
R12
R6
C4
U2
VR2
R7
C6
R8
D8

6.0 Bill of Materials

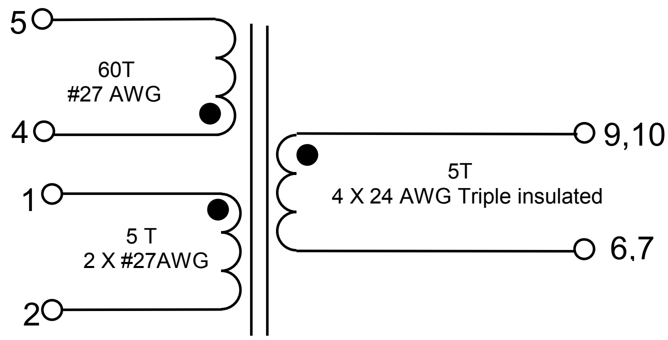
BOM for EP7 30W/12V TOP234 Supply

Item	Qty.	Ref	Description	Manufacturer	Part Number
1	1	U1		Power Integrations	TOP234Y
2	1	U2	Optocoupler, controlled CTR	Liteon	LTV817A
3	1	VR2	Zener, 10V 500 mW, 2%	American Power Devices	1N5240C
4	1	BR1	600V, 2A	General Instruments	2KBP06M
5	1	D5	600V, 1A, UFR	General Instruments	UF4005
6	1	D7	Diode, 75V		1N4148
7	1	D8	60V, 10A, Schottky	Motorola	MBR1060
8	1	CX1	X2 capacitor, 100nF	Roederstein	F1772-401-2000
9	1	C1	68 uF, 400V, 85C 22 X 25 mm	Panasonic	ECO-S2GP680BA
10	1	C3	Ceramic disk, 4.7 nF/1KV		
11	1	C4	100 nF, 50V, ceramic		
12	1	C6	47 uF/10V 105C	Panasonic	ECE-A1AGE470
13	1	CY1	2.2nF Y1	Cera-Mite	440LD22
14	2	C10,20	560 uF, 35V Lo ESR	Panasonic	ECA-1VFQ561
15	1	C11	220 uF, 35V 105C	Panasonic	ECE-A1VGE221
16	1	C14	1 nF, 100V, ceramic		
17	1	T1	Transformer, EF25	see documentation	
18	1	L1	Balun, 22mH/0.8A	Panasonic	ELF-18N008A
19	1	L2	3.3 uH, 5.5A	Toko	622LY3R3M
20	1	F1	Fuse, 3.15A/250VAC	Wickman	19372-3.15A
21	1	R3	68K/2W, 5%		
22	1	R6	6R8 /1/4W, 5%		
23	1	R7	100 /1/4W, 5%		
24	2	R8,15	150 /1/4W, 5%		
25	1	R12	4.7M/1/2W, 5%		
26	1	R13	9.09K / 1%		
27	2	HS1,2	Heatsink, TO-220	Thermalloy	6390B
28	1	J1*	Header 0.156” spacing, 3 pos	Molex	26-48-1035
29	1	J2	Header 0.156” spacing, 2 pos	Molex	26-48-1025

*remove middle pin

7.0 Transformer Drawing

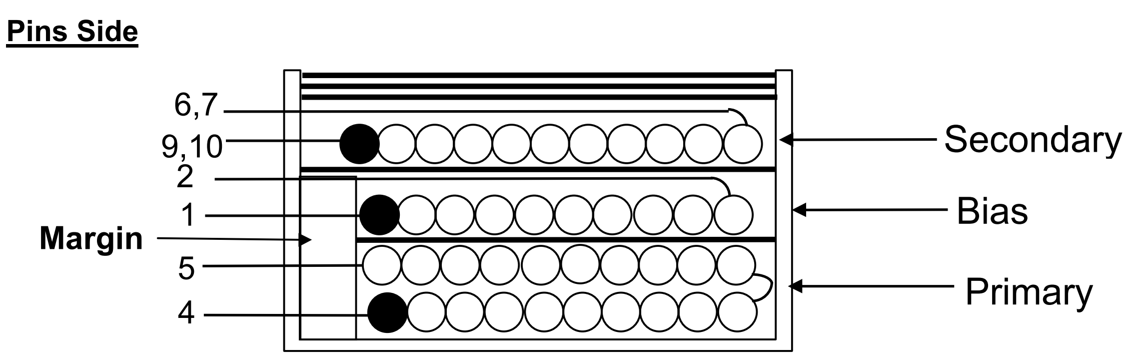
Transformer, T1



ELECTRICAL SPECIFICATIONS:

Electrical Strength	60Hz 1 minute, from Pins 1-5 to Pins 6-10	3000 VAC
Creepage	Between Pins 1-5 and Pins 6-10	6.4 mm (Min.)
Primary Inductance	Pins 4-5, all other windings open, measured at 100KHz	1016 μH, $\pm$10%
Resonant Frequency	Pins 4-5, all other windings open	570 KHz (Min.)
Primary Leakage Inductance	Pins 4-5, with Pins 6-10 shorted, measured at 100KHz	28 μH (Max.)

TRANSFORMER CONSTRUCTION

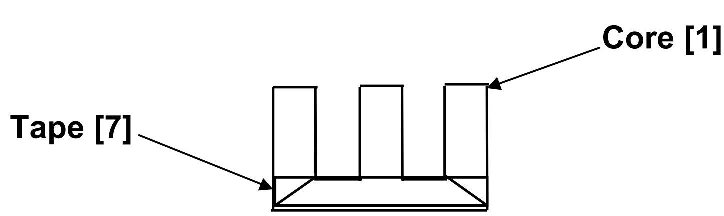


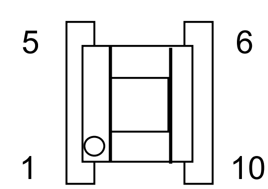
MATERIALS

Item	Description
[1]	Core: EF25, Siemens N67 material or equiv. Gapped for A_L of 282 nH/T^2
[2]	Bobbin: 10 pin EF25, Vertical Mount, Miles-Platts FE0100 w/TBS-601 pins
[3]	Magnet Wire: #27 AWG Double Coated
[4]	Triple Insulated Wire: #24 AWG
[5]	Tape, 3M # 44 or equiv. 1.5mm wide (min)
[6]	Tape, 3M #1298 or equiv. 14.2 mm wide
[7]	Tape, 3M #1298 or equiv. 15.7 mm wide
[8]	Varnish

WINDING INSTRUCTIONS:

Bobbin Preparation	Remove Pin 8 on bobbin [2] to provide polarization. Bobbin pinout is shown below.
Primary Margin	Apply 1.5 mm wide margin to pin side of bobbin using item [5]. Match height of primary and bias windings.
Primary	Start at Pin 4. Wind 60 turns of item [3] in approximately 2 layers. Finish on Pin 5.
Basic Insulation	Use one layer of item [6] for basic insulation.
Bifilar Bias winding	Starting at pin 1, wind 5 bifilar turns of item [3]. Spread turns evenly across bobbin. Finish at pin 2.
Basic Insulation	Use one layer of item [7] for basic insulation.
12V Quadrifilar Secondary Winding	Start at Pins 9 and 10. Wind 5 quadrifilar turns of item [4] (about 1.2 layers). Spread turns evenly across bobbin. Finish on Pins 6 and 7.
Outer Wrap	Wrap windings with 3 layers of tape [item [7].
Core Preparation	Wrap bottom of one E core [1] with 2 layers of tape [7] as shown.
Final Assembly	Assemble and secure core halves so that the tape wrapped E core is at the bottom of the transformer. Varnish impregnate (item [8]).





Bobbin Pinout (Top View)

Design Notes:

Power Integrations Device	TOP234Y
Frequency of Operation	130 KHz
Mode	Continuous
Peak Current	0.87 A
Reflected Voltage (Secondary to Primary)	150V
Maximum DC Input Voltage	375
Minimum DC Input Voltage	82

7.1 Transformer Spreadsheet

Note: This transformer spreadsheet was designed for use with *TOPSwitch* and *TOPSwitch-II,* and does not take into account the extended duty cycle range of TOPSwitch-FX, or its capability for external current limit trimming via the MULTIFUNCTION pin. As such, the spreadsheet shows error messages for Dmax, Bp, and VDRAIN. In fact, the Dmax shown is well within the capability of *TOPSwitch-FX*, and the current limit has been trimmed externally to 70% of nominal, avoiding transformer saturation during startup. The current limit trimming features, along with the RCD clamp used in this design also help to keep the absolute peak DRAIN voltage less than 650V. When these discrepancies are taken into account, the spreadsheet is still a useful guide for transformer design. These discrepancies will be corrected in a *TOPSwitch-FX* spreadsheet to be released in the near future.

Rev 3.1	INPUT		OUTPUT		ACDC_TOP_REV3_1_040899.xls: TOPSwitch Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					Optimized for 68 uF input capacitor
VACMIN	85			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
fS	120000	100000		Hertz	TOPSwitch Switching Frequency
VO	12			Volts	Output Voltage
PO	30			Watts	Output Power
n	0.78				Efficiency Estimate
Z	0.5				Loss Allocation Factor
VB	12			Volts	Bias Voltage
tC	3			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	68			uFarads	Input Filter Capacitor
ENTER TOPSWITCH VARIABLES					
TOPSwitch	TOP234			Universal	115/230V
Chosen Device	TOP234		Power Out	45W	75W
VOR	150			Volts	Reflected Output Voltage
ILIMITMAX	1.396	1.605		Amps	From TOPSwitch Data Sheet
VDS	10			Volts	TOPSwitch on-state Drain to Source Voltage
VD	0.5			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KRP/KDP	0.44				Ripple to Peak Current Ratio (0.4 < KRP < 1.0 : 1.0< KDP<6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					

Core	EF25				
Type					
Core Manuf					
Bobbin Manuf					
Core		EF25		P/N:	PC40EF25-Z
Bobbin		#N/A		P/N:	#N/A
AE		0.518		cm^2	Core Effective Cross Sectional Area
LE		5.78		cm	Core Effective Path Length
AL		2000		nH/T^2	Ungapped Core Effective Inductance
BW	15.7	15.7		mm	Bobbin Physical Winding Width
M	0.75			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	1.9				Number of Primary Layers
NS	5				Number of Secondary Turns

DC INPUT VOLTAGE PARAMETERS

VMIN			81	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage

CURRENT WAVEFORM SHAPE PARAMETERS

DMAX	Warning		0.68		!!!!!!!!!! REDUCE DMAX Dmax<0.60 (increase CIN, decrease VOR)
IAVG			0.48	Amps	Average Primary Current
IP			0.90	Amps	Peak Primary Current
IR			0.40	Amps	Primary Ripple Current
IRMS			0.59	Amps	Primary RMS Current

TRANSFORMER PRIMARY DESIGN PARAMETERS

LP			1016	uHenries	Primary Inductance
NP			60		Primary Winding Number of Turns
NB			5		Bias Winding Number of Turns
ALG		282		nH/T^2	Gapped Core Effective Inductance
BM			2951	Gauss	Flux Density at PO, VMIN
BP	Warning		5408	Gauss	!!!!!!!!!! REDUCE BP<4200 (increase NS,smaller TOPSwitch, larger Core,increase KRP)
BAC		655		Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur		1776			Relative Permeability of Ungapped Core
LG			0.20	mm	Gap Length (Lg >> 0.051 mm)
BWE		26.98		mm	Effective Bobbin Width
OD			0.45	mm	Maximum Primary Wire Diameter including insulation
INS		0.06		mm	Estimated Total Insulation Thickness (= 2 * film thickness)
DIA			0.39	mm	Bare conductor diameter
AWG			27	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM		203		Cmils	Bare conductor effective area in circular mils
CMA			347	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

TRANSFORMER SECONDARY DESIGN PARAMETERS

ISP			10.81	Amps	Peak Secondary Current
ISRMS			4.83	Amps	Secondary RMS Current
IO			2.50	Amps	Power Supply Output Current
IRIPPLE			4.13	Amps	Output Capacitor RMS Ripple Current
CMS		1675		Cmils	Secondary Bare Conductor minimum circular mils
AWGS			17	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS			1.15	mm	Secondary Minimum Bare Conductor Diameter
ODS			2.84	mm	Secondary Maximum Insulated Wire Outside Diameter
INSS		0.84		mm	Maximum Secondary Insulation Wall Thickness

VOLTAGE STRESS PARAMETERS

VDRAIN	Warning		710	Volts	!!!!!!!!!! REDUCE DRAIN VOLTAGE Vdrain<680
PIVS			43	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB			44	Volts	Bias Rectifier Maximum Peak Inverse Voltage

8.0 Performance Data

All data collected on EP7 Sample 1.

8.1 Efficiency

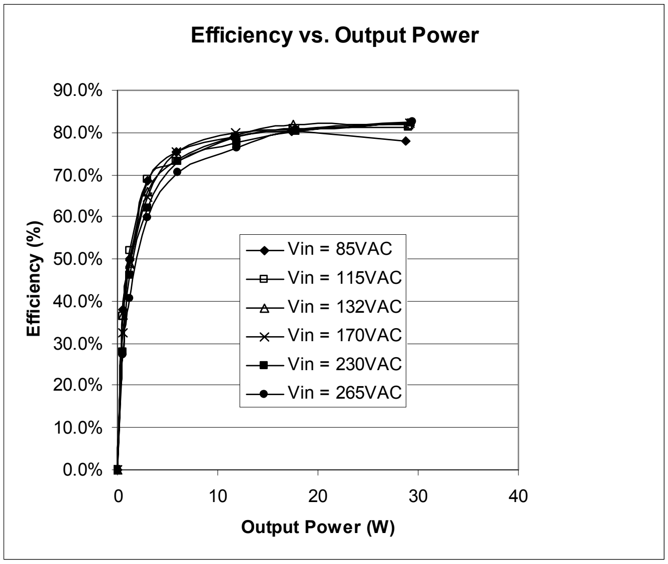


Figure 8.1.1. Efficiency vs. Output Power, EP7, Room Temperature, 60Hz AC Line Frequency

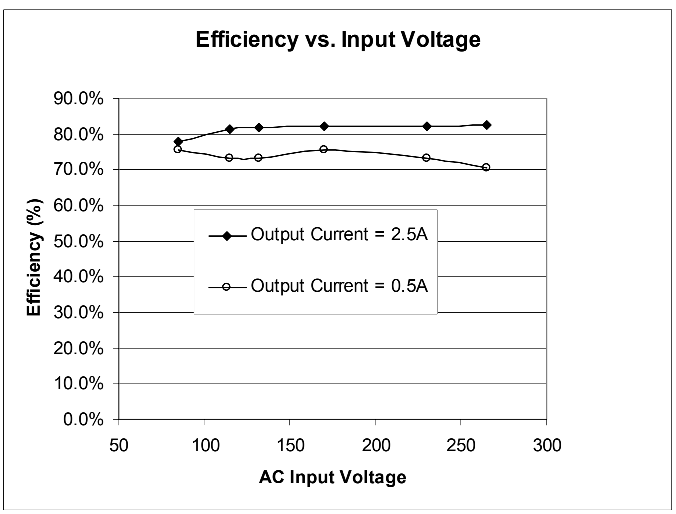


Figure 8.1.2. Efficiency vs. Input Voltage, EP7, Room Temperature, 60 Hz AC Line Frequency

8.2 Regulation

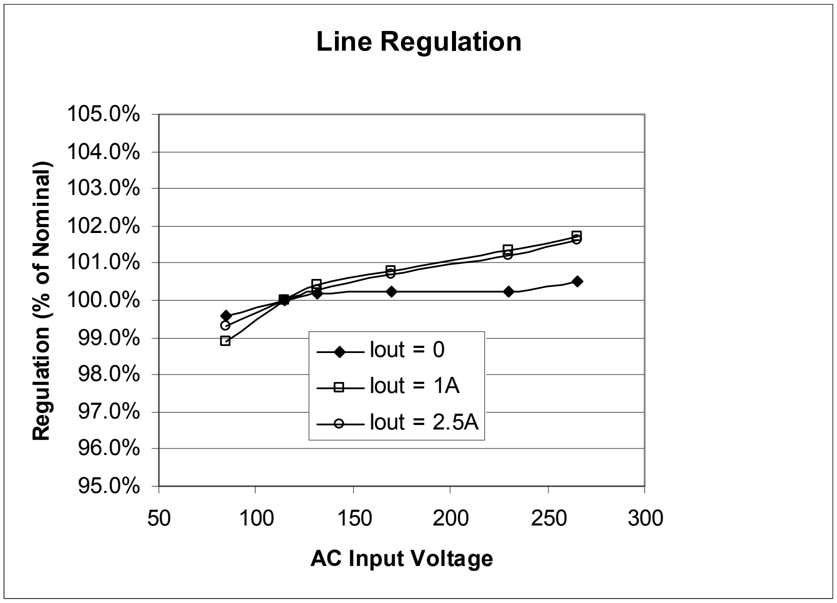


Figure 8.2.1. Regulation vs. Input Voltage (Nominal Voltage is measured at 115VAC Operating Point for each output current range).

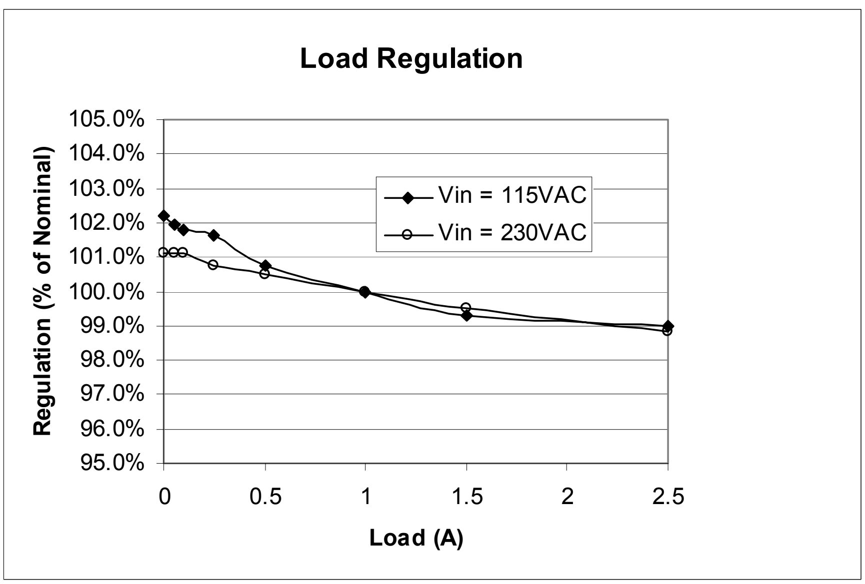


Figure 8.2.2. Load Regulation (Nominal voltage is measured at 1A operating point for each input voltage).

8.3 Temperature

85 VAC Input, 30W Output	**High Temperature**	**Low Temperature**
Ambient	**48ºC**	**25ºC**
Internal Enclosure Temperature	54ºC	28ºC
TOPSwitch	119ºC	94ºC
Output Diode	77ºC	64ºC
Transformer	86ºC	66ºC

8.4 Waveforms

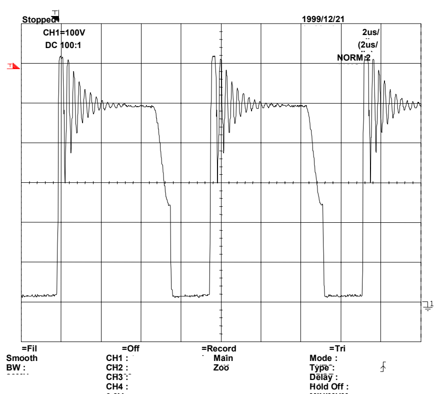


Figure 8.4.1. Peak Drain Voltage at Maximum Load, 265VAC Input Voltage (100 V/div, 2 usec/div)

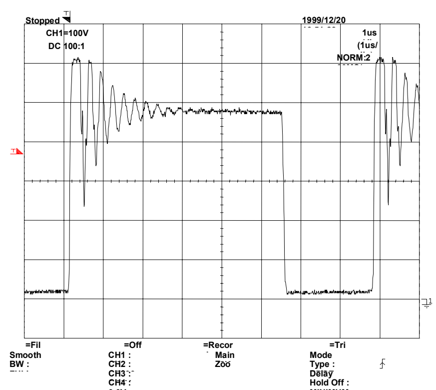


Figure 8.4.2. Peak Drain Voltage at 265VAC,with Output Load set just before autorestart. (100 V/div, 2 usec/div).

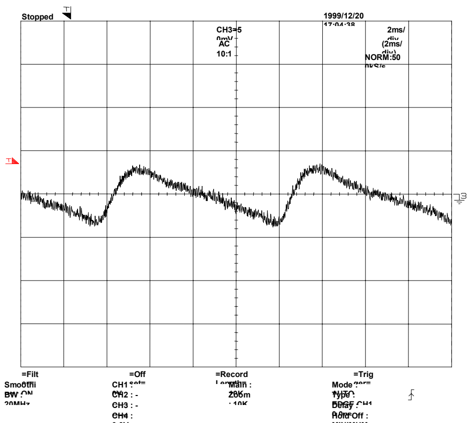


Figure 8.4.3. Output Ripple, at 85VAC, 30W Load (50 mV/div, 20 MHz bandwidth)

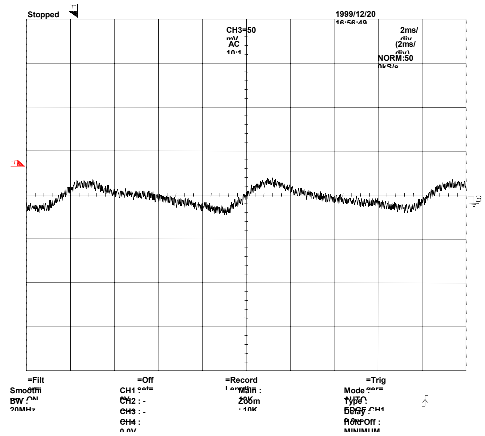


Figure 8.4.4. Output Ripple at 115VAC, 30W Load (50 mV/div, 20 MHz bandwidth).

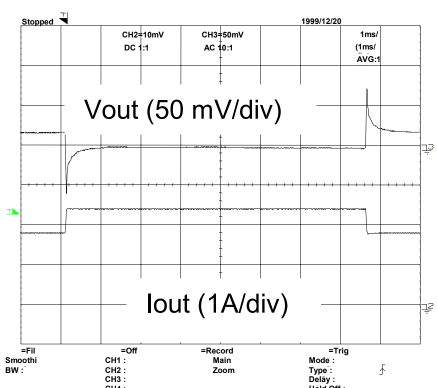


Figure 8.4.5. Output Transient Response, 75-100% Load, 115VAC, Averaged Waveform, 2 msec/div.

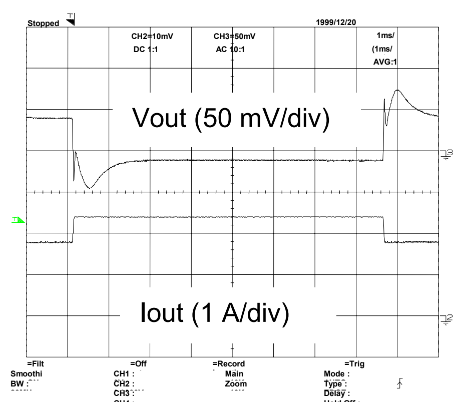


Figure 8.4.6. Output Transient Response, 75-100% Load, 230VAC, Averaged Waveform, 2 msec/div.

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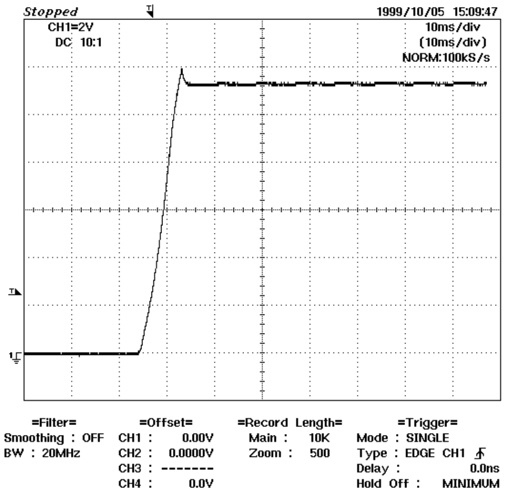


Figure 8.4.7. Output Startup Transient, 30W Load, 85 VAC Input.

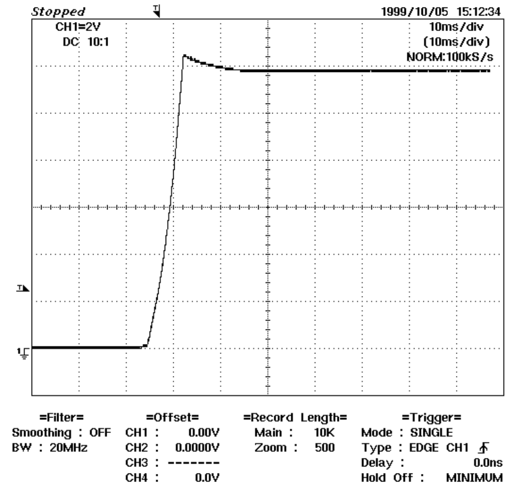


Figure 8.4.8. Output Startup Transient, Zero Load, 85 VAC Input

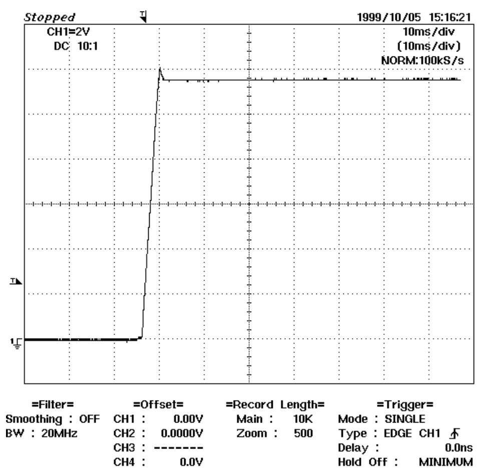


Figure 8.4.9, Output Startup Transient, 30W Load, 265 VAC Input.

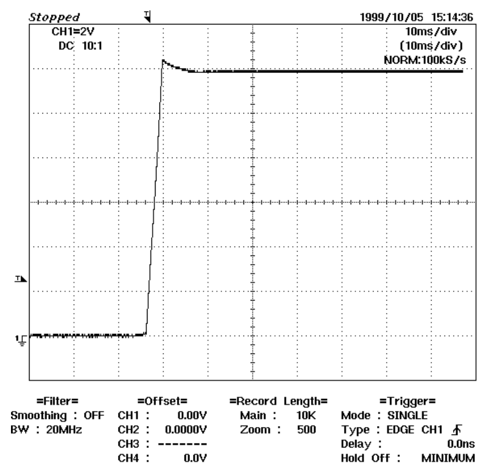


Figure 8.4.10, Output Startup Transient, Zero Load, 265 VAC Input

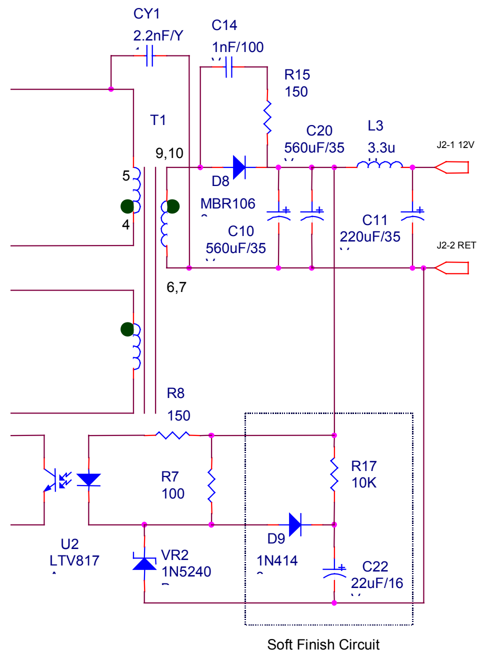
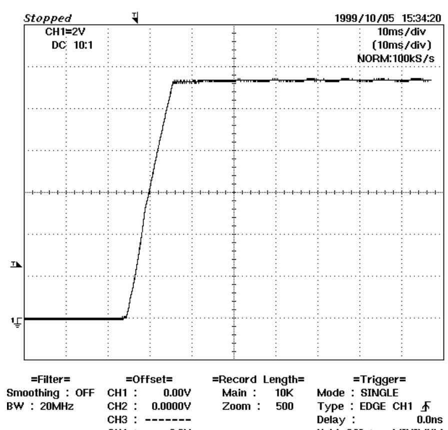
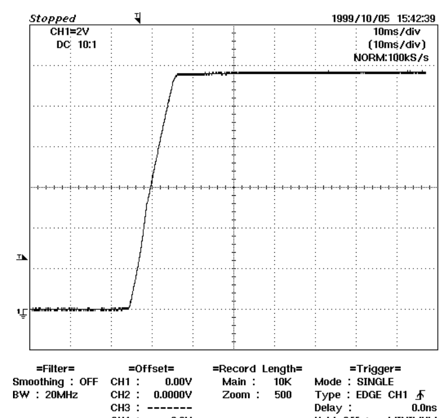


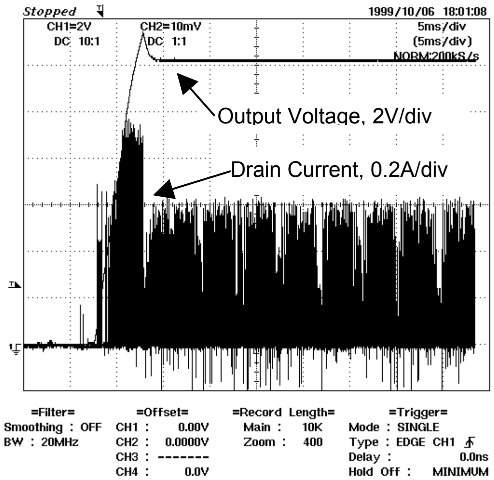
Figure 8.4.11. Soft Finish Circuit for Eliminating Output Overshoot at Startup



8.4.12. Output Startup Transient with Soft FinishCircuit, 30W Load, 85 VAC Input

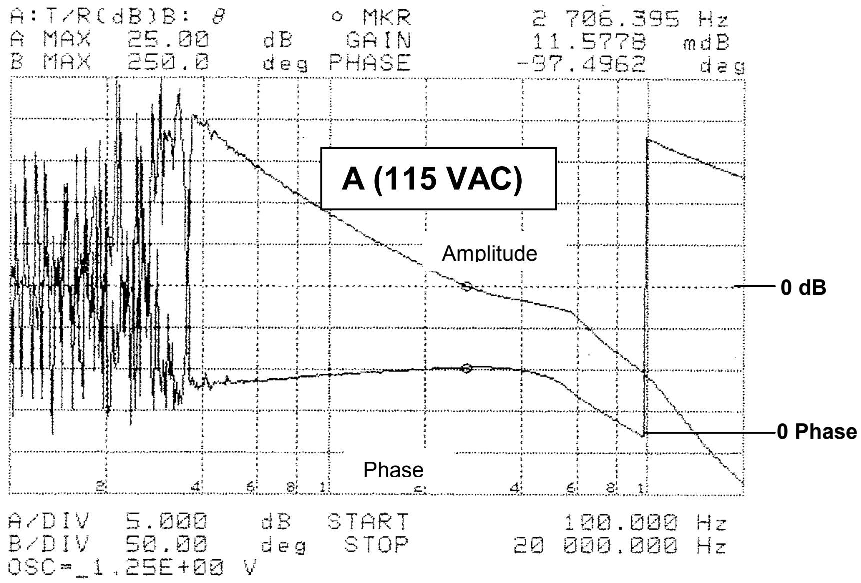


8.4.13. Output Startup Transient with Soft FinishCircuit, Zero Load, 85 VAC Input



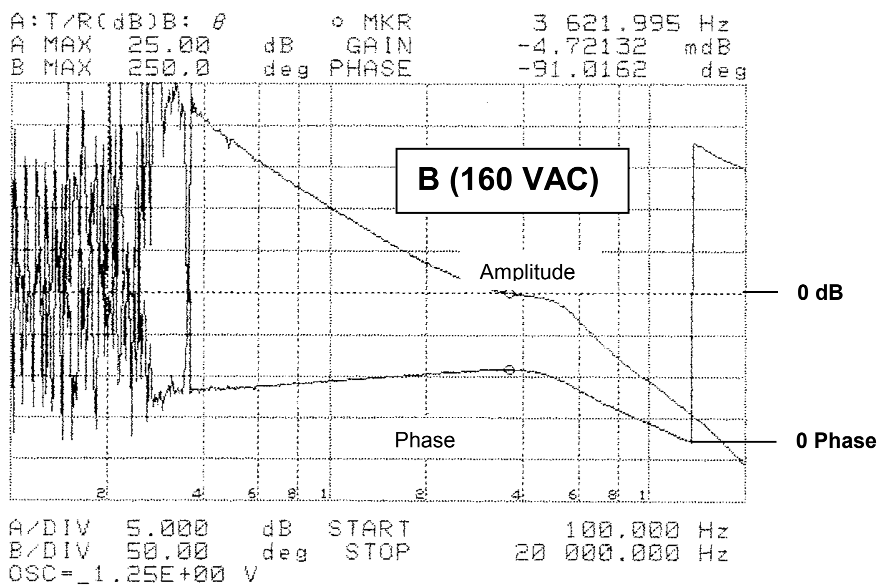
8.4.14. Drain Current vs. Output Voltage Startup Profile, 265VAC (worst case), no soft finish network.

8.5 Frequency Response



Gain
Crossover – 2.7 kHz

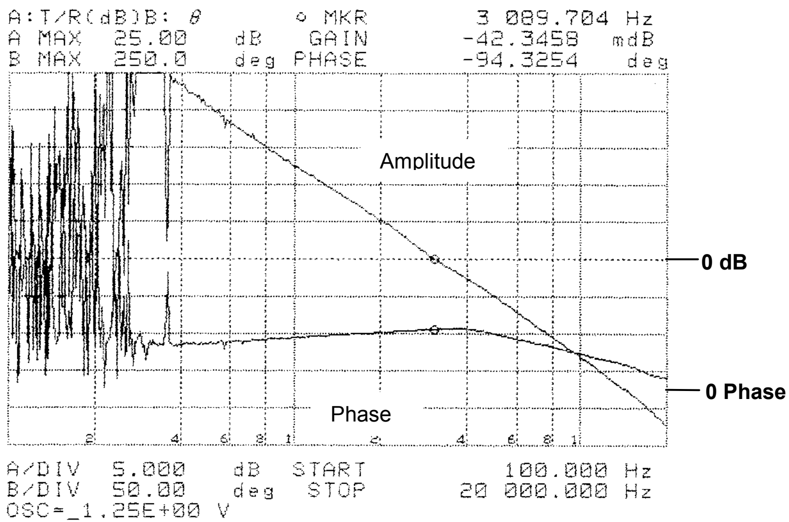
Phase Margin - 83º



Gain
Crossover – 3.6 kHz

Phase Margin - 89º

8.5.1. Frequency Response at 115VAC, maximum load (A), and 160VAC (maximum input voltage for continuous mode operation), maximum load (B).



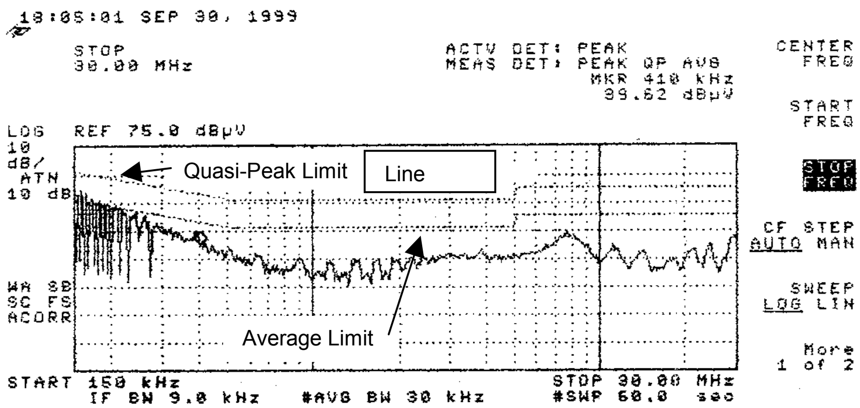
Gain
Crossover – 3 kHz

Phase Margin - 86º

Figure 8.5.2. Frequency Response at 230VAC, Maximum Load (supply is operating in discontinuous mode)

8.6 Conducted EMI Scans

The attached plots show EMI performance for the EP7 as compared to CISPR22B conducted emissions limits. Initial results are shown for scans using peak detection. Peak detection is commonly used for initial diagnosis of EMI, as full range results can be quickly obtained using a common spectrum analyzer. This is also a worst-case form of analysis, as the CISPR22B limits are based on quasi-peak and average detection, both of which give lower amplitude results than peak detection.



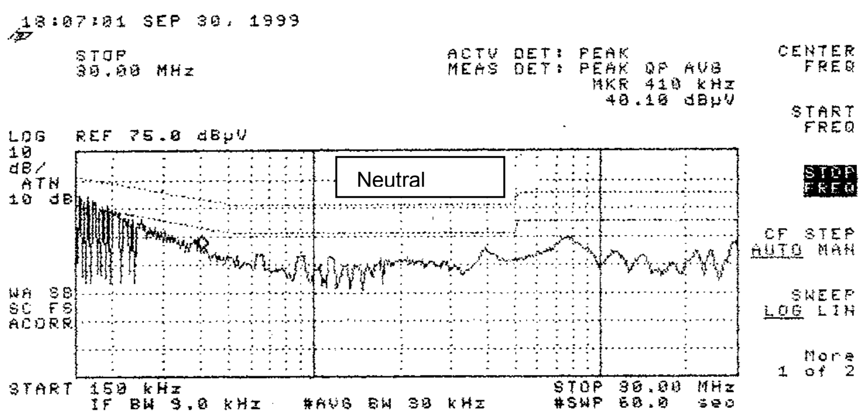


Figure 8.6.1 Conducted EMI, Peak Scan, CISPR22B Limits, Full Load, 115VAC, line and neutral. Peak scan is slightly above CISPR22B Average limit at 150-200 kHz.

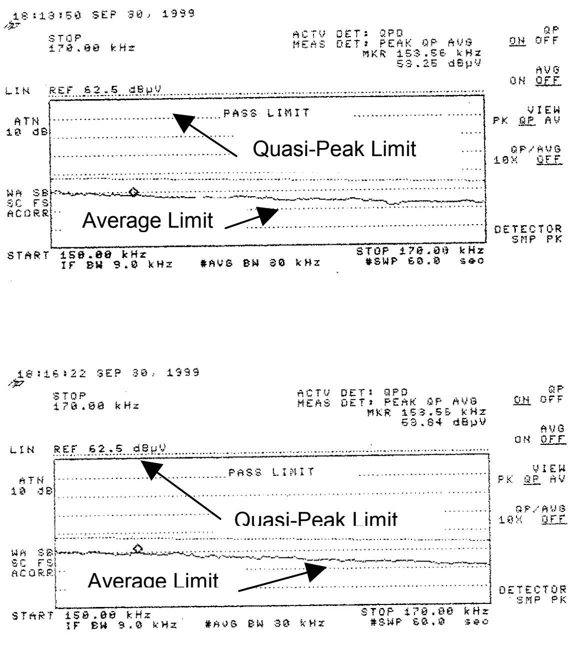


Figure 8.6.2. 115V Quasi-peak scan of 150-170 kHz region at shows compliance with CISPR22B Quasi-peak limits. (margin > 12 dB)

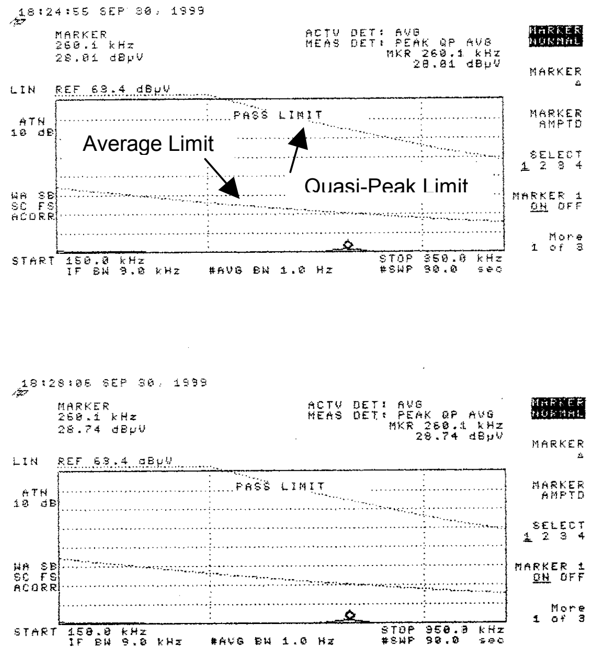
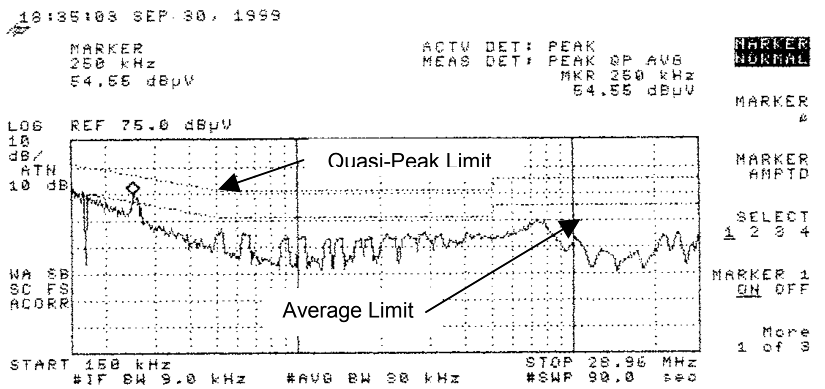


Figure 8.6.3. 115VAC Average Scan of 150-300 kHz region shows compliance with CISPR22B average limit (margin >18dB)



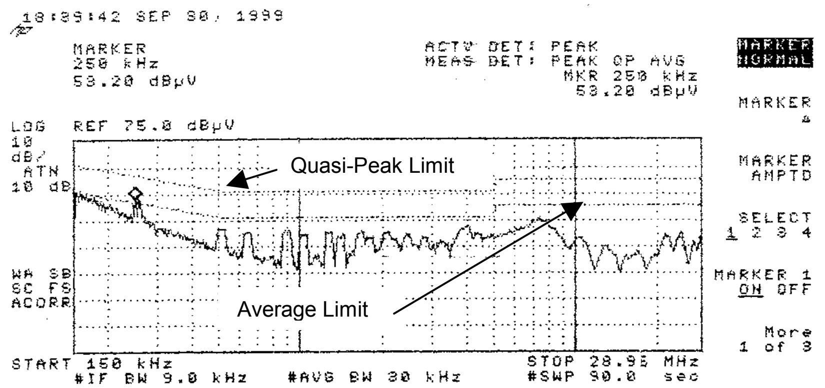
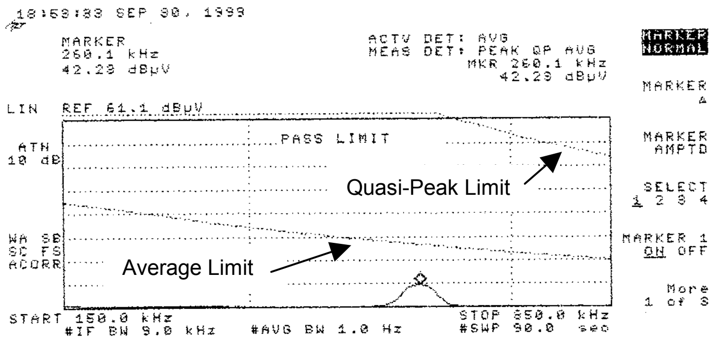


Figure 8.6.4. 230 VAC Conducted EMI, Peak Scan, CISPR22B Limits, Full Load, line and neutral. Peak scan is slightly above CISPR22B Average limit at 150-170 kHz and at 250-260 kHz.



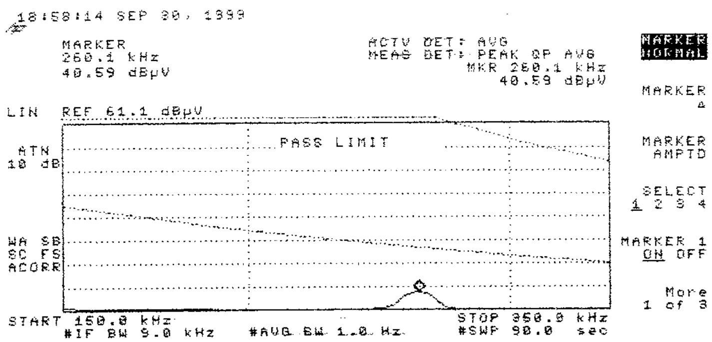


Figure 8.6.5. Average Scan of 150-300 kHz region
Shows compliance with CISPR22B average limit
(margin > 10dB)

Appendix A. Enhanced Regulation Circuit for EP7

Figure A.1 shows an alternate circuit for the EP7 that provides higher efficiency, improved regulation, and lower output ripple than the standard EP7 circuit. In the standard EP7, the value of R8 must be relatively large (150 ohms) in order to assure loop stability. The extra voltage drop across this resistor deteriorates both line and load regulation, and shifts the output voltage set point, forcing the use of a lower zener voltage with higher bias current to center the output at 12V. This reduces the overall efficiency of the supply. A smaller resistor value can be used for R8 if extra compensation is added. In the circuit of Figure A.1, R8 is reduced to 47 ohms from 150 ohms, reducing the output error and increasing the loop gain. R18 and C23 provide high frequency compensation. The performance of this circuit is shown in Figures A.2 through A.13.

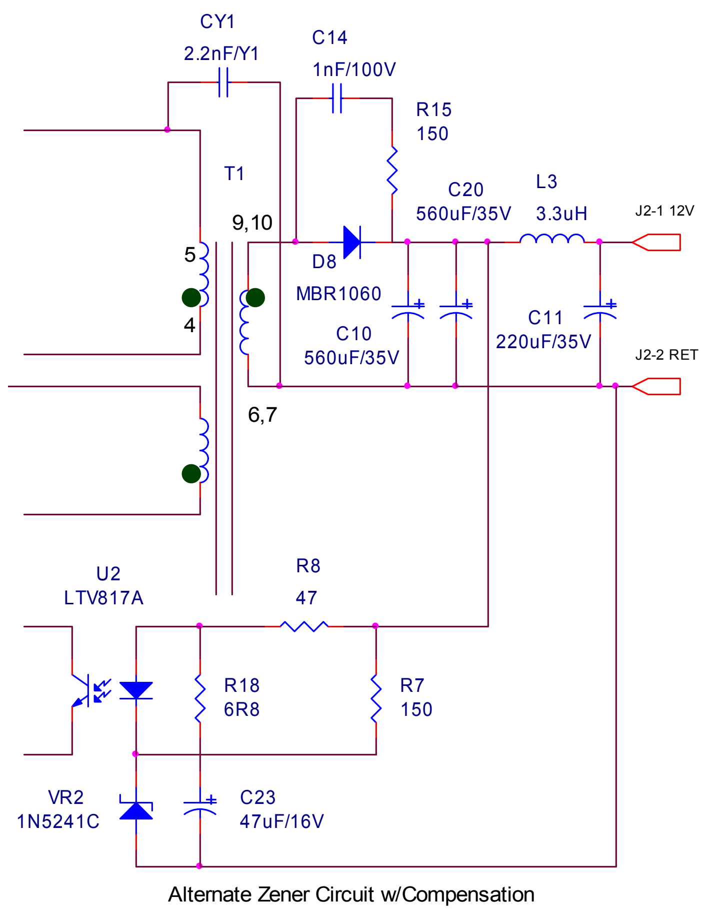


Figure A.1. Enhanced Regulation Circuit for EP7

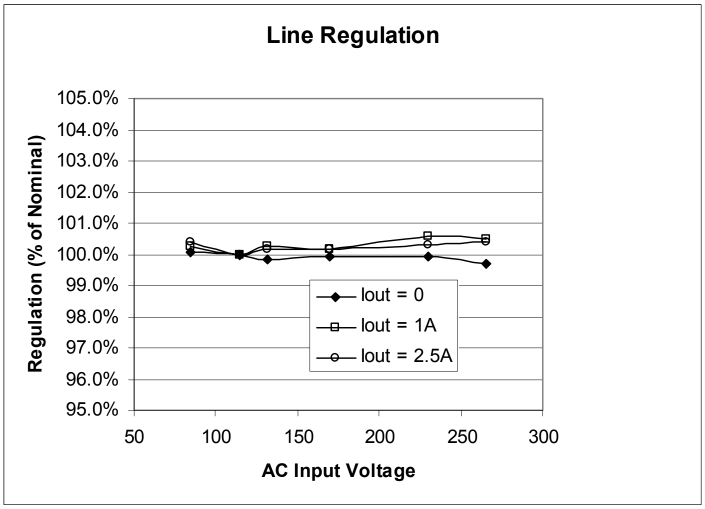


Figure A.2. Line Regulation for EP7 with Enhanced Regulation Circuit

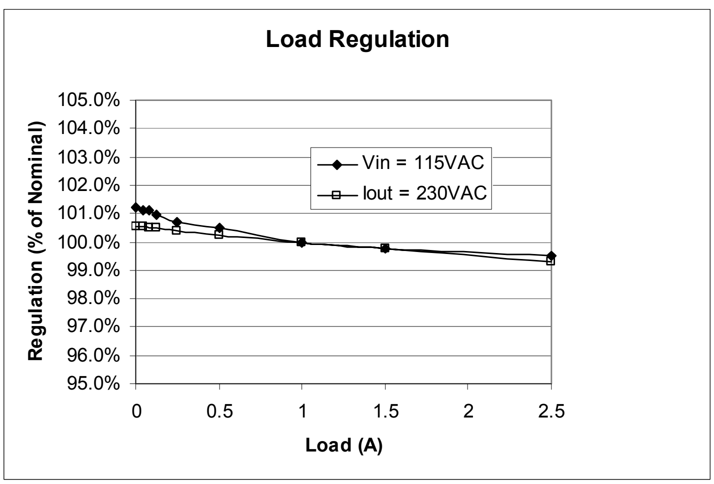


Figure A.3. Load Regulation for EP7 with Enhanced Regulation Circuit

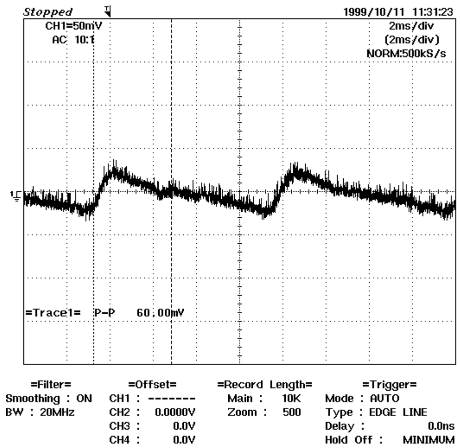


Figure A.4. Output Ripple at Maximum Load,85VAC Input, EP7 Enhanced Regulation Circuit (50 mV/div)

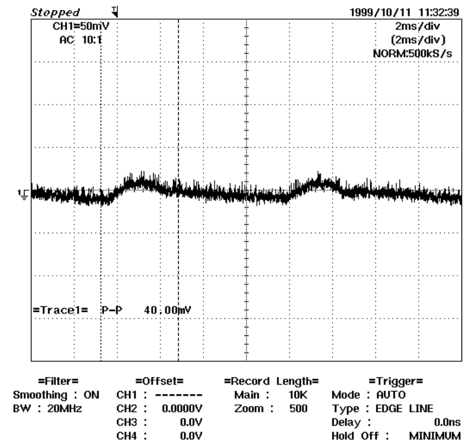


Figure A.5. Output Ripple at Maximum Load,115VAC Input, EP7 Enhanced Regulation Circuit (50 mV/div)

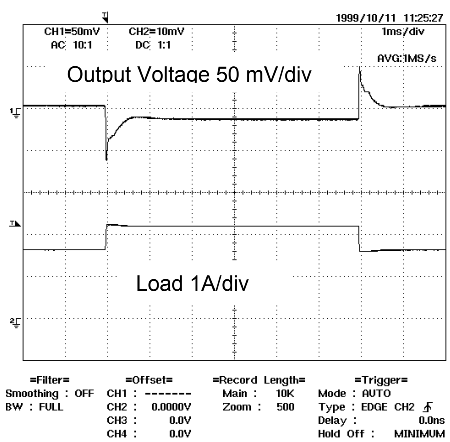


Figure A.6. Load Transient Response, 115VAC Input, EP7 Enhanced Regulation Circuit (Averaged Waveform).

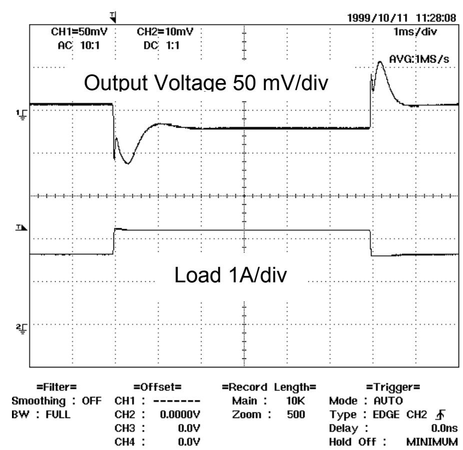


Figure A.7. Load Transient Response, 230VAC Input, EP7 Enhanced Regulation Circuit(Averaged Waveform)

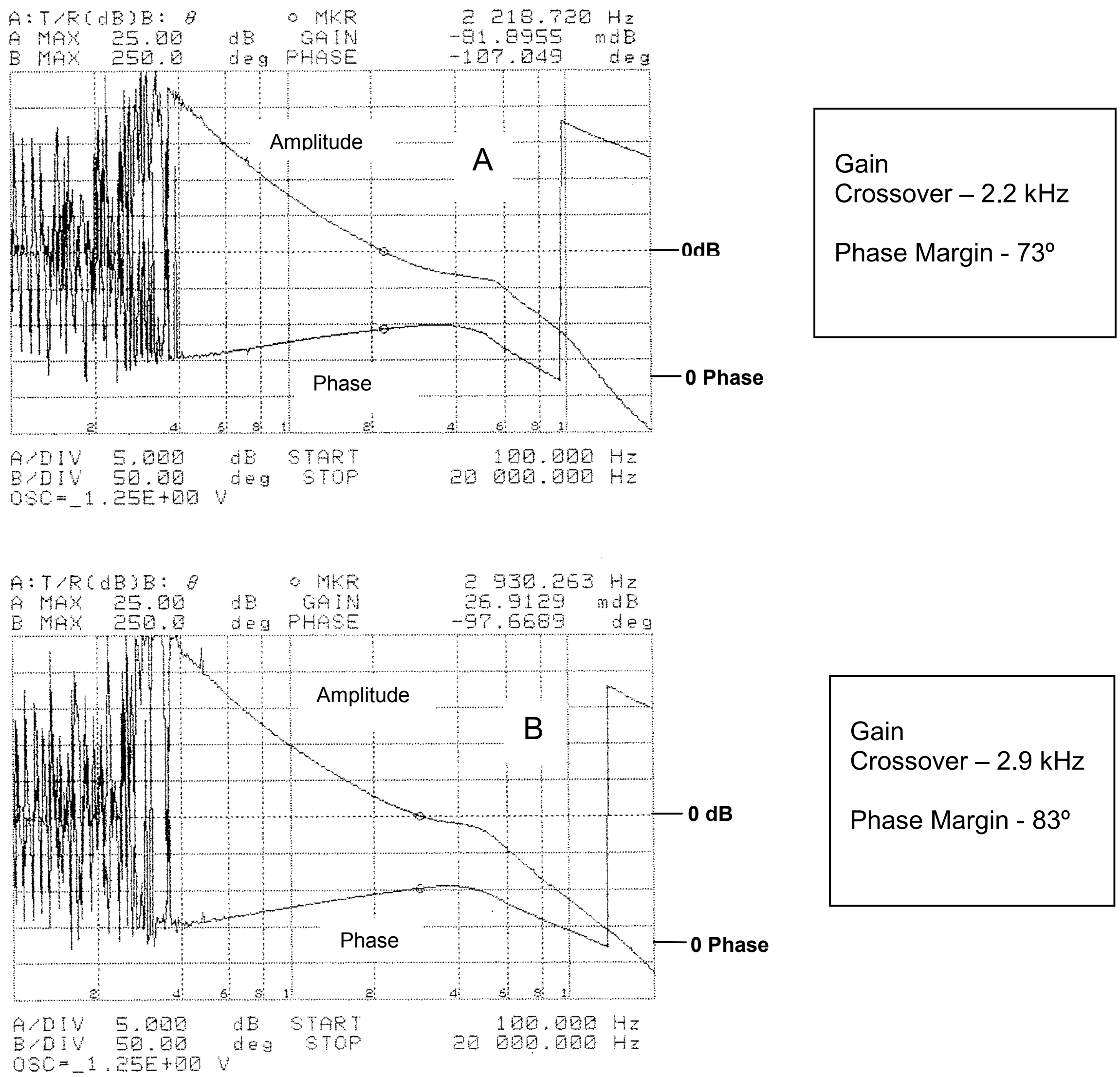
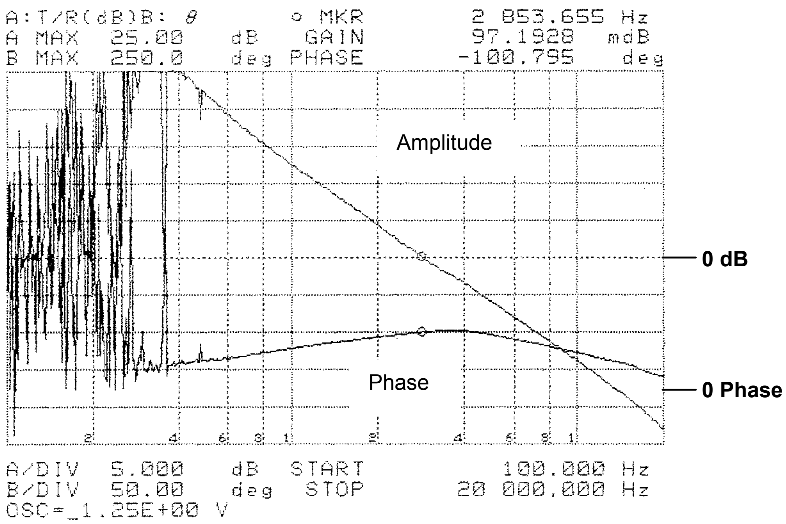


Figure A.8. Frequency Response for Enhanced EP7, Maximum Load, 115VAC (A), and 160VAC (B).



Gain
Crossover – 2.8 kHz

Phase Margin – 79.3º

Figure A.9. Frequency Response for Enhanced EP7, Maximum Load, 230VAC.

Author	Date	Rev	Description
R. H.	09/29/99	1	Original draft
R. H.	10/11/99	2	Second Draft – Added Appendix A
R. H.	10/13/99	3	Third draft
R.H.	12/21/99	4	Production release