Title	***Engineering Prototype Report (EP-25) - LCD Monitor Power Supply with TOP247Y***
Specification	12 V, 45 W
Customer	
Application	LCD Monitor
Author	RH
Document Number	EPR-25
Date	01-May-2002
Revision	1.0

Objective

This report presents a design and performance data for a 12 V, 45 W LCD monitor power supply using the TOP247Y.

- High Efficiency (82% at 90 VAC)
- Extremely Low EMI – Passes FCC Part 15, Class B with Margin
- Low Zero Load Power Consumption
  (< 0.35 W @ 115 VAC, < 0.45 W @ 230 VAC)
- Overload Protection Limits Power Delivery at High Line

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Important Note:
Although the EP-25 is designed to satisfy safety isolation requirements, this engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report for a 12 V, 45 W LCD monitor power supply design using the TOP247Y, and contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit board layout, and performance data.

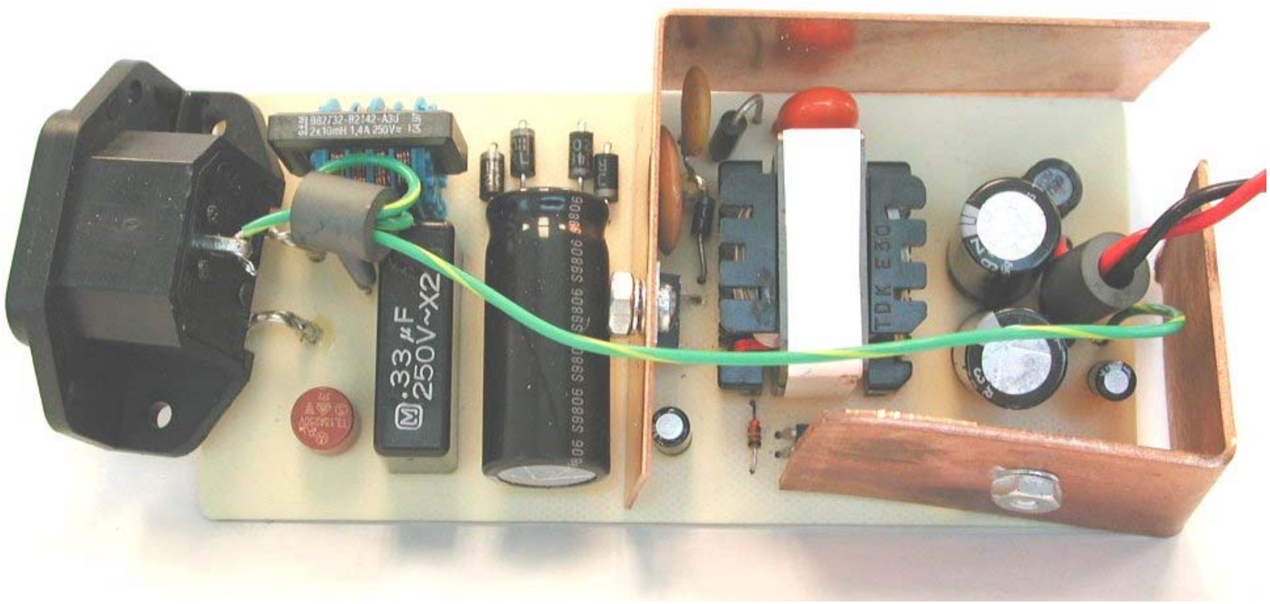

Figure 1 – EP-25 Populated Circuit Board.

2 Power Supply Specification

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	90		265	VAC	3 Wire
Frequency	f_{LINE}	47	50/60	64	Hz	
No-load Input Power (230 VAC)				0.5	W	
Output						
Output Voltage 1	V_{OUT1}	11.4	12.00	12.6	V	± 5%
Output Ripple Voltage 1	$V_{RIPPLE1}$			120	mV	20 MHz Bandwidth
Output Current 1	I_{OUT1}	0	3.75	3.75	A	
Total Output Power						
Continuous Output Power	P_{OUT}			45	W	
Peak Output Power	P_{OUT_PEAK}			N/A	W	
Efficiency	η	82			%	Measured at P_{OUT} (45 W), 25 °C
Environmental						
Conducted EMI		PASS				Meets CISPR22B / EN55022B, FCC Part 15, Class B
Safety						Designed to meet IEC950, UL1950 Class II
Surge		4			kV	1.2/50 µs surge, IEC 1000-4-5, 12 Ω series impedance, differential and common mode
Surge		4			kV	100 kHz ring wave, 500 A short circuit current, differential and common mode
Ambient Temperature	T_{AMB}	0		50	°C	Free convection, sea level

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3 Schematic

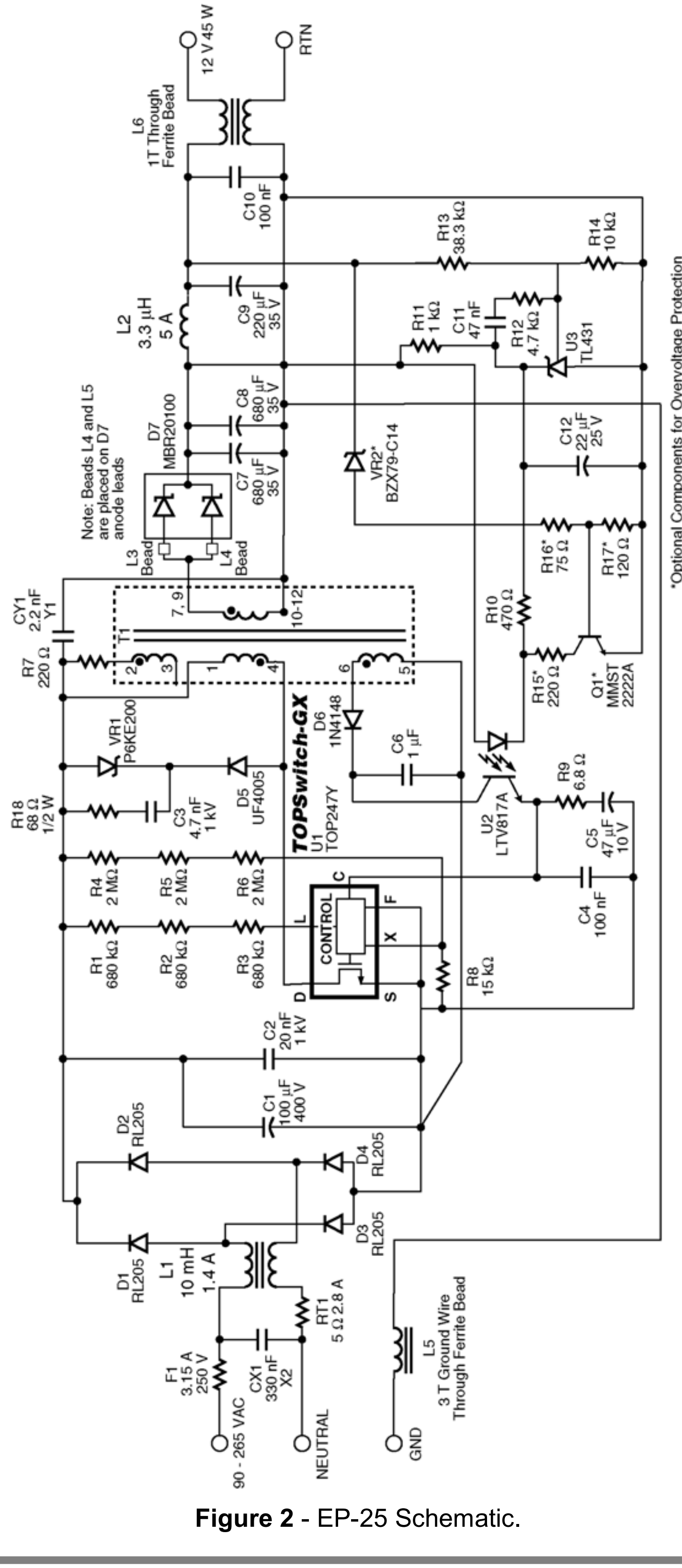

Figure 2 - EP-25 Schematic.

4 Circuit Description

4.1 Input Components

L1 and CX1 provide input EMI filtering for common mode and differential mode interference. L5 provides EMI filtering for the safety ground connection. F1 provides protection in case of an input component failure. RT1 limits inrush current at turn-on.
D1-D4 and C1 rectify and filter the input AC voltage. C2 provides high frequency decoupling for the high voltage DC bus to reduce high frequency EMI.

4.2 Primary Components

The high voltage DC bus is fed to the DRAIN pin of *TOPSwitch-GX* U1 via the primary winding of T1. Resistors R1-R3 set the DC turn-on threshold of U1. R8 sets the current limit threshold of U1 to 60% of its rated value. Current limit reduction allows use of a lower cost, more continuous transformer with fewer turns for a given operating power, lowering cost and increasing efficiency. R4-R6 are used in conjunction with R8 to lower the U1 current limit as a function of AC input voltage. This keeps the ultimate power limit of the power supply almost constant over the entire input voltage range. D6 and C6 rectify and filter the bias winding of T1. Operating and control current for U1 is supplied via optocoupler U2. C5 provides start-up bias for U1, sets auto-restart frequency, and provides frequency compensation for the *TOPSwitch-GX*. R8 introduces a zero into the control loop frequency response to improve phase margin. C4 provides high frequency bypassing for the U1 CONTROL pin.

D6 and VR1 clamp the maximum voltage on the U1 DRAIN pin. C3 diverts current from the rising edge of the turn-off leakage spike away from VR1, lowering its power dissipation and increasing overall supply efficiency. R18 provides damping for C3 to limit drain voltage ringing.

The winding, at transformer T1 pins 2-3, provides EMI improvement, allowing use of a smaller common mode choke. R7 provides damping for this winding. CY1 provides a return path for common mode EMI coupled from primary to secondary via the interwinding capacitance of T1.

4.3 Output Rectification

Schottky diode D7 and capacitors C7-C8 rectify and filter the T1 output winding. Ferrite beads L3-L4 provide snubbing for D7 and reduce high frequency EMI. L2, C9, and C10 provide a second stage of output filtering to reduce high frequency output ripple to acceptable levels. L6 is a single-turn ferrite bead, common mode inductor placed on the supply output cable to reduce radiated EMI.

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4.4 Output Feedback

The supply output voltage is applied to the U3 reference pin via voltage divider R13-R14. The divider ratio and the U3 reference voltage set the supply output voltage. C11 and R12 provide frequency compensation for U3. R11 provides quiescent bias current for U3 to ensure linear operation. R10 sets the voltage to current transformation ratio for the input of optocoupler U2, setting the high frequency control loop gain. C12 provides open loop drive for the optocoupler during supply start-up, limiting output voltage slew rate at start-up, and eliminating output voltage start-up overshoot. Q1, VR1, and R15-R17 provide overvoltage protection.

5 PCB Layout

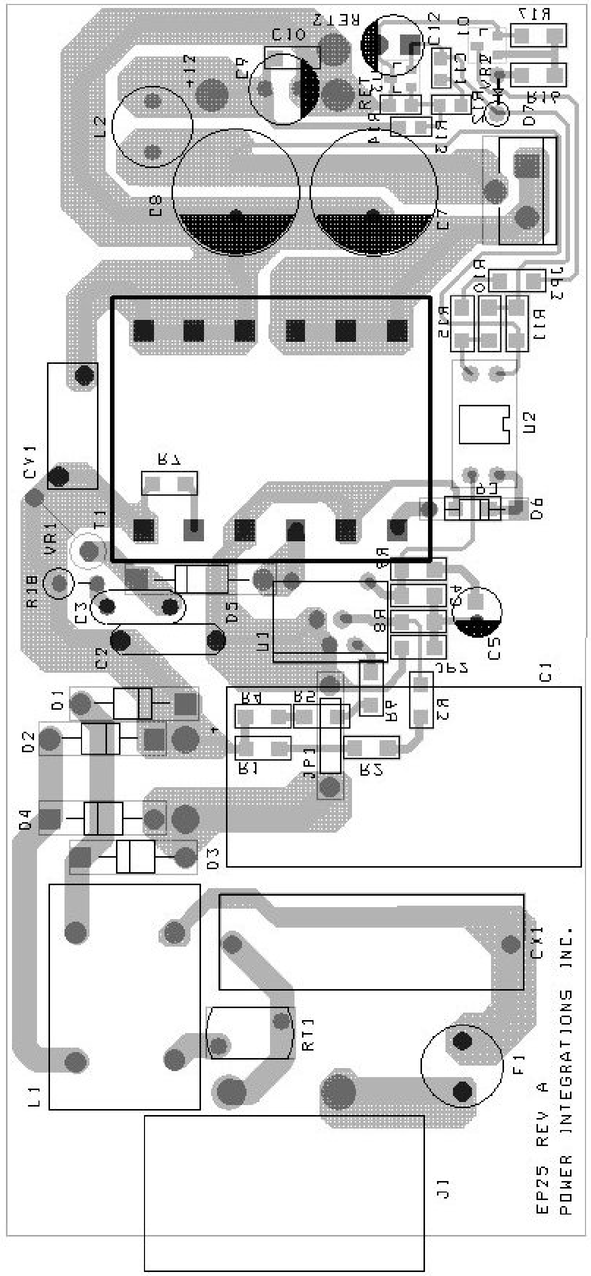

Figure 3 - EP-25 Printed Circuit Board Layout.

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6 Bill Of Materials

EP-25 - 45 W LCD Monitor Example
Bill Of Materials

Item	Qty	Reference	Description	P/N	Manufacturer
1	1	CX1	0.33 µF 250 V, X2	306 20224	Panasonic
2	1	C1	100 µF 400 V	400AXW100M16X35	Rubycon
3	1	C2	20 nF 1 kV, disc		
4	1	C3	4.7 nF 1 kV, disc		
5	2	C4, 10	100 nF 25 V, 1206		
6	1	C5	47 µF 10 V, 105C		
7	1	C6	1 µF 50 V, 105C		
8	1	CY1	2.2 nF Y1	440LD22	Cera-Mite
9	2	C7, 8	680 µF 35 V, low ESR	35ZL680M12.5X20	Rubycon
10	1	C9	220 µF 16 V, 105C		
11	1	C11	47 nF 25 V, 0805		
12	1	C12	22 µF 35 V, 105C		
13	4	D1-4	2 A 600 V	RL205	Rectron
14	1	D5	1 A 600 V, 75 ns	UF4005	General Instruments
15	1	D6	Diode, 75 V	1N4148	
16	1	D7	20 A 100 V, 50 ns	MBR20100	General Instruments
17	1	Q1*	XSTR, General Purpose SOT-23	MMST2222A	Diodes, Inc.
18	1	F1	Fuse, 250 VAC 3.15 A	372-1315	Wickman
19	1	L1	10 mH 1.4 A	B82732-R2142-A30	Epcos
20	1	L2	3.3 µH,	622-LY-3R3M	Toko
21	2	L3.4	Ferrite Bead	2643200101	Fair-Rite
22	2	L5, 6	Ferrite Bead	2643006302	Fair-Rite
23	3	R1-3	680 kΩ 5%, 1206		
24	3	R4-6	2.7 MΩ 5%, 1206		
25	2	R7, 15*	220 Ω 5%, 1206		
26	1	R8	15.0 kΩ 1%, 1206		
27	1	R9	6.8 Ω 5%, 1206		
28	1	R10	470 Ω 5%, 1206		
29	1	R11	1.0 kΩ 5%, 1206		
30	1	R12	4.7 kΩ 5%, 0805		
31	1	R13	38.3 kΩ 1%, 0805		
32	1	R14	10.0 kΩ 1%, 0805		
33	1	R16*	75 Ω 5%, 1206		
34	1	R17*	120 Ω 5%, 1206		
35	1	R18	68 Ω 5% 1/2 W		
36	1	T1	Transformer, Custom, EE30		
37	1	U1	TOP247Y		Power Integrations
38	1	U2	Optocoupler graded CTR	LTV817A	Liteon
39	1	U3	Shunt Regulator, SOT-23	LM431AIM3	National Semiconductor
40	1	VR1	TVS, 200 V	P6KE200	
41	1	VR2*	Zener, 14 V 5%	BXY79-C14V	Philips
42	1	RT1	Thermistor, 5 Ω	KC016L	Keystone

* Optional Components

7 Transformer Specification

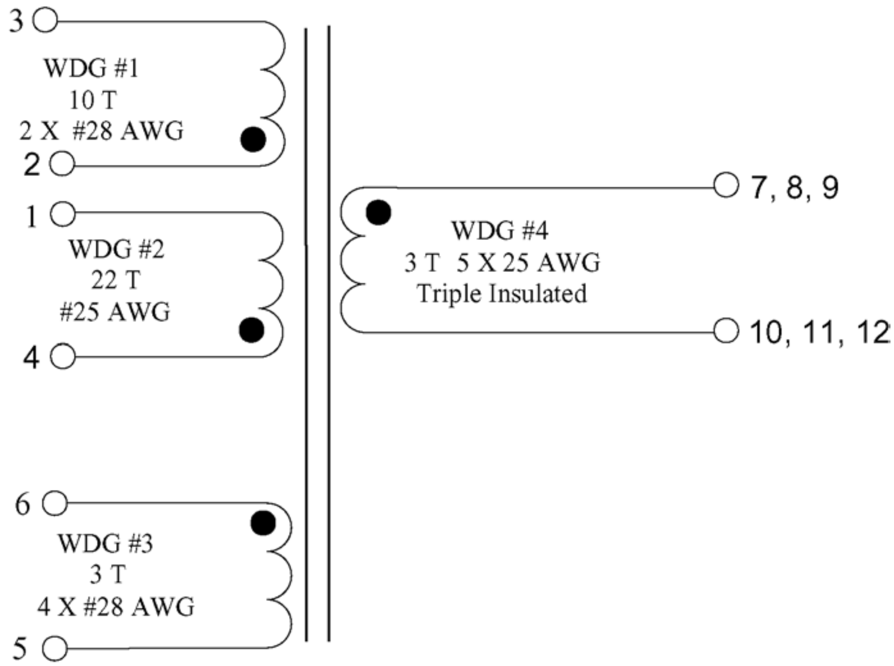

Figure 4 – T1, EP-25 Transformer.

7.1 Electrical Specifications

Electrical Strength	60 Hz, 1 min, from Pins 1-6 to Pins 7-12	3000 VAC
Creepage	Between Pins 1-6 and Pins 7-12	6 mm (Min.)
Primary Inductance	Pins 1-4, all other windings open, measured at 100 kHz	490 μH, ±10%
Resonant Frequency	Pins 1-4, all other windings open	2 MHz (Min.)
Primary Leakage Inductance	Pins 1-4, with Pins 7-12 shorted, measured at 100 kHz	6 μH (Max.)

7.2 Materials

Item	Description
[1]	Core: TDK PC40EE30-Z or equivalent, gapped for AL of 1045 nH/T^2
[2]	Bobbin: 12 pin EI30, Vertical Mount, Yih Hwa YW-016 or equivalent
[3]	Magnet Wire: #28 AWG Double Coated
[4]	Magnet Wire: #25 AWG Double Coated
[5]	Triple Insulated Wire: #25 AWG
[6]	Tape, 3M #44 or equivalent, 1.5 mm wide (min)
[7]	Tape, 3M #1298 or equivalent, 12 mm wide
[8]	Tape, 3M #1298 or equivalent, 13.5 mm wide
[9]	Tape. 3M #1298 or equivalent, 16.7 mm wide
[10]	Varnish

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7.3 Transformer Build Diagram

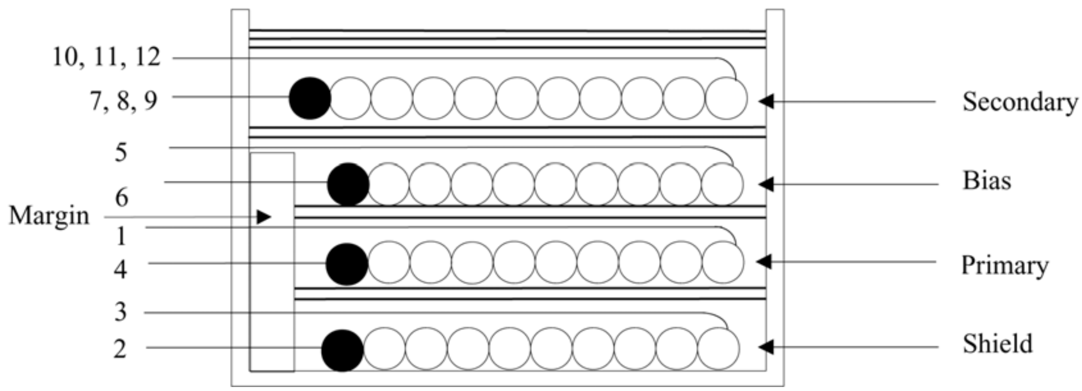

Figure 5 – T1, EP-25 Transformer Pins Side.

7.4 Transformer Construction

Primary Margin	Apply a 1.5 mm wide margin to pin side of bobbin using item [6]. Match height of cancellation, primary and bias windings.
Shield Winding	Starting at Pin 2, wind 10 bifilar tuns of item [3] in a single layer. Finish on Pin 3.
Basic Insulation	Use two layers of item [7] for basic insulation.
Primary	Start at Pin 4. Wind 22 turns of item [4] in approximately 1 layer. Finish on Pin 1.
Basic Insulation	Use two layers of item [7] for basic insulation.
Bifilar Bias winding	Starting at Pin 6, wind 3 bifilar turns of item [3]. Spread turns evenly across bobbin. Finish at Pin 5.
Basic Insulation	Use two layers of item [7] for basic insulation.
Pentafilar Secondary Winding	Start at Pins 7, 8, and 9. Wind 3 pentafilar turns of item [5] in a single layer. Spread turns evenly across bobbin. Finish on Pins 10, 11, and 12.
Outer Wrap	Wrap windings with 3 layers of tape (item [8]).
Core Preparation	Wrap bottom of one E core [1] with 2 layers of tape [9] as shown.
Final Assembly	Assemble and secure core halves so that the tape wrapped E core is at the bottom of the transformer. Clip Pin 3 to approximately 1/8", retaining winding termination. Varnish impregnate (item [10]).

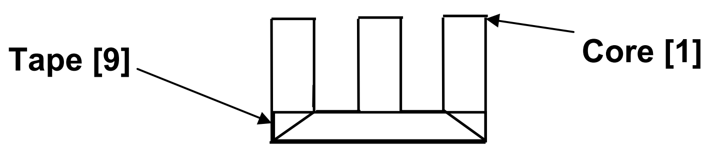

Figure 6 – T1, EP-25 Transformer Construction.

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8 Transformer Spreadsheet

ACDC_TOPGX_Rev1.2_052901 Copyright Power Integrations Inc. 2001	INPUT	INFO	OUTPUT	UNIT	TOP_GX_052901.xls: *TOPSwitch-GX* Continuous/Discontinuous Flyback Transformer Design Spreadsheet
ENTER APPLICATION VARIABLES					Customer
VACMIN	90			Volts	Minimum AC Input Voltage
VACMAX	265			Volts	Maximum AC Input Voltage
fL	50			Hertz	AC Mains Frequency
VO	12			Volts	Output Voltage
PO	45			Watts	Output Power
n	0.84				Efficiency Estimate
Z	0.5				Loss Allocation Factor
VB	12			Volts	Bias Voltage
tC	3			mSeconds	Bridge Rectifier Conduction Time Estimate
CIN	100			μFarads	Input Filter Capacitor
ENTER *TOPSWITCH-GX* VARIABLES					
TOPSwitch-GX	TOP247			Universal	115 V Doubled/230 V
Chosen Device		TOP247	Power Out	105 W	200 W
KI	0.5				External Ilimit reduction factor (KI = 1.0 for default ILIMIT, KI < 1.0 for lower ILIMIT)
ILIMITMIN			1.620	Amps	Use 1% resistor in setting external ILIMIT
ILIMITMAX			1.980	Amps	Use 1% resistor in setting external ILIMIT
Frequency - (F) = 132 kHz, (H) = 66 kHz	f				Full (F) frequency option – 132 kHz
fS	132000		1.32E+05	Hertz	*TOPSwitch-GX* Switching Frequency: Choose between 132 kHz and 66 kHz
fSmin			1.24E+05	Hertz	*TOPSwitch-GX* Minimum Switching Frequency
fSmax			1.40E+05	Hertz	*TOPSwitch-GX* Maximum Switching Frequency
VOR	90			Volts	Reflected Output Voltage
VDS	10			Volts	*TOPSwitch-GX* on-state Drain to Source Voltage
VD	0.5			Volts	Output Winding Diode Forward Voltage Drop
VDB	0.7			Volts	Bias Winding Diode Forward Voltage Drop
KP	0.50				Ripple to Peak Current Ratio (0.4 < KRP < 1.0 : 1.0< KDP < 6.0)
ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES					
Core Type	EI30				
Core		EI30		P/N:	PC40EI30-Z
Bobbin		EI30_BOBBIN		P/N:	BE-30-1112CP
AE			1.11	cm^2	Core Effective Cross Sectional Area
LE			5.8	cm	Core Effective Path Length
AL			4690	nH/T^2	Ungapped Core Effective Inductance
BW			13.7	mm	Bobbin Physical Winding Width
M	1			mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
L	1				Number of Primary Layers
NS	3				Number of Secondary Turns
DC INPUT VOLTAGE PARAMETERS					
VMIN			93	Volts	Minimum DC Input Voltage
VMAX			375	Volts	Maximum DC Input Voltage
CURRENT WAVEFORM SHAPE PARAMETERS					
DMAX			0.52		Maximum Duty Cycle
IAVG			0.57	Amps	Average Primary Current
IP			1.47	Amps	Peak Primary Current
IR			0.74	Amps	Primary Ripple Current
IRMS			0.81	Amps	Primary RMS Current

TRANSFORMER PRIMARY DESIGN PARAMETERS

LP	488	μHenrys	Primary Inductance
NP	22		Primary Winding Number of Turns
NB	3		Bias Winding Number of Turns
ALG	1045	nH/T^2	Gapped Core Effective Inductance
BM	2998	Gauss	Maximum Flux Density at PO, VMIN (BM < 3000)
BP	4027	Gauss	Peak Flux Density (BP < 4200)
BAC	750	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
ur	1950		Relative Permeability of Ungapped Core
LG	0.10	mm	Gap Length (Lg > 0.1 mm)
BWE	11.7	mm	Effective Bobbin Width
OD	0.54	mm	Maximum Primary Wire Diameter including insulation
INS	0.07	mm	Estimated Total Insulation Thickness (= 2*film thickness)
DIA	0.47	mm	Bare conductor diameter
AWG	25	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
CM	323	Cmils	Bare conductor effective area in circular mils
CMA	397	Cmils/Amp	Primary Winding Current Capacity (200 < CMA < 500)

TRANSFORMER SECONDARY DESIGN PARAMETERS (SINGLE OUTPUT / SINGLE OUTPUT EQUIVALENT)

Lumped parameters			
ISP	10.62	Amps	Peak Secondary Current
ISRMS	5.62	Amps	Secondary RMS Current
IO	3.75	Amps	Power Supply Output Current
IRIPPLE	4.19	Amps	Output Capacitor RMS Ripple Current
CMS	1124	Cmils	Secondary Bare Conductor minimum circular mils
AWGS	19	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
DIAS	0.91	mm	Secondary Minimum Bare Conductor Diameter
ODS	3.90	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
INSS	1.49	mm	Maximum Secondary Insulation Wall Thickness
VOLTAGE STRESS PARAMETERS			
VDRAIN	584	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
PIVS	64	Volts	Output Rectifier Maximum Peak Inverse Voltage
PIVB	65	Volts	Bias Rectifier Maximum Peak Inverse Voltage

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9 Performance Data

All measurements performed at room temperature, 60 Hz input frequency, unless otherwise specified.

9.1 Efficiency

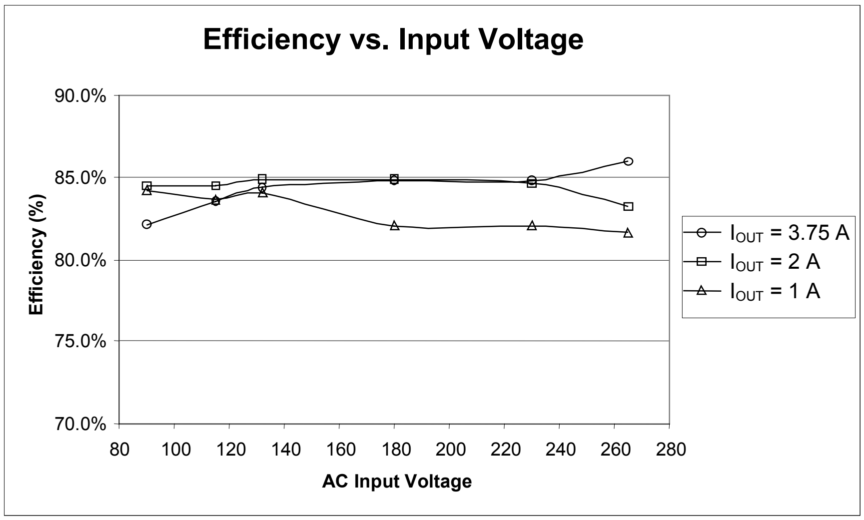

Figure 7 - Efficiency vs. Input Voltage, Full Load, Room Temperature, 60 Hz.

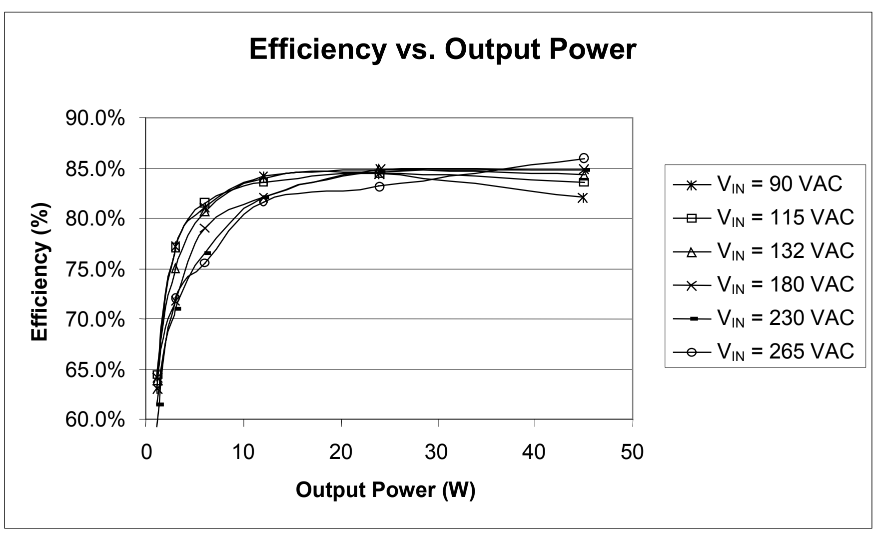

Figure 8 - Efficiency vs. Output Load, Room Temperature, 60 Hz.

9.2 No-load Input Power

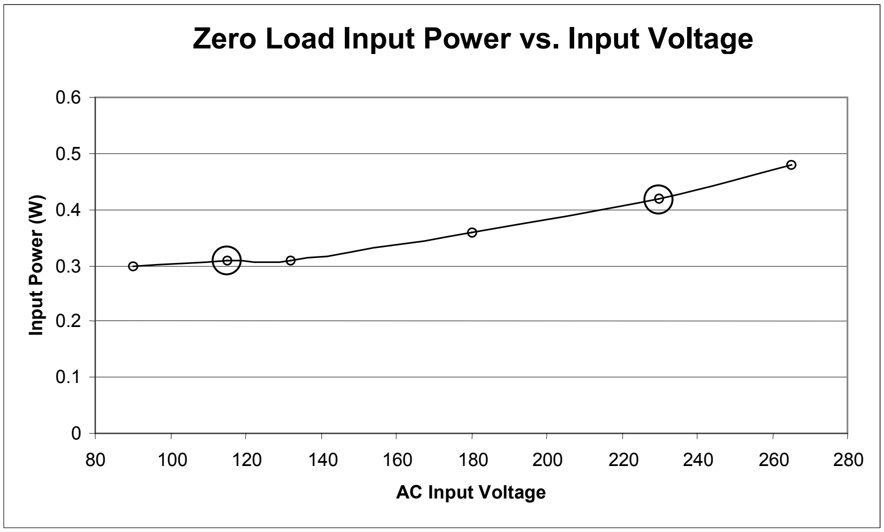

Figure 9 - Zero Load Input Power vs. Input Line Voltage, Room Temperature, 60 Hz.

9.3 Regulation

All regulation measurements were taken directly at the supply output terminals.

9.3.1 Load Regulation

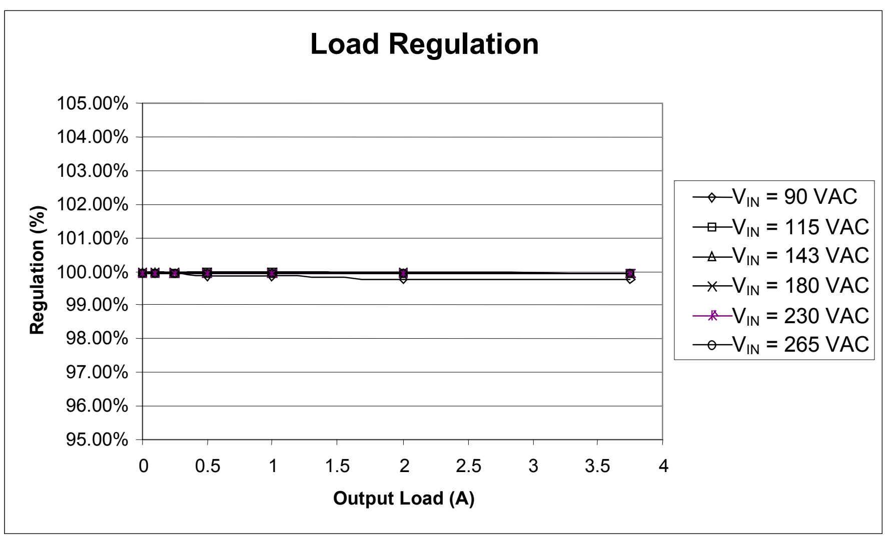

Figure 10 - Load Regulation, Room Temperature, 60Hz.

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9.3.2 Line Regulation

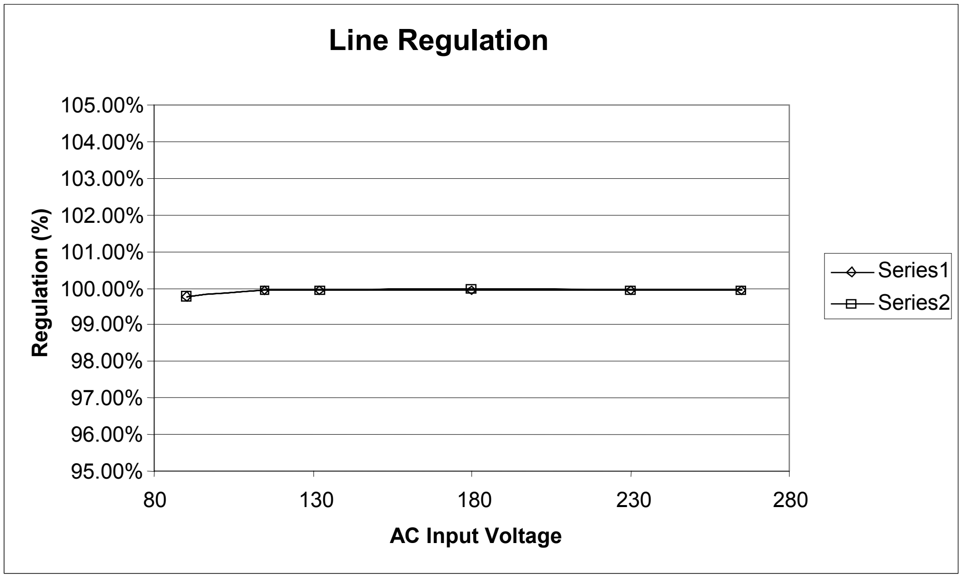

Figure 11 - Line Regulation, Room Temperature, 60 Hz.

10 Waveforms

10.1 Drain Voltage and Current, Normal Operation

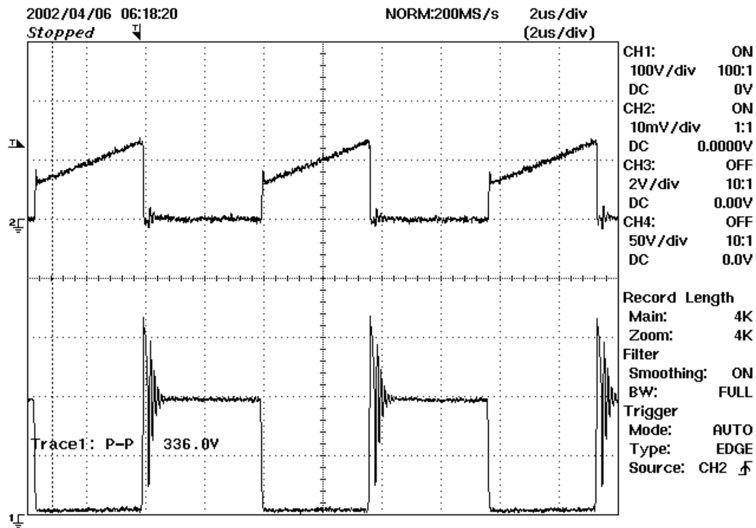

Figure 12 - 90 VAC, Full Load - Upper: I_{DRAIN}, 1 A/div, Lower: V_{DRAIN}, 100 V/div, 2 μs/div.

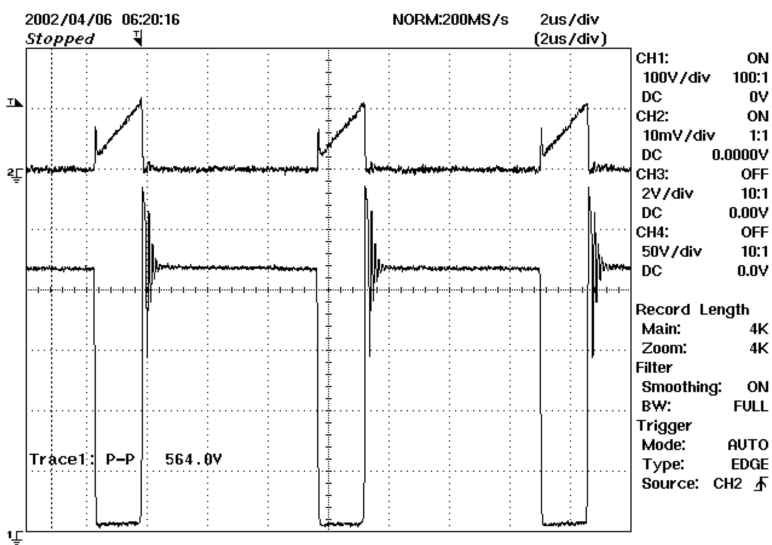

Figure 13 - 265 VAC, Full Load - Upper: I_{DRAIN}, 1 A/div, Lower: V_{DRAIN}, 100 V/div, 2 μs/div.

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10.2 Output Voltage Start-up Profile

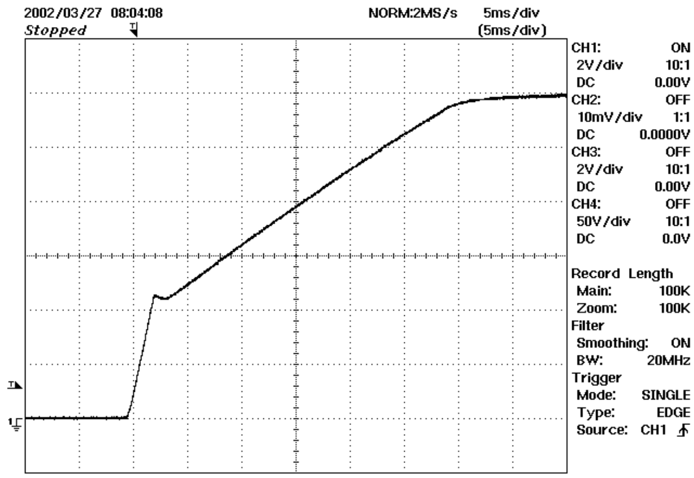

Figure 14 - Start-up Profile, 115 VAC, Full Resistive Load.

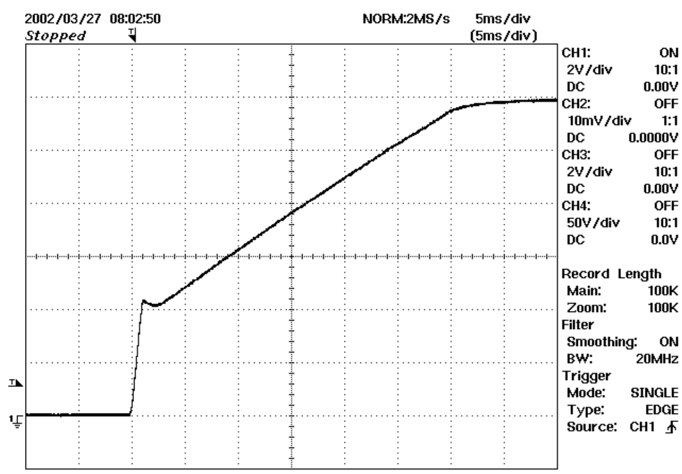

Figure 15 - Start-up Profile, 230 VAC, Full Resistive Load.

10.3 Load Transient Response (75% to 100% Load Step)

In the figures shown below, signal averaging was used to more clearly view the load transient response. The oscilloscope was triggered using the load current step as a trigger source. Since the output switching and line frequency occur essentially at random with respect to the load transient, contributions to the output ripple from these sources will average out, leaving only the contribution from the load step response.

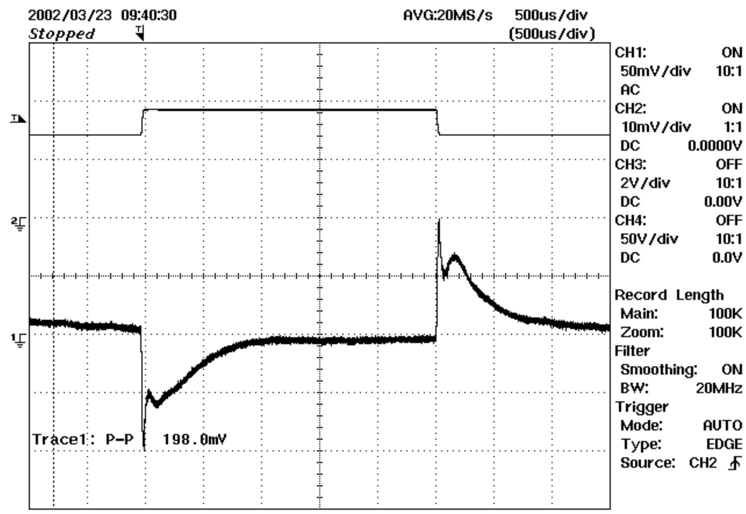

Figure 16 - Output Transient Response, 115 VAC. (75-100-75)% Load Step.
Upper: Output Current, 2 A/div. Bottom: Output Transient Response, 50 mV/div.
Time Base: 500 μs/div.

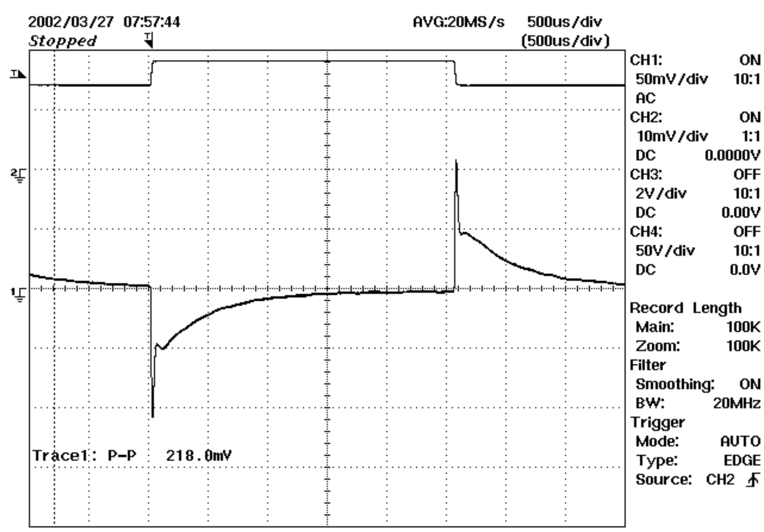

Figure 17 - Output Transient Response, 230 VAC, (75-100-75)% Load Step.
Upper: Output Current, 2 A/div. Bottom: Output Transient Response, 50 mV/div.
Time Base: 500 μs/div.

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10.4 Output Ripple Measurements

10.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pickup. Details of the probe modification are provided in Figure 18 and Figure 19.

The 5125BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 1.0 μF/50 V aluminum electrolytic. *The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).*

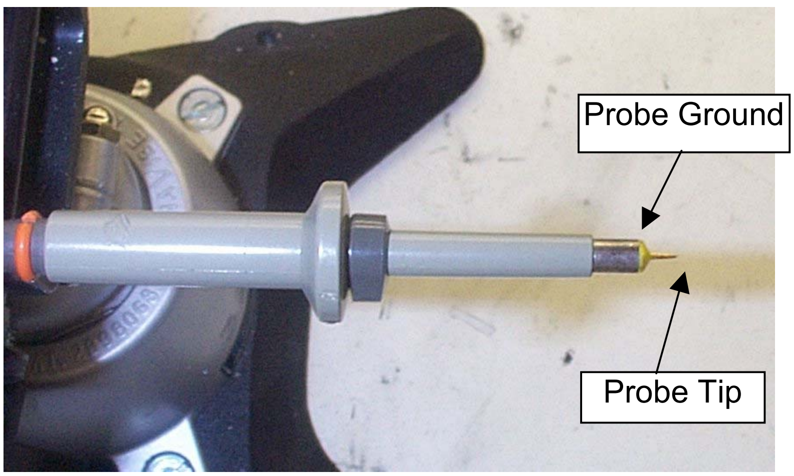

Figure 18 - Oscilloscope Probe Prepared for Ripple Measurement (End Cap and Ground Lead Removed).

Figure 19 - Oscilloscope Probe with Probe Master 5125BA BNC Adapter (Modified with wires for probe ground for ripple measurement, and two parallel decoupling capacitors added).

10.4.2 Measurement Results

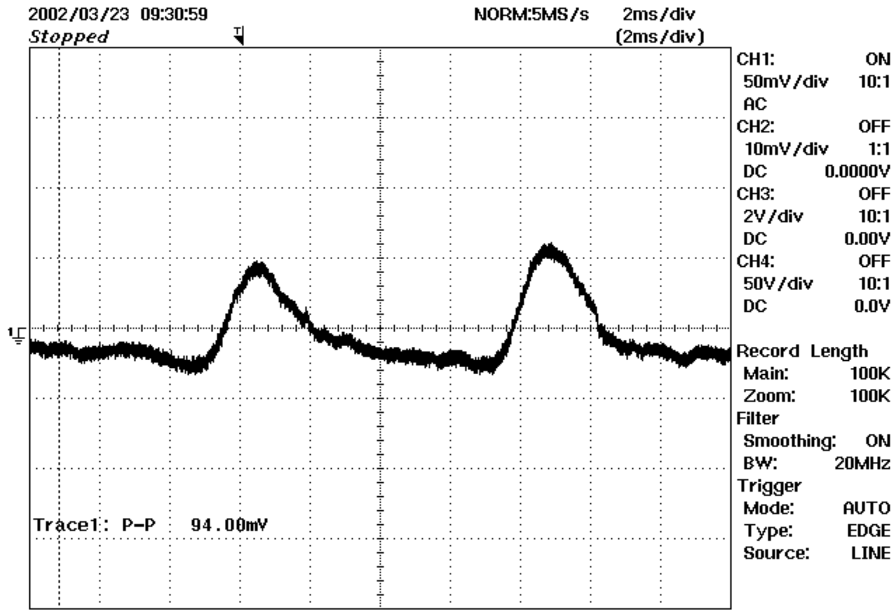

Figure 20 - Output Ripple, 90 VAC, 60 Hz, Full Load. 50 mV/div, 2 ms/div.

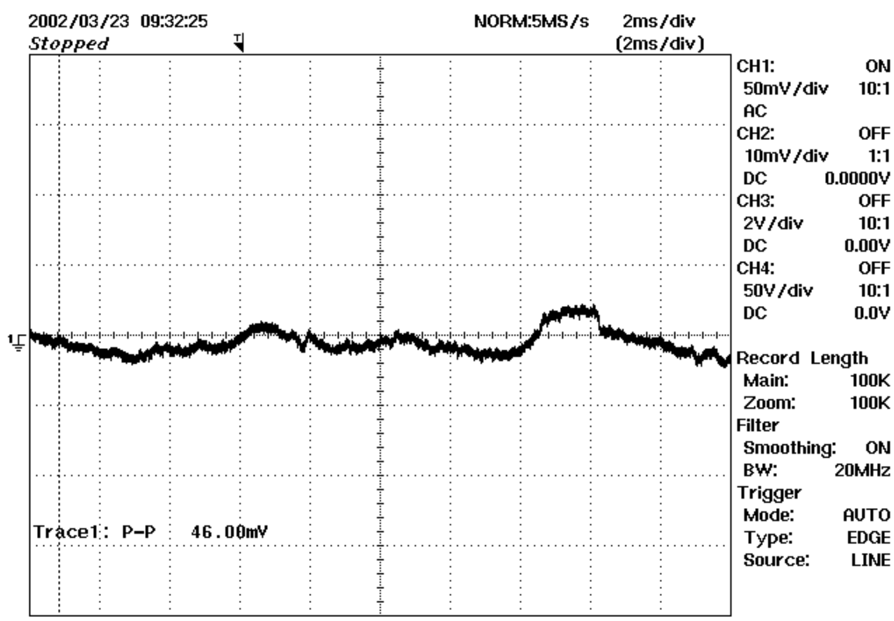

Figure 21 - Output Ripple, 115 VAC, Full Load, 60 Hz. 50 mV/div, 2 ms/div.

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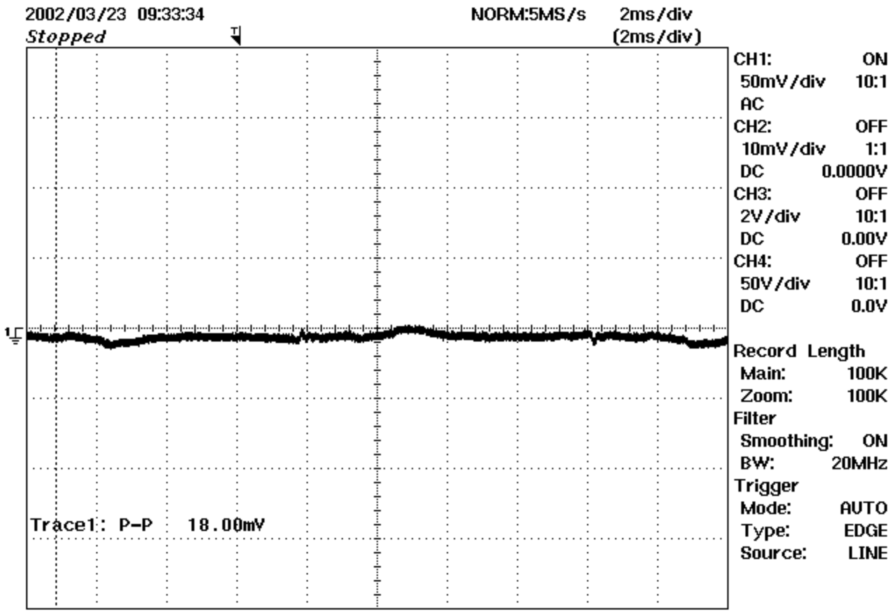

Figure 22 - Output Ripple, 230 VAC, Full Load, 60 Hz. 50 mV/div, 2 ms/div.

11 Control Loop Measurements

11.1 115 VAC Maximum Load

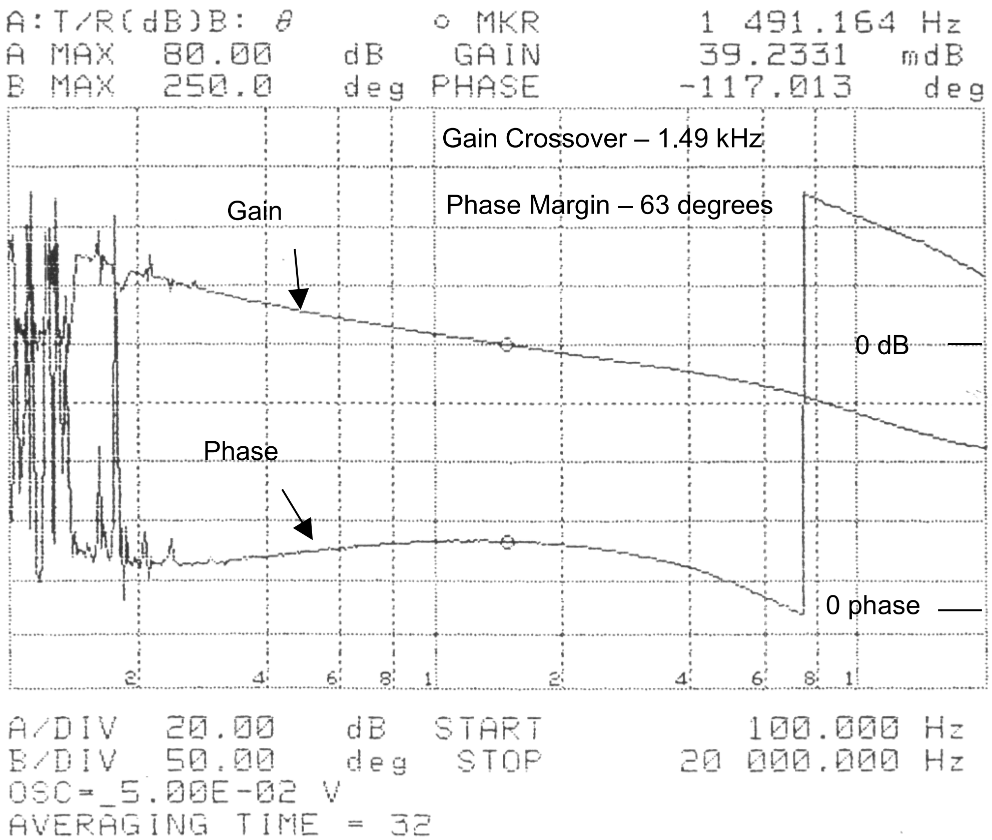

Figure 23 - Gain-Phase Plot, 115 VAC, Maximum Steady State Load, 0 dB Gain Crossover – 1.49 kHz, Phase Margin – 63 degrees.

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11.2 230 VAC Maximum Load

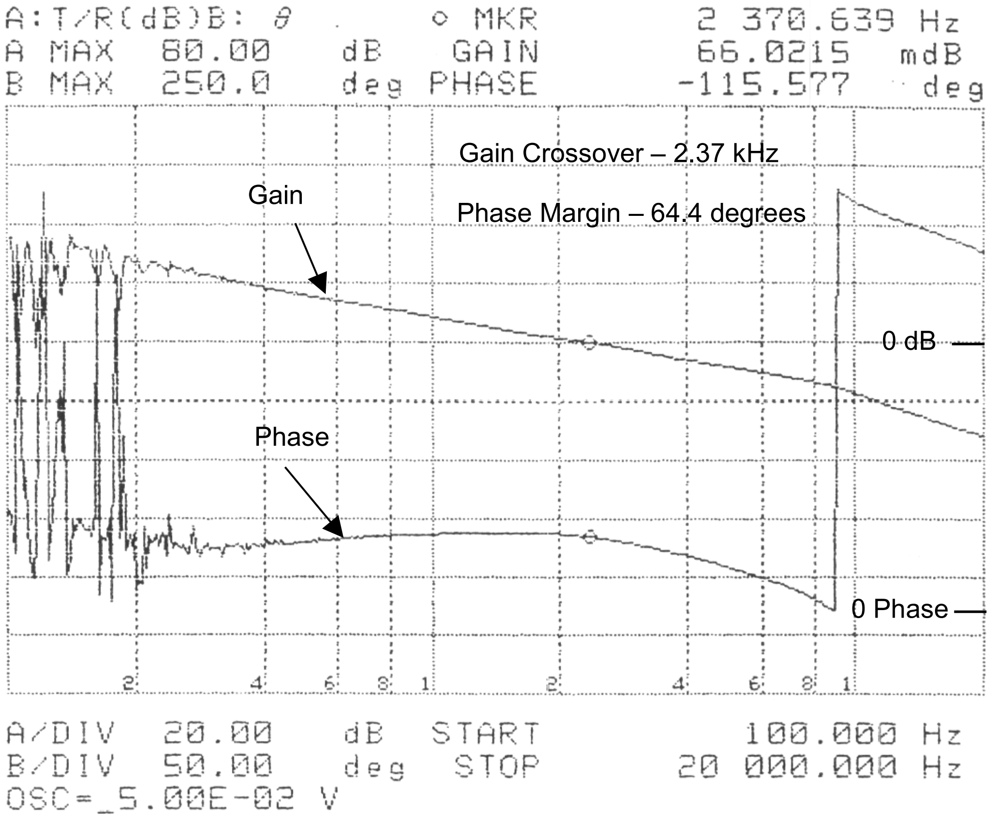

Figure 24 - Gain-Phase Plot, 230 VAC, Maximum Steady State Load, 0 dB Gain Crossover – 2.37 kHz, Phase Margin – 64.4 Degrees

12 Conducted EMI

All conducted EMI measurements were taken with a 6' cable at the output of the supply, terminated in a resistive load, The return wire at the end of the cable was connected to the LISN ground. A 6' 3-wire cord was used at the supply AC input.

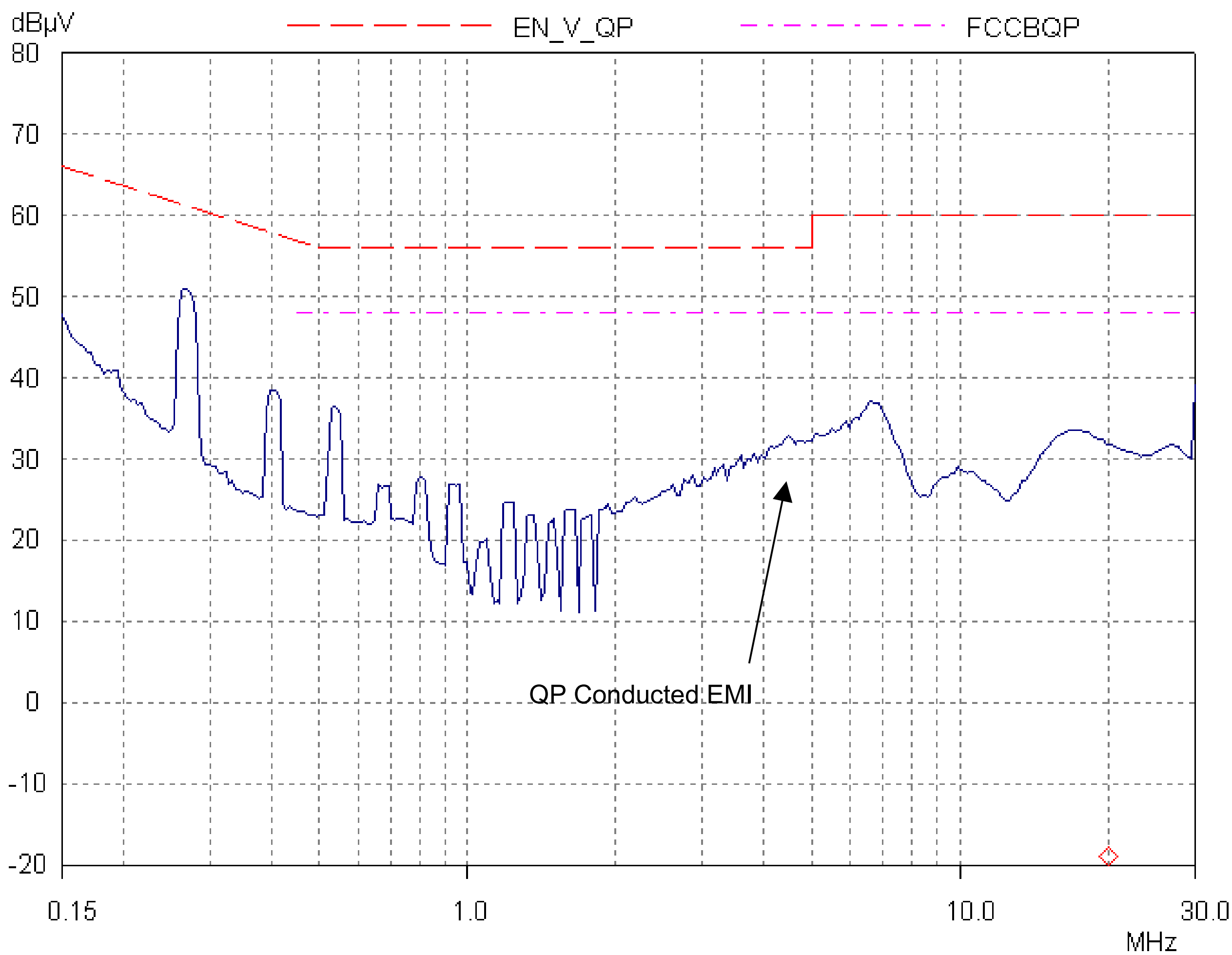

Figure 25 - Conducted EMI, Maximum Load, 115 VAC, 60 Hz, EN55022 B and FCC B Quasi-Peak Limits.

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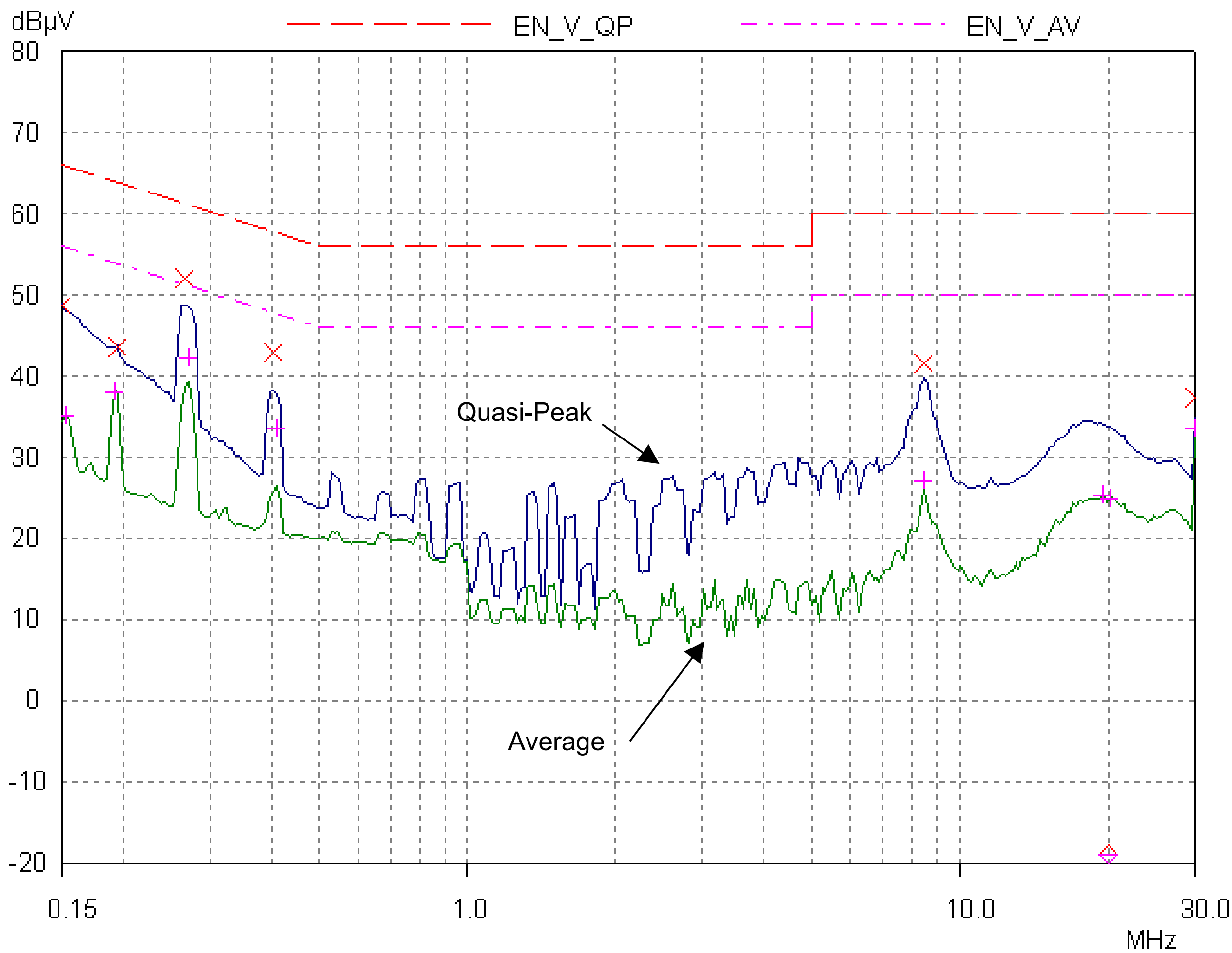

Figure 26 - Conducted EMI, Maximum Load, 230 VAC, 60 Hz, EN55022 B Limits.

13 Revision History

Date	Author	Revision	Description & changes
01-MAY-02	RH	1.0	Release

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Notes

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