Design Idea DI-31

DPA-Switch™ 5 V, 70 W DC-DC Converter with Synchronous Rectification

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
DC-DC Converter	DPA426R	70 W	36-75 VDC	5 V	Forward

Design Highlights

- Extremely low component count
- High efficiency, 90% using synchronous rectification
- No current sense resistor or current transformer required
- Output overload, open loop and thermal protection
- Accurate input under/overvoltage meets ETSI standards
- 300 kHz switching frequency – optimizes efficiency using simple self-driven synchronous rectification

Operation

The 70 W converter shown in Figure 1 benefits from many of the *DPA-Switch* integrated features. In particular, no external current sense components are required. In a discrete implementation, an expensive current transformer and a number of additional components would increase the cost of this converter significantly.

R1 programs the input UV/OV thresholds. The tight tolerance of the UV/OV thresholds limits the range of gate drive voltages applied to MOSFETs Q1 to Q6, eliminating the need for gate voltage clamp circuitry. The self-driven synchronous rectification configuration is therefore very simple, with R4 to R6 filtering voltage spikes at the gates of Q1, Q2 and Q3 and D4 preventing the body diodes of Q4, Q5 and Q6 from conducting.

Capacitor C9, diodes D1-D2, and inductor L2 form a resonant snubber that recycles leakage and magnetizing energy stored in T1, and also helps to reset T1. Zener diode VR1 provides a hard voltage limit and only conducts during output transient and overload conditions. Capacitor C12 and Resistor R7 damp secondary switching spikes and help to reset T1.

Key Design Points

- For nominal undervoltage set point V_{UV}: R1 = (V_{UV} - 2.35 V)/50 µA. V_{OV} = (R1 x 135 µA) + 2.5 V.
- Locate C10, C11, and R3 close to the U1 CONTROL pin, with ground connections returned to SOURCE pin.

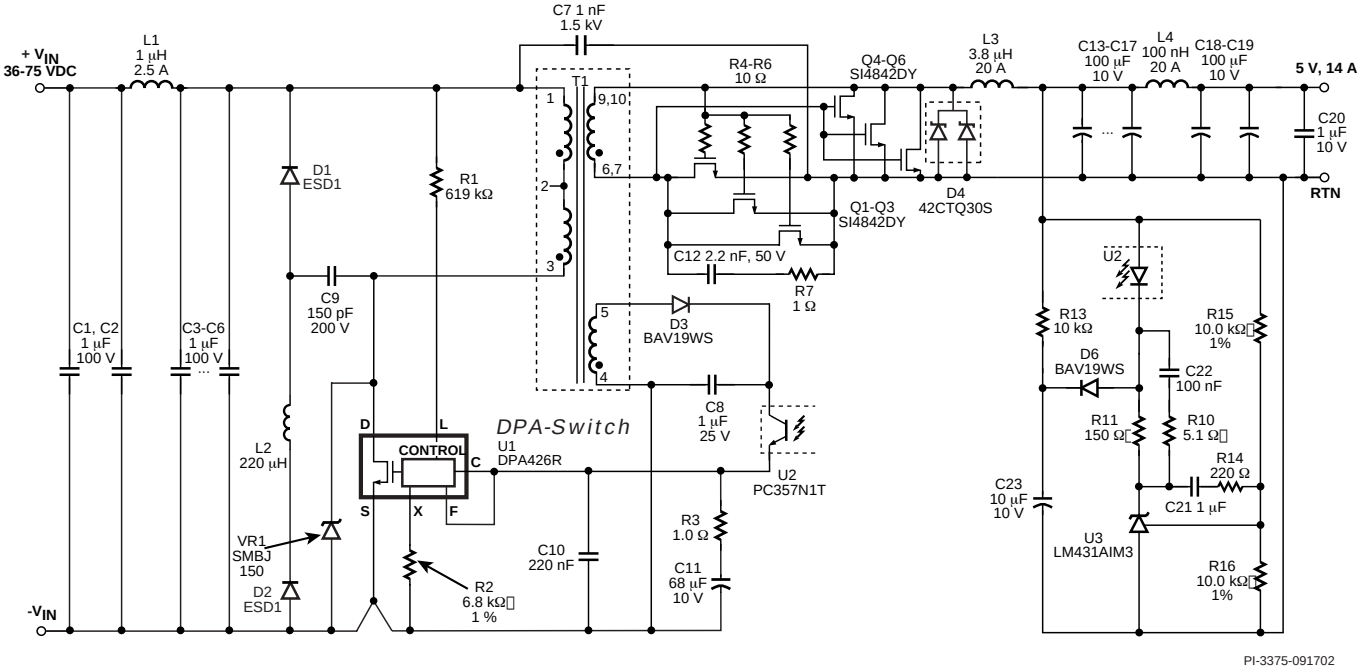

Figure 1. DPA426 70 W, 5 V, 14 A DC-DC Converter.

- Minimize primary and secondary high current loop areas to reduce parasitic inductance.
- Optocoupler U2 should have a controlled CTR range of 100 to 200% for optimum loop stability.
- Size transformer reset components to ensure transformer reset at minimum operating voltage without exceeding 170 V drain voltage at high line. It may be necessary to gap T1 to offset effect of Q4-Q6 gate capacitance.
- Set Zener VR1 clamp voltage to 150 V to both safely limit the DRAIN below BV_{DSS} and guarantee transformer reset.
- Select number of bias turns to provide 12 V to 14 V at minimum input voltage and full load.
- Main primary power return should be connected to the *DPA-Switch* tab, not to the SOURCE pin.
- Scale time constant of C9 and L2 to allow C9 to reset completely during minimum on-time conditions.
- Consult AN-31 for additional design tips and information.

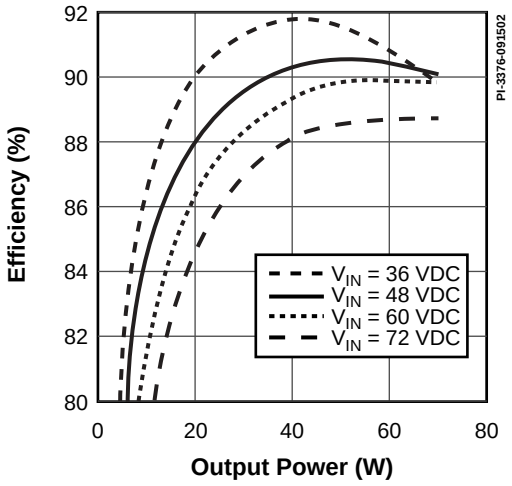

Figure 2. Efficiency vs. Output Power.

TRANSFORMER PARAMETERS	
Core Material	EFD25, 3F3 Gap for A_{LG} = 1100 nH/T^2
Bobbin	EFD25 10 pin (B&B B-025 or equivalent)
Winding Details	Bias: 5T, 30 AWG Primary: 6T+ 5T, 4 x 26 AWG Secondary: 3T, 0.005" Cu foil
Winding Order (Pin Numbers)	Primary (3-2), tape, Bias (4-5), tape, Secondary (6,7-9,10), tape, Primary (2-1), tape
Inductance	Primary: 130 µH ±10%, Leakge: 10 µH (max)
Primary Resonant Frequency	3 MHz (minimum)

Table 1. Transformer Design Parameters.

OUTPUT INDUCTOR PARAMETERS	
Core	EE22, TDK PC40 Material Gap for A_{LG} of 250 nH/T^2
Bobbin	TDK BE-22-5116
Winding Details	4T, 0.016" Cu foil
Inductance	4 µH ± 10%

Table 2. Output Inductor Construction Information.

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