# Design Idea DI-29
# *DPA-Switch*™
# 25 W Flyback DC-DC Converter

| Application | Device | Power Output | Input Voltage | Output Voltage | Topology |
|---|---|---|---|---|---|
| DC-DC Converter | DPA425R | 25 W | 36 - 75 VDC | 7 V | Flyback |

## Design Highlights

- Extremely low component count
- High efficiency – 85% using Schottky rectifiers
- No current sense resistor or transformer required
- Accurate input under/over voltage meets ETSI standards
- Operates to zero load with no pre-load required
- Output overload, open loop and thermally protected
- 400 kHz operation minimizes size of magnetics

## Operation

*DPA-Switch* greatly simplifies the design compared to a discrete implementation. Resistor R1 programs the input under/over voltages to 33 V and 86 V, respectively. These thresholds have tolerances that guarantee the converter is operational at 36 V, without the cost of additional line sense components.

Resistor R3 programs the internal current limit of the DPA425R to 50% of nominal. The larger *DPA-Switch* selection reduces conduction losses, raising efficiency without circuit changes or increased overload power.

Zener VR1 clamps leakage inductance spikes, keeping the DRAIN voltage below $BV_{DSS}$. The bias supply for U1 is provided from an auxiliary flyback transformer winding.

On the secondary, a snubber across D2 (C9, R5 and R13) limits the secondary leakage inductance spikes generated by diode reverse recovery. Inductor L2, C13 and C14 form a post-filter to reduce high frequency output switching ripple. A soft-finish network, C18, D3 and R7, eliminates output turn-on overshoot. The remaining components provide output voltage regulation and loop compensation.

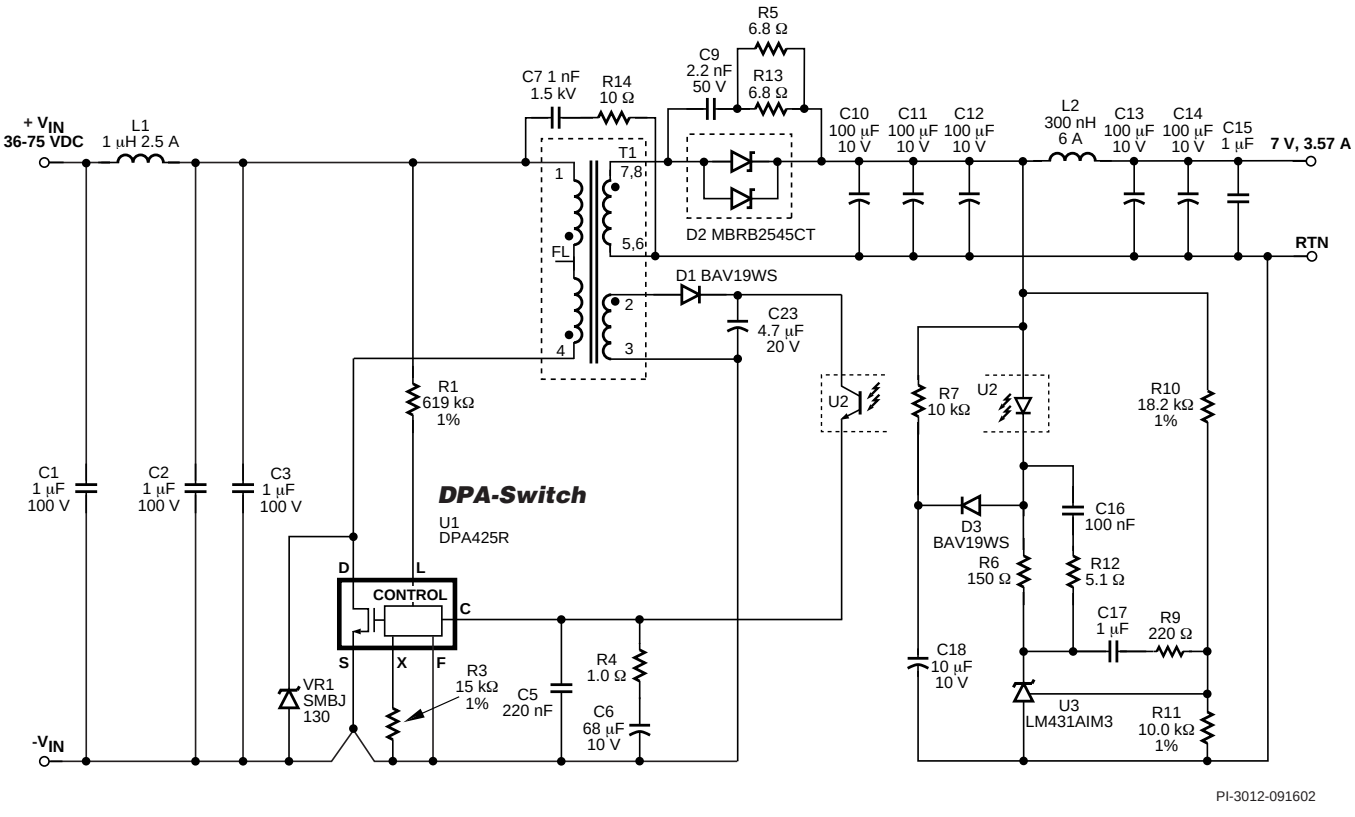


*Figure 1. DPA-Switch Flyback DC-DC Converter Schematic.*

## Key Design Points

- For nominal under-voltage set point $V_{UV}$: R1 = ($V_{UV}$-2.35 V)/50µA. $V_{OV}$ = (R1×135 µA)+2.5 V.
- Zener VR1 voltage is 130 V to safely limit the DRAIN voltage below $V_{DSS}$ of 200 V.
- Opto U2 should have a CTR of between 100% and 200% for optimum loop stability.
- Set resonance of L2 and C13 + C14 to beyond loop crossover frequency (typically 5% to 10% of switching frequency).
- Good layout practices should be followed:
  - Locate C5, C6 and R4 close to U1, with grounds returned to the SOURCE pin.
  - Primary return should be connected to the *DPA-Switch* tab, not the SOURCE pin.
  - Minimize the primary and secondary loop areas to reduce parasitic leakage inductance.

| Transformer Parameters | |
|---|---|
| Core Material | PR1408<br>Siemens N87<br>Gap for 340 nH/T$^2$ |
| Bobbin | P1408 8 pin (B&B B-096 or equivalent) |
| Winding Details | Primary: 6T + 6T, 2 x 27 AWG<br>Secondary: 3T, 4 x 25 AWG<br>Bias: 6T, 32 AWG |
| Winding Order (pin numbers) | Primary (4-FL), tape, Bias (2-3), tape,<br>Secondary (5,6-7,8), tape,<br>Primary (FL-1), tape |
| Inductance | Primary: 49 µH ±10%, Leakage: 1 µH (max) |
| Primary Resonant Frequency | 3.8 MHz (minimum) |

*Table 1. Transformer Construction Information.*

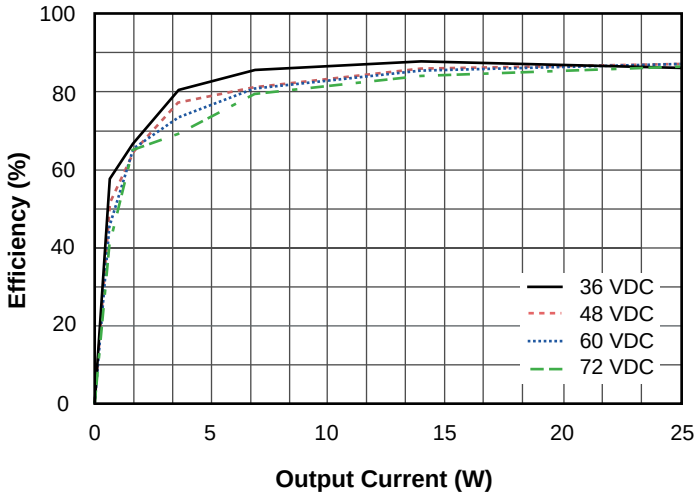


*Figure 2. Efficiency vs. Output Power.*

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