Design Idea DI-14

TinySwitch-II® 10 W PC Standby: Meets 1 W Standby Executive Order

Application	Device	Power Output	Input Voltage	Output Voltage	Topology
PC Standby	TNY266P	10 W	140-375 VDC	5 V / 15 V	Flyback

Design Highlights

- Low cost, low component count solution for PC Standby
- >700 mW output with <1 W input
- 132 kHz operation allows small, low cost EE19 core
- ON/OFF digital regulation - no loop compensation needed
- ±5% output tolerance with simple Zener reference

Operation

The *TinySwitch-II* PC standby supply in Figure 1 delivers 10 W output power. Two outputs are generated: 5 V for the processor and peripherals, and a primary side 15 V for the main power supply switcher. The design shown in Figure 1 takes advantage of many of the built-in features of TNY266P.

The combined voltage drops of Zener diode (VR2) and optocoupler diode (U2) set the output voltage. R3 biases VR2 according to its specification. The *TinySwitch-II* feedback current is independent of load allowing ±5% output voltage tolerance with this simple Zener reference.

Due to the digital nature of the *TinySwitch-II* control scheme, no loop compensation is required. In addition, the current transfer ratio (CTR) of the optocoupler is not critical and no DC gain setting resistor in series with VR2 is required.

The 15 V primary winding is used to provide a low voltage supply for the BYPASS pin. This optimizes efficiency by disabling the internal high voltage current source that normally powers the IC from the DRAIN. R2 is chosen to provide >500 μA under standby conditions, exceeding the maximum IC current consumption. An internal Zener clamps the BYPASS pin to the required voltage.

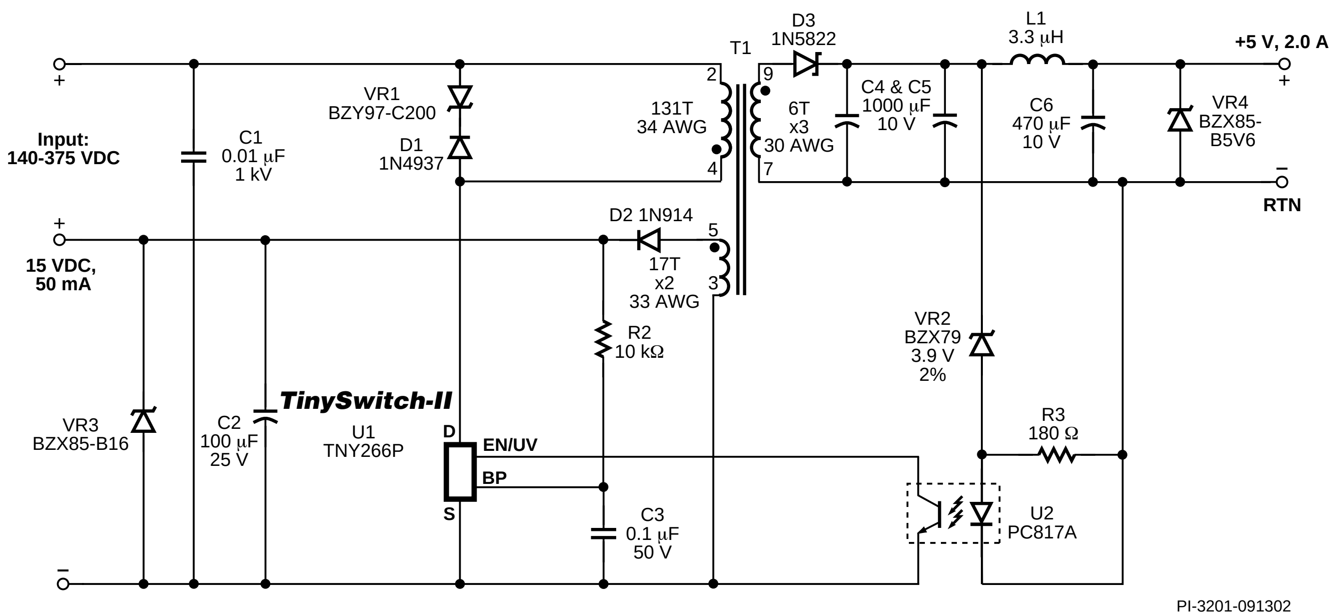

Figure 1. TinySwitch-II 10 W PC Standby.

Key Design Points

- To optimize efficiency:
  - Use continuous mode transformer design to reduce primary and secondary rms currents.
  - Use low reflected voltage to reduce primary turns and minimize leakage inductance using complete winding layers fully utilizing bobbin width.
  - Place tape between primary layers to reduce capacitance and therefore switching losses.
- Minimize secondary circuit bias currents. Use a low current feedback Zener for best tolerance.
- Standby power is reduced further with a TL431 secondary reference which requires less bias current.
- Optional UV detect resistor (2 MΩ for 100 VDC threshold) from input DC rail to EN/UV pin prevents turn-off glitches if necessary.
- Layout – minimize high current loops on primary and secondary to reduce ripple and noise on outputs.
- Optimum cross regulation on 5 V and 15 V windings is achieved by winding in full even layers using parallel wires if necessary. An RCD clamp also improves cross regulation though increases losses - use >200 kΩ resistor to limit dissipation.
- C1 provides local decoupling if main capacitors are located away from standby supply input.

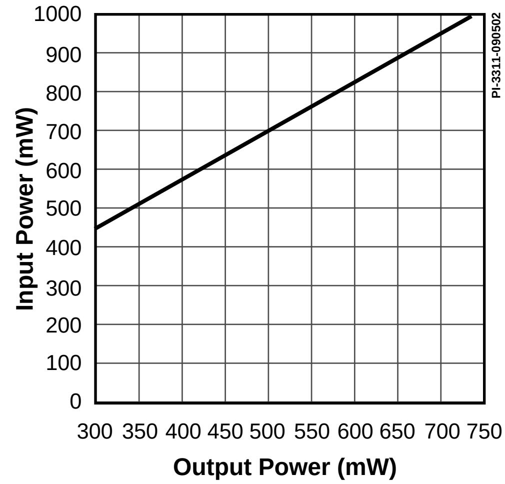

Figure 2. Standby Power Consumption vs. Output Power measured at 325 VDC.

TRANSFORMER PARAMETERS	
Core Material	EE19 TDK PC40, or equivalent A_L of 131 nH/T[2]
Bobbin	EE19, 10 pin
Winding Order (pin numbers)	Primary (2-4), tape, Secondary (7-9), 5 V, tape, bias (3-5) tape
Primary Inductance	2.25 mH ±10%
Primary Resonant Frequency	500 kHz (minimum)
Leakage Inductance	50 µH (maximum)

Table 1. Transformer Construction Information.

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