# Design Idea DI-10 **TOPSwitch<sup>®</sup>FX** PC Standby



Application	Device	Power Output	Input Voltage	Output Voltage	Topology
PC Standby	TOP232Y	17 W	200 - 375 VDC	3.3 V / 5 V	Flyback

## **Design Highlights**

- Exceeds Blue Angel efficiency requirements, achieving 78% at 3.9 W output (5 W input)
- Soft-start capability reduces start-up component stresses
- 132 kHz operation allow small, low cost EE19 transformer to deliver 17 W and prevents audio interaction with main converter
- Under-voltage detect eliminates turn-on/off glitches
- Dual sensing ensures 5% accuracy on 3.3 V and 5 V outputs
- 15 V bias supply for primary side circuitry

# Operation

The *TOPSwitch-FX* PC Standby supply provides 17 W of output power. Three outputs are generated, 3.3 V and 5 V for the processor and peripherals, and 15 V for the main power supply switcher.

The design utilizes the TOP232 and takes advantage of many of the device's built in features. Soft-start is one of these, requiring no external components. During the first 10 ms of operation, the duty cycle is raised from 0 to 78%, lowering current and voltage stresses on the internal power MOSFET, clamp circuits and output rectifier.

Line under-voltage is implemented using a single 3.9 M $\Omega$  resistor (R1) to eliminate glitches during turn-on/off. This value was chosen to set V<sub>UV</sub> at 195 VDC. This is just below the lowest operating DC input voltage for a doubler input configuration.

The input bypass capacitor C1 is needed only if the main supply filter is located remotely. Diode D1 and Zener VR1 are used to clamp the leading edge voltage spikes caused by transformer leakage inductance, to a safe value. The bias winding is rectified and filtered by D2 and C6 to create a bias voltage for the TOP232. This 15 V primary referenced voltage may also be used to power the main converter control circuitry. Shunt regulator U3 along with R6, R7, R9, R10 & R11 are used to sense and regulate the two output voltages.

# **Key Design Points**

- The value of the under-voltage detection is set according to the equation  $V_{\mu\nu} = 50 \ \mu A \ X \ R1$ .
- Suitable layout and filtering (L1, L2, C11, C13) results



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## **DI-10**

in low output ripple on 3.3 V and 5 V channels. At full load, peak-to-peak ripple is significantly below 50 mV.

- Y1 capacitor (CY1) is tied between secondary return and primary positive DC rail to minimize potential noise coupling to SOURCE pin during AC common mode surge events.
- Good cross regulation on the main channels is maximized with dual sense feedback to the 3.3 V and 5 V outputs (R9, R10).
- Capacitor (C8) is added to eliminate output start-up overshoot on DC output channels.
- Feedback compensation is accomplished with capacitor C7, across TL431 reference amplifier (U3), and correct choice of CONTROL pin capacitor and series resistor (C5, R5). Resistor R6 sets feedback gain while resistor R7 provides bias to the TL431 when the 5 V output is lightly loaded. Compensation is optimized for the transformer design and the power supply provides satisfactory phase margin and operating bandwidth across wide operating conditions.



Figure 2. DC output ripple seen on +3.3 V output, full load

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Transformer Parameters					
Core Material	EE 19 Nippon Ceramic NC-2H A <sub>L</sub> of 116 nH/T <sup>2</sup>				
Bobbin	EE19 8 pin (TDK BE-19-118CPH or equivalent)				
Winding Order (pin numbers)	Primary (1-2), Tape, 3.3 V (6-7/8), 5 V (7/8-5), Tape, Bias (3-4), Tape				
Primary Inductance	2.4 mH ±10%				
Primary Resonant Frequency	1 MHz (minimum)				
Leakage Inductance	75 μΗ				

Table 1. Transformer construction information



Figure 3. Transformer build diagram

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