or Prototyping the PCM16C010 and PCM16C011 a Single **Function PC Card Interface**

Using the PCM16C02 as a **Single Function PC Card** Interface or Prototyping the PCM16C010 and PCM16C011

National Semiconductor Application Note 1051 August 1996



OVERVIEW

The PCM16C02 Configurable Multiple Function PC Card Interface Chip can also be used as a PC Card 95 standard compliant interface between the PC Card host bus and a single card function. The PCM16C02 will operate with a single memory or I/O function allowing host system software or a generic enabler to configure the card. Either function interface of the PCM16C02 can be used as long as the unused function's configuration is properly disabled. Unused inputs and registers including the configuration profile in the Card Information Structure (CIS) must be addressed.

USING FUNCTION 0 ONLY

Connecting the single card function to the function 0 interface of the PCM16C02 will enable the use of the NAND Flash (NM29N16) interface if desired. See the PCM16C02 data sheet for details on configuring function 0 for this use. The disabling of function 1 described here will be effective regardless of the mode used for function 0. The use of function 0 only can be used as a prototype for the National Semiconductor PCM16C010 Single Function PC Card interface. The pin conditions used for disabling function 1 of the PCM16C02 are identical to the pinout, conditions, and device footprint used on the PCM16C010.

Table I lists the pin conditions necessary to insure that function 1 does not interfere with the desired operation of functon 0 as the single PC Card function. The values assigned to the unused input pins are chosen based on the default values of their associated configuration registers. The unused outputs should be left disconnected.

The PCM16C02 specific configuration register default values are loaded upon power up along with the CIS from the EEPROM used in the card design. The Pin Polarity Register at 0x03E4 must contain a value of zero for bit D1. The other registers which include configuration information for function 1 are the PMGR and Clock (0x03E6) and the CTERM 1 (0x03EA) registers. These registers should contain values of zero for the bits associated with function 1.

In addition, the PC Card standard configuration registers for function 1 must not be changed from their default value of zero. The function 1 PC Card registers are located at attribute memory locations 0x1040 through 0x1052. These registers include the Function 1 Configuration Option, Configuration Status, Pin Replacement, I/O Event, Base A, Base B, and Limit Registers. These registers could only be changed by system or client software writing to these locations. It is necessary to insure that your client driver does not access these locations. System software will not access these locations if the base address of the function 1 registers is not provided to the software in the CIS. The CISTPL CONFIG tuple of the CIS must provide the base address 0x1020 of the configuration registers for function 0 only.

TABLE I. Pin Values to Disable Function 1

Pin Name	Pin No.	Туре	Connection
RIIN(1)#	87	I	V _{CC}
MCLK(1)	90	I	GND
IOCS16(1)#	91	I	V _{CC}
READY(1)	92	1	No Connect
CINT(1)	94	1	GND
CWAIT(1)	96	1	GND
PCNTL(1)	15	0	No Connect
CS(1)#	95	0	No Connect
SRESET(1)	93	0	No Connect
FCLK(1)	89	0	No Connect

USING FUNCTION 1 ONLY

Connecting the single card function to the function 1 interface of the PCM16C02 will enable the use of the DMA mode which supports the DMA extension to the PC Card Standard if desired. For information on the DMA mode for function 1, see the Application Note number 998 for the Functional Description and Specifications of the PCM16C02 PC Card interface Device in Rev 3 DMA Mode. The disabling of function 0 described here will be effective regardless of the mode used for function 1. The use of function 1 only can be used as a prototype for the National Semiconductor PCM16C011 Single Function PC Card interface. The pin conditions used for disabling function 0 of the PCM16C02 are identical to the pinout, conditions, and device footprint used on the PCM16C011.

Table II lists the pin conditions necessary to ensure that function 0 does not interfere with the desired operation of function 1 as the single PC Card function. The values assigned to these unused pins are chosen based on the default values of their associated configuration registers. The unused outputs should be left disconnected.

The PCM16C02 specific configuration register default values are loaded upon power up along with the CIS from the EEPROM used in the card design. Note that the EEPROM clock is derived from FCLK(0) so that a clock must still be connected to function 0. The Pin Polarity Register at 0x03E4 must contain a value of zero for bit D0. The other registers which include configuration information for function 0 are the PMGR and Clock (0x03E6) and the CTERM 0 (0x03E8) registers. These registers should contain values of zero for the bits associated with function 0.

In addition, the PC Card standard configuration registers for function 0 must not be changed from their default value of zero. The function 0 PC Card registers are located at attribute memory locations 0x1020 through 0x1032. These registers include the Function 0 Configuration Option, Configuration Status, Pin Replacement, I/O Event, Base A. Base B. and Limit Registers. These registers could only be changed by system or client software writing to these locations. It is necessary to ensure that your client driver does not access these locations. System software will not access these locations if the base address of the function 0 registers is not provided to the software in the CIS. The CISTPL_CONFIG tuple of the CIS must provide the base address 0x1040 of the configuration registers for function 1 only.

TABLE II. Pin Values to Disable Function 0

Pin Name	Pin No.	Туре	Connection
RIIN(0)#	23	I	V _{CC}
MCLK(0)	24	I	GND
IOCS16(0)#	26	I	V _{CC}
READY(0)	27	I	No Connect
CINT(0)	29	1	GND
CWAIT(0)	31	I	GND
PCNTL(0)	14	0	No Connect
CS(0)#	30	0	No Connect
SRESET(0)	28	0	No Connect

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

- 1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- 2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor

National Semiconductor Corporation 1111 West Bardin Road Arlington, TX 76017 Tel: 1(800) 272-9959 Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe

Fax: +49 (0) 180-530 85 86 Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-534 16 80
Italiano Tel: +49 (0) 180-534 16 80 **National Semiconductor** Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408