Mass Storage— SCSI Hard Disk Drive

National Semiconductor
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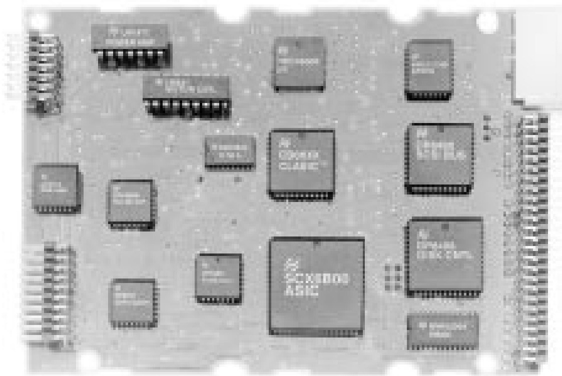

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SYSTEM DESCRIPTION

Rigid magnetic disk drives have shrunk considerably over the years to today's 5¼-, 3½- and 2½-inch form factor drives that are used in virtually every type of computer, including ''notebook'' computers. Data capacities range from 40 Mbytes for the 2½-inch drives to over 1 Gbyte for the 5¼-inch drives.

A disk drive consists of one or more platters and read/write heads, a spindle motor, a read/write head actuator and all of the associated control electronics. Previously a portion of the control electronics was located on a disk controller card external to the disk drive, but today almost all new drives being developed are so-called ''intelligent'' drives with this circuitry embedded in the drive itself. The two most common interfaces provided by intelligent drives to a host computer are SCSI (small computer system interface) and AT bus (the bus used in IBM-compatible personal computers; drives using this interface are also called integrated drive electronics (IDE) drives.

The functions performed by the circuitry in an intelligent disk drive are: conversion of the very low-level analog signals from the read/write head to a digital data stream and vice-versa (read/write channel), error detection and correction while performing serial-to-parallel data conversion and transfer to buffer memory (disk controller), transfer of data from buffer memory to host system bus (bus interface), overall control (microcontroller), spindle motor speed control and head position/servo control. The read/write channel consists of several ICs that include a pulse detector, data synchronizer, encoder/decoder (ENDEC), servo detector and frequency synthesizer. A major effort is under way by IC suppliers to reduce the entire read/write channel to a single chip. For the disk controller and bus interface functions, the state of the art today is for both to be in a single IC. Microcontroller usage is rapidly evolving from 8-bit to 16-bit processors as servo control moves from an analog implementation to a digital solution. The other functions in a drive, motor speed and head position control, are also moving toward single-chip solutions.

KEY DESIGN CHALLENGES

- Increase Data Density on the Platter—Packing more bits per square inch means reducing the amplitude of the magnetic flux change the read/write head sees for each bit, and this requires careful design of the read/write channel in order to extract data from very low-level analog signals in the presence of significant background noise. A technique also being employed is zoned density recording (ZDR), where different read/write clock frequencies are used according to how far a given track is from the center of the platter in an effort to maintain relatively constant flux density across the platter (previously, a single frequency read/write clock was used for all tracks resulting in decreasing flux, and data, density as the head moves from inner to outer tracks).
- Increase Data Rates—This further complicates the read/write channel design, and also requires the entire data path from disk controller to buffer memory to bus interface to be faster.
- Decrease Access Times—This requires sophisticated servo techniques.
- Shrink the Drive Form Factor—This requires advanced surface-mount packaging technology as well as higher levels of circuit integration. Advanced means not only shrinking the package footprint but also the package height, which becomes critical for 2½ inch form factor, 0.6 inch high drives.
- Decrease Power Consumption—This requires sleep/power down modes as well as semiconductor process technology that facilitates low-power designs without sacrificing performance, like BiCMOS.
- Meet All of the Above at the Lowest Possible Cost—This requires both analog and digital semi-custom ICs to integrate the ''glue'' circuitry needed to accommodate the specific combination of platters, read/write heads, spindle motor and head actuator for a given drive.

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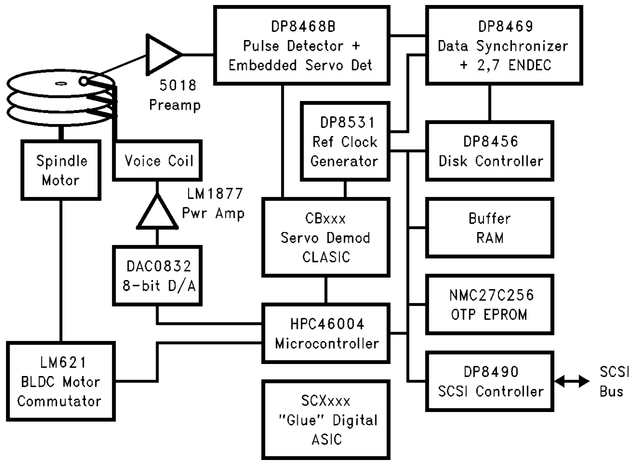
Silicon Solution for a Typical SCSI Drive



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KEY COMPONENTS

DP8531 Reference Clock Generator:

- Generates Variable Frequency Clocks for ZDR
- Microprocessor Bus Programmable

DP8456 Disk Data Controller:

- Programmable Disk Format
- 20 Mb/s Disk Data Rate
- 8 Mbytes/s DMA Transfer Rate

HPC46004 Microcontroller:

- High-Performance 16-Bit, 30 MHz CMOS Microcontroller
- 16 x 16 Multiply, 32 x 16 Divide
- 512 Bytes On-Chip RAM
- Four Input Capture Registers
- Eight PWM Timers

Custom Linear ASIC (CLASIC™)

- 15V Bipolar LFAST (Linear Fairchild Advanced Schottky Technology) Process
- 13V LMCMOS (Linear CMOS) Process
- Standard Cell Methodology
- Complete PC-Based Linear CAD Toolset

Bill of Material

Function	Description	NSC Part	Quantity
Read/Write Channel	8 Channel Pre Amp	5018	1
	Pulse Dectector w/Embedded Servo	DP8468B	1
	Synchronizer/2, 7 ENDEC	DP8469	1
	Reference Clock Generator	DP8531	1
Disk Controller	Disk Data Controller	DP8456	1
SCSI Bus I/O	Enhanced Asynchronous SCSI Interface	DP8490	1
Microcontroller	16 Bit, ROMless/512 Bytes RAM	HPC46004	1
Memory			
EPROM	32k x 8 CMOS OTP EPROM	NMC27C256	1
SRAM	32k x 8 SRAM		1
Temperature Reference	°F/°C Temperature Sensor	LM34/LM35	1
Voltage Reference	Voltage Reference	LM385	1
Motor			
Speed Control	Brushless DC Motor Commutator	LM621	1
Driver	Power FET	IRF9220	3
	Power FET	IRF220	3
Head			
Position Control	8-Bit D to A	DAC0832	1
Driver	Power Amp	LM1877	1
Logic			
System ASIC	Glue Logic and Interface (Note 1)	SCXxxx	1
Analog			
System ASIC	Glue Analog and Servo Control (Note 2)	CBxxx	1

Note 1: The systems Digital ASIC may be designed using National's broad ASIC capabilities.

Note 2: The system analog ASIC may be designed using National's CLASIC capabilities.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408