# μP Interface for a Free-Running A/D Allows Asynchronous Reads

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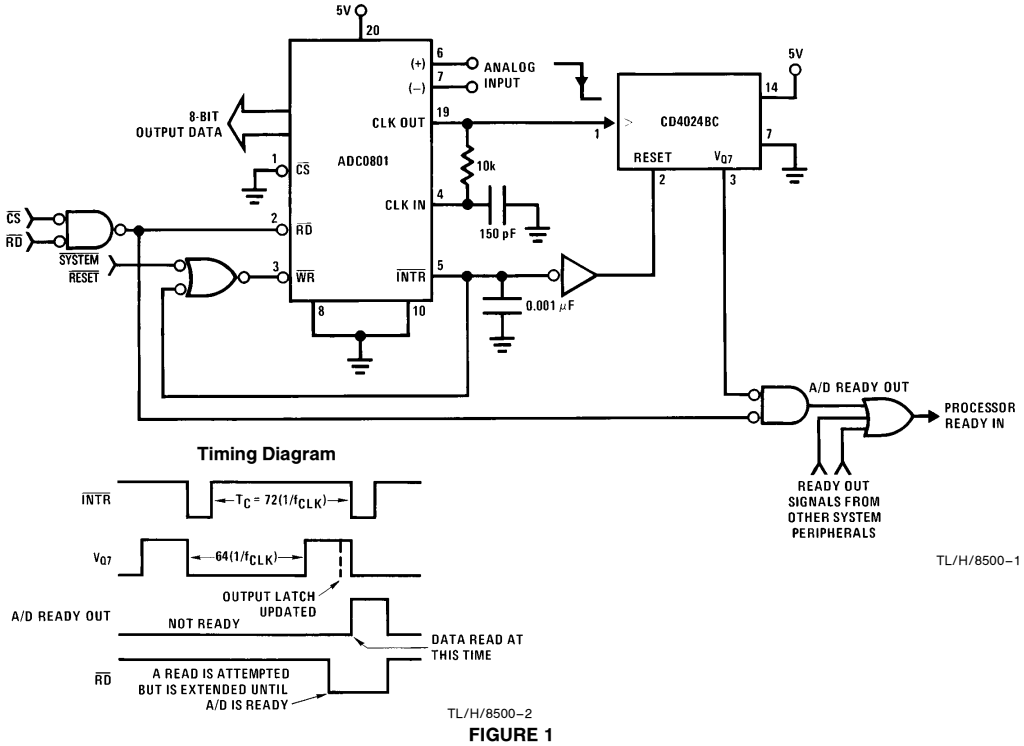
In many data acquisition applications it is necessary to have an A to D converter operate as its maximum conversion rate. The controlling microprocessor would then be able to read the most current input data at *any* point in time as required by software. To minimize program execution time, a DATA READ may not be snychronous to the completion of a conversion, and herein lies a problem. It is entirely possible that the processor could assert a READ command right at the instant the A/D converter is updating its output register. The data read would be the value of the converter's output lines in transition from the result of the previous conversion to the latest result, and would very likely be in error.

The addition of a simple binary counter to the A/D interface circuitry can be used to generate a READY signal to the microprocessor that will prevent a READ during a data update. The circuit of *Figure 1* shows a CD4024BC7-stage ripple carry binary counter used in conjunction with an ADC0801, 8-bit microprocessor compatible A to D converter. Circuit operation relies on two basic properties of the A/D converter. First of all, the free-running conversion time of the A/D must be a constant number of clock cycles; and secondly, the output latches must be updated prior to the end of conversion signal. The ADC0801 fulfills both of these requirements. The output data latches are updated one A/D clock period before the $\overline{INTR}$ falls low, and the free-running conversion time is always 72 clock periods long.

As part of the system power-up initializaton sequence, a logic low must be temporarily applied to the $\overline{SYSTEM\ RESET}$ input to the A/D to force the converter to start. At the end of a conversion, the $\overline{INTR}$ output goes low, and both resets the counter outputs to all zeros and signals another conversion to start by pulling $\overline{WR}$ low. The length of time that the $\overline{INTR}$ output stays low is normally only a few internal gate propagation delays (approximately 300 ns) and is independent of the A/D clock frequency. The 1000 pF capacitor on this output extends this time to approximately 1 μs to insure adequate reset time for the counter.

A conversion is started on the low to high transition of the $\overline{INTR}$ and $\overline{WR}$ pins. The next data update will occur 71 clock periods after this edge occurs. The counter will signal that a data update is about to occur after 64 clock periods. If the processor attempts a DATA READ within an 8 clock period time frame around the data update time, its READY input line will remain low, signifying a NOT READY condition. The processor would then extend the READ cycle time until it receives a READY indication created by the counter being reset by $\overline{INTR}$. This insures that the latches have already been updated and proper data will be read.

If a READ is attempted during the 64 clock period interval after the start of a conversion, the READY IN line to the processor will go high to permit a normal READ cycle, and




**Timing Diagram**




**FIGURE 1**



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the data output by the A/D will be the result of the previous conversion. The processor READY IN logic, as shown, requires that all system devices that may need special READ or WRITE timing provide a NOT READY (a Logic 0 on their READY OUT lines) indication until selected to be read from or written to.

The chance of having the processor extend its READ cycle time is 1 in 9 (8 clock periods out of 72) and the maximum length of time a READ would be extended is 8 A/D clock periods. These two timing considerations are insignificant trade-offs to take to insure that proper A/D data is always read.



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