National Semiconductor

# National's Design for Test Solutions with Boundary Scan

## What is DFT?

Design for Test, or DFT, is being used by many companies to lower the overall cost of development, manufacturing, test and field service. Some companies call it ''Concurrent Engineering'' and it replaces the ''Over-the-wall'' method of product development. In each stage of the product life-cycle, a consideration for testing is made in the earliest stages of design.

National employs boundary scan technology to enable not just chip testing, but also board testing, system testing, and in-field service testing.

What is the standard? For most purposes the following terms are used interchangeably:

IEEE 1149.1

1149.1

JTAG

Dot 1

Boundary Scan

SCAN

IEEE 1149.1 is a set of standards for *board* test protocol. Newer standards are being developed by different IEEE working groups for *system* test and *analog* test protocol. IEEE 1149.1 is a 4-wire standard which allows compliant silicon to perform interconnect testing. It supports BIST (Built In Self-Test), and provides an alternative or supplement to Bed of Nails testing and functional testing.

Adding boundary scan to a board does add cost and time to the design cycle due to the increased cost of boundary scan compliant components and initial time investment required to understand the boundary scan architecture and tools. However, these costs are easily justified when viewing the benefits and cost savings boundary scan provides at every stage of a product's life cycle. What was originally developed as a manufacturing test tool offers benefits before, during and after manufacturing.

## Board Development

A designer uses boundary scan to save time during the prototyping and design debug stage. With boundary scan, non design-related, structural faults can be detected and then eliminated at both the board level and component level. This allows designers to effectively locate and resolve design related problems. Additionally, designers use boundary scan to partition a board, load seed values for devices with BIST and/or load internal values into device registers (e.g. internal scan, LSSD, etc.) to isolate logic errors. With boundary scan, many of the vectors developed and used during the design phase can be passed on to manufacturing to provide an additional cost and time savings.

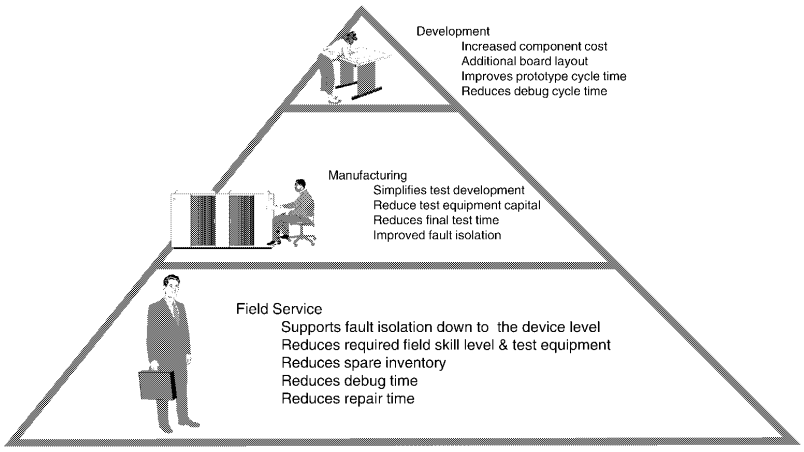


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**FIGURE 1. Boundary Scan Benefits Entire Product Life Cycle**

## Board Manufacturing

The key benefits at the manufacturing phase are test development time savings; improved fault coverage and diagnosis; and improved test throughput through reduced test times. As with the design phase, boundary scan provides the additional advantage of applying many of the vectors used for manufacturing to be later applied during field debug and diagnosis.

## Field Service

Field failures are often due to structural failures which surface due to the stress—temperature, humidity, vibration—that the boards are exposed to in the field environment. Using boundary scan, field technicians have the ability to quickly test for structural faults down to the component level without the burden of probing or returning the board to the factory. Eliminating these tasks allows for more efficient diagnosis and repair which reduces cost and system downtime.

The advantage of boundary scan become even more apparent when boundary scan is extended from the board level to the system level test.

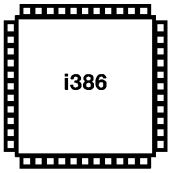
Often, the objection to the use of boundary scan include:

1. Performance (speed) decreases due to the extra delay added by the boundary scan multiplexer in the data path.
2. Cost increases due to additional silicon and TAP pins on the device package—as well as design time.
3. Delay to market due to additional circuit design time.

However, the manufacturing benefits as well as product development cycle time improvements easily outweigh the initial added efforts.

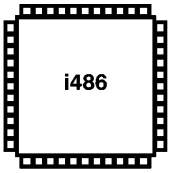
Using boundary scan on their 80486 design, Intel realized two orders of magnitude improvement in time to develop circuit test-patterns with significant cost reduction, too. See *Figure 2*.

Boundary scan provides cost savings over the life cycle of a system in the testing of boards, systems, and in field maintenance.




80386 Conventional ICT Patterns

| | |
|---|---|
| Study Part | 1 Weeks |
| Develop Test Patterns | 4 Weeks |
| Verify on ATE | 2 Weeks |
| Total Time | 7 Weeks ($14,000) |




80486 with VICTORY/1149.1 ICT Patterns

| | |
|---|---|
| Generate/Verify BSDL | 8 Hours |
| Generate Test Patterns | --- |
| Verify Patterns | 2 Hours |
| Total Time | 10 Hours ($500) |

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**FIGURE 2. Intel Reduced Test Development Time and Test Cycle Time**

## The Economics of Design for Test

Many of the perceived costs of a DFT strategy fall upon the design organization, while many of the benefits reward the manufacturing and test organizations. This adversarial position can be eliminated by meeting the needs of all organizations involved in DFT.

**EFFECT OF DFT BY DEPARTMENT**

| | | |
|---|---|---|
| Design | Die Area | Increased Cost |
| | Design Cycle Time | Lowered Cost |
| | Performance Impact | Increased Cost |
| | EDA Tools | Increased Cost |
| Test | Fault Simulation | Lowered Cost |
| | Simplified Debug & Diagnostics | Lowered Cost |
| | Fewer Design Changes | Lowered Cost |
| | Lower ATE Cost | Lowered Cost |

**IMPACT OF DFT VARIABLES BY DEPARTMENT**

| Profit Factor | Department | Impact |
|---|---|---|
| Units Sold | Design | New product feature, faster design cycle time |
| | Marketing | Lower selling price through cost reduction |
| | Sales | Lower selling price |
| Selling Price | Design<br>Marketing<br>Sales | New product features of higher quality |
| Variable Cost | Marketing<br>Sales<br>Manufacturing<br>Design | Higher cost of silicon, lower overall manufacturing costs |
| Fixed Cost | Manufacturing | Lower cost ATE, more productive ATE (higher throughput), improved fault coverage |
| | Field Service | Less field spare inventory, faster debug and diagnosis |
| Total Profit | Management | Overall investment strategy, capital utilization, ROA, cost calculation methods |

Boundary scan also provides cost savings which can be measured directly in production and can reduce the time to market. This method fits within a concurrent engineering environment in various ways:

- Reduces test time and costs
- Reduces test preparation time and costs
- Increases the time available for test programs for production
- Allows simpler, less costly testers
- Shortens diagnostic times
- Provides a commonality of tester interface
- Allows the continued test of high density/poor-access boards

## Where the Failures Are

PCB test failures can result from either structural faults (opens, stuck-ats, bridging, missing/wrong components, etc.), analog failures (faulty or incorrect passive components) or performance faults (timing problems or board/component design errors). However, structural faults account for the overwhelming majority of board failures during manufacturing test. In fact, data from Teradyne, a leader in the test industry, suggests that greater than 80% of the board level test manufacturing failures are structural in nature. See *Figure 3*.

## Where the Failures Are (Continued)

A number of methods have been implemented to provide a means of detecting structural failures. These methods range from use of functional board testers (FBT) to in-circuit testers (ICT) and combinational (ICT and FBT) testers. Boundary scan was created to provide an improved technique for screening structural faults through reduced test programming time and improved fault coverage.

It should be noted that boundary scan is not a technique for detecting at-speed, dynamic performance faults. Performance fault testing requires the use of an at-speed functional board tester. With very thorough debug and simulation during board development and pre-assembly test of board components, the need for performance fault testing during manufacturing is up to the discretion of the board manufacturer and its customers. Even if at-speed functional testing is required, the use of structural testing prior to functional testing will help eliminate manufacturing defects and ease the diagnosis of performance or functional failures.

For the cases where access is possible, the access occurs at a price. Even if it is possible to add test pads, pads consume board area—contrary to the goal of saving board area—and can present performance degradation. Additionally, the cost increases substantially for test point fixtures, the fine tip probes or clam shell probes for double sided boards. See *Figure 4*.

For the case of MCMs (multi-chip modules) and inaccessible board nodes (nodes under a mezzanine card, blocked by a component or other hardware, etc.), access is not possible and the only option other than boundary scan is cluster testing: using bed of nails to apply stimulus on MCM or board cluster inputs and measure values at outputs of the MCM or board cluster. This creates the same burdens as when using a FBT, where creating test vectors requires knowledge of the entire MCM or board cluster functionality which increases test development, diagnostics and test time.

The existence of inaccessible nodes in manufacturing are passed on to the field service engineer attempting to use manual probing as a vital step in debugging a board failure. This leads to increased field service time and costs and, longer system down time for your customer.

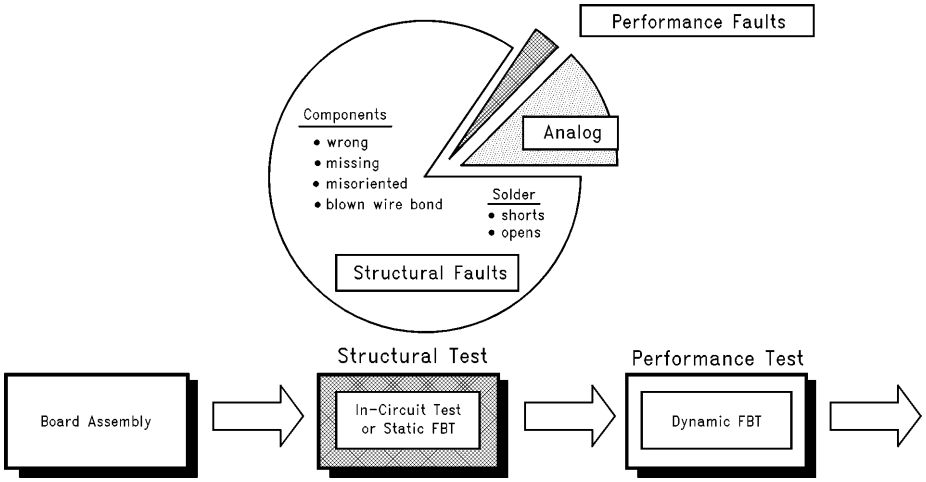


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**FIGURE 3. The Majority of Printed Circuit Board (PCB) Manufacturing Failures Are a Result of Structural Faults**

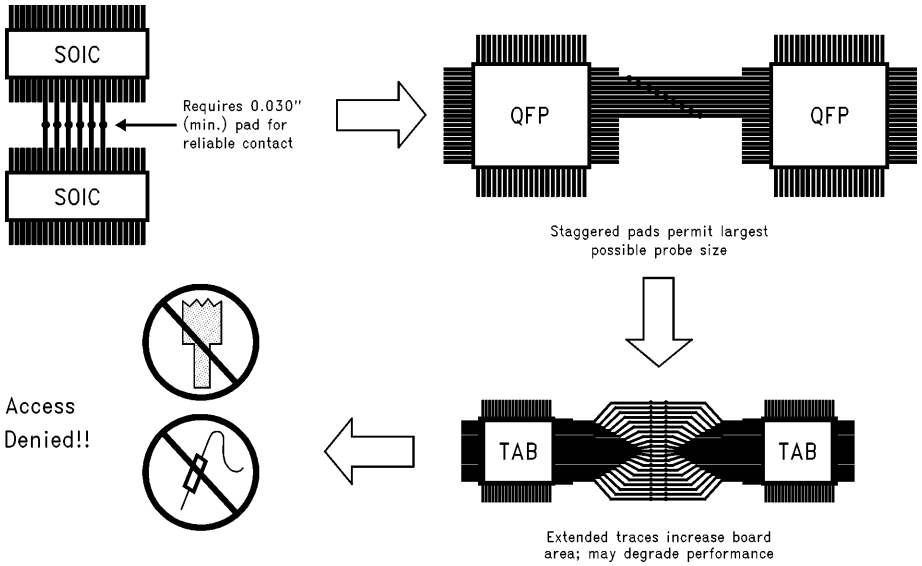


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**FIGURE 4. Device Packaging Density Makes Physical Access Expensive, Unreliable, or Impossible**

**Boundary Scan Fundamentals**

The IEEE 1149.1 standard defines a 4 pin TAP (Test Access Port) which allows electrical access around the "boundary" of compliant devices. The TAP pins are:

| | |
|---|---|
| TDI | Test Data In |
| TDO | Test Data Out |
| TMS | Test Mode Select |
| TCK | Test Clock |

It also defines a 16 state TAP Controller and several registers used to control the test data.

Boundary scan registers are placed at all I/O pins, and they are interconnected to form a serial chain around the core functionality of the device.

With the addition of the boundary scan registers at the I/O of a component, interconnect testing with boundary scan devices can be performed with no dependence on device functionality. IEEE 1149.1 compliant automatic test program generation (ATPG) tools are available from a number of vendors to automatically generate interconnect tests using a board netlist and BSDL files for each 1149.1 compliant device on the board as inputs. BSDL files provide a description of the specific implementation of boundary scan features within each compliant component.

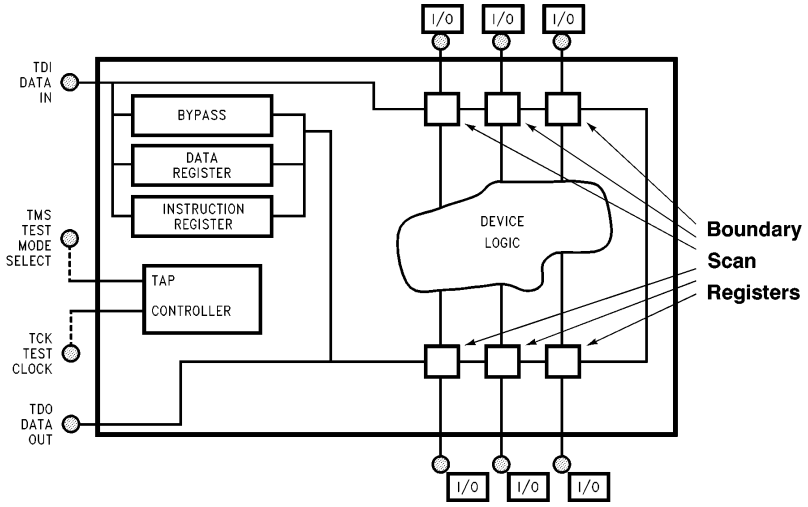


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**FIGURE 5. 1149.1 Device Hardware**

In like fashion as the chip, the boundary scan chain is extended to the board in a serial scan chain. Boards in systems can also be linked in a scan chain.

When placed on a printed circuit board, each 1149.1 component is connected together to form a chain of boundary scan devices. In *Figure 6*, note the scan chain connections:

**TDI/TDO:** The tester's serial test data out pin is connected to the first device's TDI. The test data is passed from the first device to the second device via the TDO pin which connects to the second device's TDI pin. This chain formation continues until the last device's TDO pin is connected back to the tester. Therefore, shifting data into a device's instruction or data registers requires that the data passes through every JTAG device which is connected ahead of the device in the scan chain. Additionally, as the data is shifted into the device, the data previously stored in the selected instruction or data register is shifted out of the chain. The tester software either reads and evaluates the returning data or masks it out. The Bypass register is included to shorten the chain when shifting data through devices which are not participating in a given scan operation.

**TCK/TMS:** All devices in the chain are connected in parallel to the TCK and TMS signals. This means that all the devices' TAP controllers are in the exact same state and transition simultaneously. The instruction register allows each device to include different data registers in the scan chain and perform different scan operations.

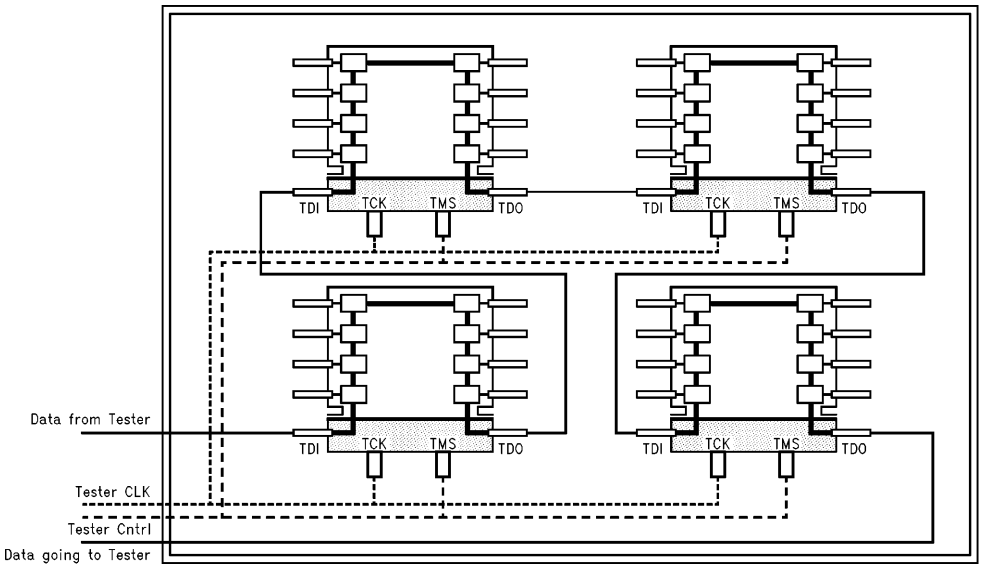


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**FIGURE 6. 1149.1 Boundary Scan Chain**

Implementing boundary scan on every component on the board provides the maximum benefit in terms of reduced tester cost, test development times and concurrent engineering. However, boundary scan can also complement an ICT in testing structural faults. See *Figure 7*. This was fully recognized by ICT tester companies when they developed their ICT systems and most ICT's now have a connector dedicated for boundary scan testing. Additionally, these tester companies included the option of mixing boundary scan and ICT in their ATPG tools by using ICT component libraries for non-scan products and BSDL for scan products. For example, vectors can be automatically generated to drive signals with boundary scan and compare results using physical test probes. Many companies have already invested millions of dollars in ICTs and may want to use boundary scan only where required for inaccessible nodes, non-library parts, etc. or as a means of cutting ICT fixture costs.

For smaller companies or companies in the process of purchasing new ICT equipment, implementing boundary scan may provide a way to reduce the required ICT features like number of channels providing a tremendous reduction in the tester cost where cost ranges from $200K up to $1M.

*Figure 7* shows two examples of ICT and boundary scan working together. The lower of the two graphics shows cluster testing. Cluster testing is the testing of a group of devices by applying data to the inputs of the group or cluster and evaluating the results on the output of the group or cluster. Cluster testing can vary from testing the interconnects between the components in the cluster to testing the internal nodes of each component within the cluster.

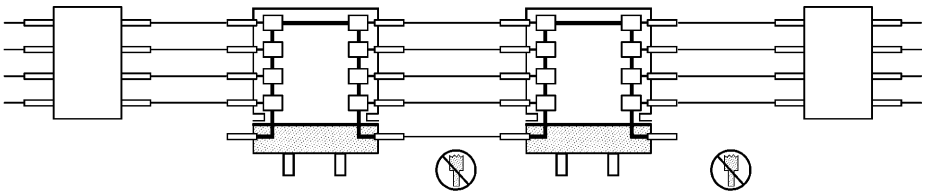
## System Test

National supports the needs of the system design architect by:

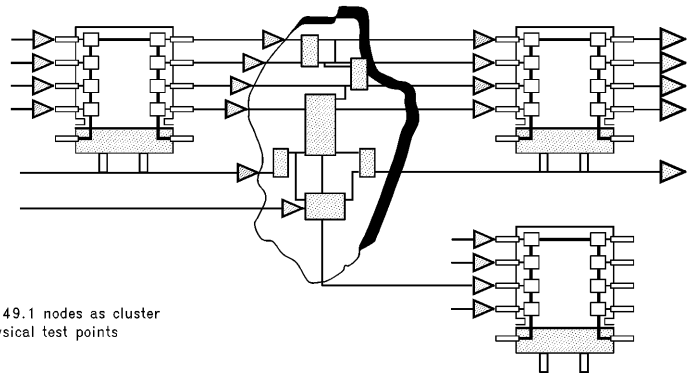
- Acknowledging the need for live insertion on the backplane
- Fully complying to IEEE 1149.1 (board test)
- Addressing the 1149.5 standard (system test)

While boundary scan diagnostics are particularly useful for telecommunications and workstations, their benefits also extend to board manufacturers that want to reduce the time-to-market of their products.

For small companies, we provide the option to expensive $1 million test equipment. With help from our software and hardware partners (such as Corelis and JTAG Technologies), National can support total system test solutions with PC-based boundary scan devices, software, and hardware solutions.



Boundary scan works with an ICT to provide access to inaccessible nodes and/or to reduce ICT physical test points



Treating non-IEEE 1149.1 nodes as cluster can eliminate ICT physical test points

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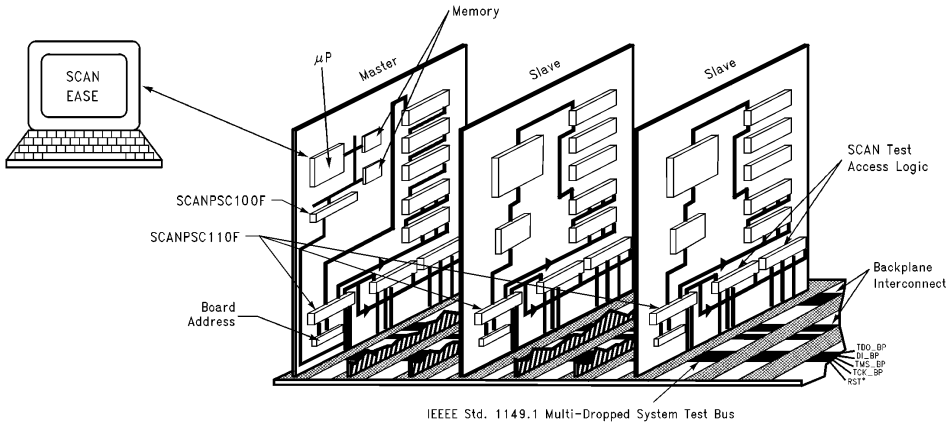
**FIGURE 7. Boundary Scan and ICT Can Work Together**

**HOW IT WORKS**

For system test and diagnostics, start with the Embedded Boundary Scan Controller, SCANPSC100F and your choice of microprocessor and memory to create an embedded test master, freeing up external test equipment.

Add the Hierarchical and Multidrop Addressable JTAG Port, SCANPSC110F Bridge to each board in the multidrop or hierarchical backplane to address any number of boards, selectively or in groups, for board test as well as backplane interconnect failures. If a board is off-line or removed, the scan chains remain unbroken.

But what if a board is removed while powered up? Then add SCAN ABT Test Access Logic along the back-plane card edge to provide fault-tolerant power-up and power-down live insertion. Now backplane interconnect checks can be performed and boards inserted/removed through controlled power-up/power-down sequences. The 25Ω series resistors on SCAN ABT outputs also eliminates the need for an external damping resistor.




- SCAN EASE Compatible with 1149.1 hardware and existing test board vectors
- SCANPSC100F creates embedded test master
- SCANPSC110F enables individual board addressing, multiple and hierarchical boards for testing "like" boards simultaneously
- SCAN ABT live insertion

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**FIGURE 8. Creating Embedded System Test**

## System-Level Embedded Test

Developing hardware and software to implement embedded test capability can be significant in terms of both time and expense. To reduce our customers' in-house software development efforts, National offers SCAN EASE to apply, control, and evaluate tests within an 1149.1-compliant embedded system. For more examples refer to AN-1022, Boundary-Scan, An Enabling Technology for System Level Embedded Test.

**SCAN EASE TOOLS**

SCAN EASE (Embedded Applications Software Enabler) is a suite of software tools that enables ATPG (Automatic Test Program Generation) or custom-generated test vectors to be embedded within an IEEE 1149.1 compatible system. See *Figure 9*. SCAN EASE includes three groups of tools:

- EmbedPrep
- EmbedTest
- EmbedComm

**TEST DEVELOPMENT PROCESS**

The test development process for embedded system test begins with generating tests using an off-the-shelf ATPG tool. See *Figure 10*. Separate tests are created for each board type in the system during manufacturing test development. These tests can be re-used for embedded test. National's SCAN EASE includes tools to compile test vectors stored in Serial Vector Format (SVF) or Pattern Format (PAT) into Embedded Vector Format (EVF) for use with EmbedTest. EVF is a compact binary vector format suitable for embedded applications. Several of the board-level EVF files can be concatenated to create a system-level test. Partitioning tests enables EmbedTest to isolate and report pass/fail information to the partition level (board, module, etc.) without running diagnostic software. EVF test files can be located in ROM for power-up self test or down loaded to RAM.

EmbedTest provides a set of functions that enable communication between the embedded system and a serial interface to a system administrator or remote computer. EmbedTest commands—such as configuration, reporting test results, downloading new tests, and uploading data logs—are performed over this interface.

Note that SCAN EASE is also included in our SCAN Developer/Demo Kit. This kit demonstrates system board check, interconnect testing, and backplane testing (see *Figure 8*). Included are:

- Embedded Boundary Scan Controller—SCANPSC100F works with customer's choice of microprocessor
- Multidrop and Hierarchical Addressable JTAG Port SCANPSC100F SCAN Bridge for system test—addresses any number of boards in the backplane
- SCAN ABT Test Access Logic—provides live insertion capability for boards along the backplane

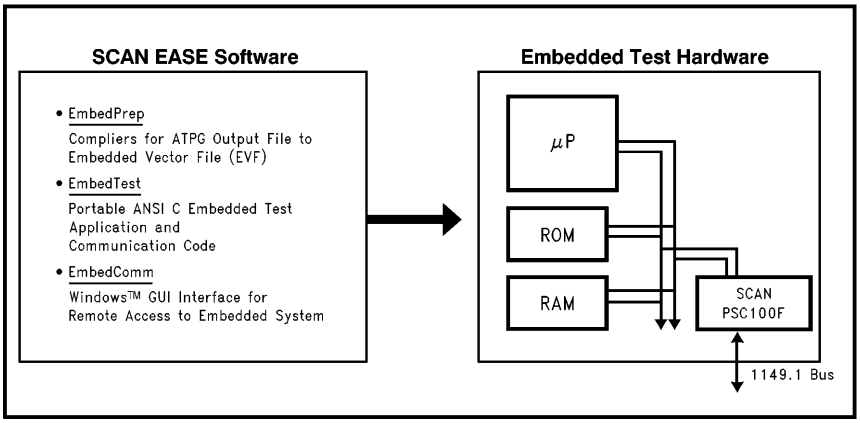


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**FIGURE 9. SCAN EASE Enables ATPG Test Vectors to be Embedded**

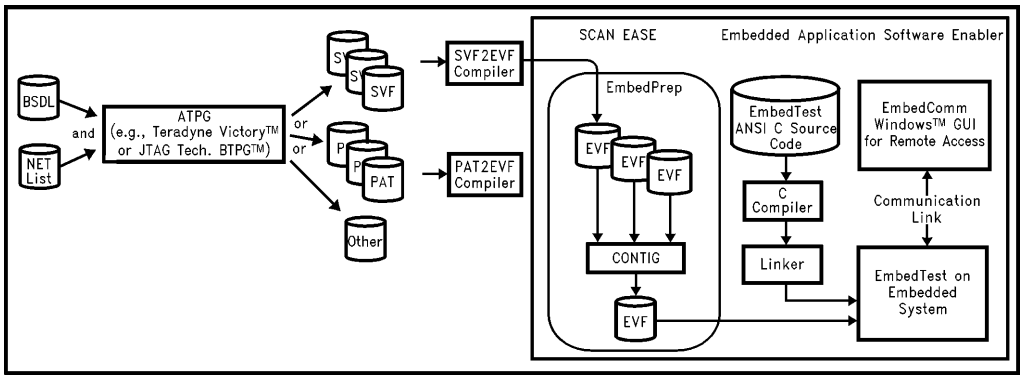


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**FIGURE 10. SCAN EASE Reuses Existing Test Vectors, Compiles them for your Target Microprocessors and Compresses them for Storage in Memory**

### The Impact of PC and Communications Technology

The market is ripe for the valuable services provided by PC-based and in-system testing. Having a system perform its own self-test upon power-up frees up design engineers to add more features to an end system, as opposed to spending money on testing a system. With advances in PCs, the capability of remote testing now exists. It is possible to dial up a modem service, connect to a remote system in the field and perform maintenance, improving the end-system up-time. Once the target site is on-line, the system performs self-testing and reports back failures.

There are many factors associated with improving end-system uptime including systems that require high reliability, systems that perform services for large groups of people or customers that need to stay on-line all the time. Initially SCAN EASE will diagnose the problem for the purpose of repair. Since vectors are stored in ROM, it will be easy to download system upgrades and new system configurations in the near future.

Recent applications have arisen to extend the use of IEEE 1149.1 boundary scan all the way to system integration and field service. This new arena boasts additional leverage for the re-use of test vectors, improved time to break-even for products and increased value to end-users.

What products will result from this tecnology? A tester on a chip will go into simple machines that give people trouble like printers, copiers, facsimile machines, and give them the intelligence to do power-on self-test, diagnosis and repair. The machine will be able to call the home office through advanced communications capabilities, communicate with the home office, literally saying, ''This is what is wrong with me.'' Remote verification of the diagnosis as well as repair can then take place.

On an even wider scale, telecommunications equipment buried in remote locations will be accessible. Board will be tested, brought off-line, and others brought on-line to replace them—electronically and remotely.