

## Boundary Scan Design Support

### Information on IEEE Standards

The IEEE Working Group developed the IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Scan Architecture. To purchase this book [\$50], please call one of the following numbers and ask for SH13144:

In the USA: 1-800-678-IEEE

Outside the U.S. or Canada: 1-908-981-1392

#### Some Excellent Literature Written on Boundary Scan Includes:

1. *Boundary-Scan Test, A Practical Approach* by Harry Bleeker, Peter van den Eijnden, Frans de Jong, Kluwer Academic Publishers
2. *The Boundary-Scan Handbook* by Kenneth P. Parker, Kluwer Academic Publishers
3. *The Test Access Port and Boundary-Scan Architecture* by Colin M. Maunder and Rodham E. Tulloss, IEEE Computer Society Press (1-800-CS-BOOKS)
4. *IEEE 1149.1—1994 SCAN Tutorial Handbook* by National Semiconductor, call 1-800-272-9959, Customer Response Center.

### CONFERENCES

An excellent platform for seeing the latest developments in boundary scan support is to attend conferences. One of the biggest is the International Test Conference (ITC) held annually in the fall.

In Europe, the European Test Conference (ETC) is held every other spring. For more information call the IEEE Computer Society in Brussels at: 32-2-7702242.

### BSDL Models

The BSDL (Boundary Scan Description Language) is designed as a subset and standard practice of VHDL, a standard language for describing the testability features of our boundary scan devices.

National Semiconductor will supply the BSDL models on a floppy to you, free of charge.

National has BSDL models available today on the following devices:

18-bit CMOS Test Access Logic

SCAN18245T

SCAN18373T

SCAN18374T

SCAN18540T

SCAN18541T

18-bit BiCMOS Test Access Logic

SCAN182245A

SCAN182373A

SCAN182374A

SCAN182541A

SCANPSC110F Hierarchical and Multidrop Addressable JTAG Port

To obtain BSDL models, call **1-800-341-0392 x4500** and ask for the SCAN Applications group, or download from National's site on the World Wide Web: <http://www.natsemi.com>.

### Other Simulation Models

National recognizes that our end customers require simulation models of our devices.

The following companies offer various models for National products:

Synopsys/Logic Modeling, 503-690-6900,  
[modelinfo@lmc.com](mailto:modelinfo@lmc.com)

Zeelan Technology, 503-520-1000, [zeelan@netcom.com](mailto:zeelan@netcom.com)

Quad Design/VIEWlogic, 805-988-8250,

<http://www.view.logic.com>

**Other Simulation Models** (Continued)

Please contact *Logic Modeling* at the following locations:

**U.S. HEADQUARTERS**

19500 N.W. Gibbs Drive  
P.O. Box 310  
Beaverton, OR 97075  
Tel: (503) 690-6900  
Fax: (503) 690-6906  
Tech. Product Support:  
1-800-445-1888

**LM Division**

1520 McCandless Drive  
Milpitas, CA 95035  
Tel: (408) 957-5200  
Fax: (408) 945-9181

**VHDL Division**

4500 East Pacific Coast Highway  
Suite 210  
Long Beach, CA 90804  
Tel: (310) 494-4127  
Fax: (310) 494-8106

**European Headquarters**

Doncastle House  
Doncastle Road  
Bracknell, Berks RG12 8PE  
England  
Tel: 44-344-300833  
Fax: 44-344-300844

**France**

Immeuble Ampère  
Rue Ampère  
95300 Pontoise  
Tel: 33-1-30-75-95-02  
Fax: 33-1-30-38-45-70

**Germany**

Logic Modeling GmbH  
Stefan-George-Ring 24  
D-81929 Muenchen  
Tel: 49-89-930-30-25  
Fax: 49-89-930-58-47

**Japan**

Logic Modeling Co., Ltd.  
Mizonokuchi-Daiichiseimei Bldg. 7F  
3-3-2 Hisamoto, Takatsu-ku  
Kawasaki-shi Kanagawa Pref. 213  
Japan  
Tel: 81-44-813-5781  
Fax: 81-44-813-5731

**Korea/Asia-Pacific**

Leema Bldg.  
Suite 400  
146-1 Soosong-Dong  
Chongro-Ku  
Seoul  
Tel: 82-2-720-0400  
Fax: 82-2-722-4497  
TLX: Suite K22652

We are in the process of evaluating which types of models are requested most often by our customers. Please contact our Applications Group (1-800-341-0392) and let us know the most preferred simulation support you would like to see with our future SCAN products.

**Boundary Scan Support Providers**

Below is a brief list of suppliers. Please contact them for more information on their boundary scan support products:

**Corelis Inc.**

12607 Hidden Creek Way  
Cerritos, CA 90701  
310-926-6727

**GenRad, Inc.**

300 Baker Avenue  
Concord, MA 01742-2174  
1-800-4-GENRAD

**Hamilton Hallmark**

Technical Support Center  
1-800-605-3296  
<http://www.tsc.hh.avnet.com>

**Hewlett Packard**

815 S.W. 14th  
Loveland, CO 80537  
<http://www.hp.com>

**JTAG Technologies**

Eindhoven  
The Netherlands  
+ 31 40 7 82584

**Synopsys Europe**

Stefan-George-Ring 6  
D-81929 Munich  
Germany  
011.49.89.99.59.12.30  
<http://www.synopsys.com>

**Synopsys N. America**

700 East Middlefield Rd  
Mountain View, CA 94043  
1-800-445-1888  
Logic Modeling Product Information  
1-800-346-6353

**Teradyne**

321 Harrison Avenue  
Boston, MA 02118  
617-422-3567  
<http://www.teradyne.com>

**Test Economic Services**

270 Hyde End Road  
Spencers Wood  
Reading  
Berks. RG7 1DL

**United Kingdom**

44.1734.88.37.57  
[tony.ambler@brunel.ac.uk](mailto:tony.ambler@brunel.ac.uk)

## Boundary Scan Tools Available from National

- *Test Cost Spreadsheet Model for ASICs and Boards*—Floppy disk and documentation; helps calculate development costs; employs Excel spreadsheet and Macros.
- *SCAN Remote and Embedded System Test Demonstration and Developer Kit*—Hardware to borrow. Includes Test Master board with  $\mu$ P, RAM/ROM, and SCANPSC100 Embedded Boundary Scan Controller; backplane populated with slave cards containing SCANPSC110 JTAG Addressable Port (Bridge), SCAN CMOS Test Access Logic and SCAN ABT Test Access Logic. Demonstrates built-in self-test upon power up; backplane interconnect test; missing board test; board partitioning and test; download of new test vectors to RAM; live insertion of slave cards. LED displays included to allow boundary scan controller TAP states to be monitored during demonstration and development. Contact SCAN Applications Group at 1-800-341-0392 x4500.
- *1994 SCAN Tutorial Volume I*—Co-developed by Tera-dyne and National, it describes JTAG terminology, methods, applications for use.
- *The Economics of Design for Test*—Series of 3 articles, co-authored by Gary O'Donnell, National Semiconductor; Prof. Tony Ambler, Brunel University; R. G. Ben Bennetts, Synopsys; Harry Bleeker, JTAG Technologies. Identifies enabling technologies, barriers to adoption, clarifying the costs. Reprinted from *Evaluation Engineering Magazine* (9-11/94).
- *Live Insertion for SCAN and VME Gets Attention*—Article reprint from *Electronic Engineering* (12/94), on SCAN ABT Test Access Logic for live insertion applications.
- *IRIDIUM Satellite: A Large System Application of Design for Testability*—Article reprint from IEEE International Test Conference 1993. Discusses application of system-level boundary scan (based on the National SCANPSC110) in the Iridium satellite program.
- *Boundary-Scan-Based System Test: Comparing Two Approaches*—Article written by National that compare our SCANPSC110 Bridge with Texas Instruments' offerings. Published 3/94 in *Electronic Engineering*.
- *Six Good Reasons Why Boundary Scan Should be Designed into a Board*—Written by Alan Nelson, Marconi Instruments; advocates the benefits boundary scan provide at all steps of the product life cycle (design prototype through field repair). Presented at NEPCON 1994.
- For articles call 1-800-341-0392 x4500 and ask for SCAN Support.