National Semiconductor

CLC952 Evaluation Board

Part Number CLC952PCASM

January 1997

Description

The Comlinear 952PCASM evaluation board is designed to support simple and effective evaluation of the CLC952 Analog-to-Digital Converter (ADC). This evaluation board can be used for the CLC952ACMSA, as well as several forthcoming products: CLC952BJMSA, CLC951, and CLC953 will all have the same pinout. The evaluation board is supplied loaded and tested, with a CLC952ACMSA converter installed. To test the ADC you need only to supply power, a clock, and a signal to be digitized. The evaluation board uses a common Eurocard connector to make the power, ground and data connections with the rest of your evaluation system. The analog input signal and clock enter the board through SMA connectors. Clock options on the board facilitate testing with either sinewave, ECL, or TTL level clocks. Another option allows duty cycle shaping with a sinewave clock source. Output data is available in two's complement and offset binary coding.

Default Configuration

The CLC952 evaluation board is shipped configured for a sinewave (or ECL) clock input. This means that zero ohm jumper resistors **OPT1A**, **OPT1B**, **OPT1C**, **and OPT1D** are installed. Resistors **OPT2A**, **OPT2B**, and **OPT2C** are not installed (open). The default configuration for duty cycle is 50%, so **R2** is zero ohms while **R3**, **R5**, **R6**, and **R8** are open.

Clock Generation

The clock is provided to the board through an SMA connector, regardless of the clocking option chosen. The evaluation circuitry includes a clock generation circuit that will convert a sinusoidal signal to the TTL levels required by the CLC952. The default clock circuit is shown in Figure 1. Note that the 10EL125 package is actually marked "HLT25."

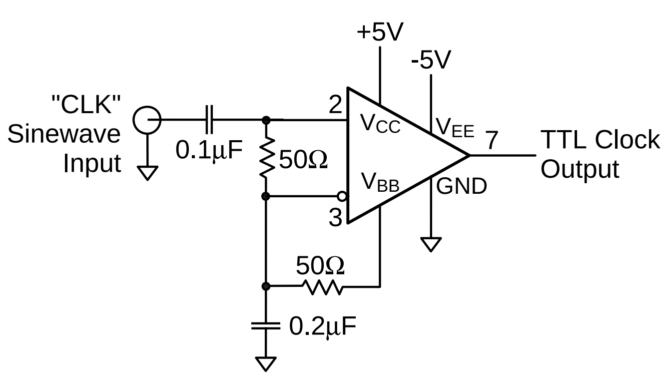

Figure 1. Default Clock Circuit

The amplitude of the sinusoidal signal should be 2-3V_{pp} (10-14dBm). For best results when digitizing high speed input signals, the converter must have a very low jitter clock. To generate this the sinusoidal input must have very low phase noise. In a laboratory environment, Comlinear suggests the use of a low phase noise synthesizer such as the HP8662 or the HP8643 as a sinewave source. If a low-jitter ECL level clock is available, it may of course be used with this circuit as well. Note that "low-jitter" in this context means much less than 5ps.

Note that the sinewave is AC-coupled into the 10EL125. Both inputs of the 10EL125 are DC biased to the VBB threshold voltage. This removes any DC offsets from the signal source and provides a nominal 50% duty cycle clock to the converter. The converter is tested, specified, and recommended for operation with a 50% duty cycle. However, for low clock rates (less than 1 MSPS), droop in the Track/Hold circuitry internal to the converter will limit performance. If operation at low sample rate is required, a shaped clock can be used. The encode signal should be limited to a maximum logic "high" time of 500ns.

To facilitate some experimentation with clock duty cycle, we have provided an option to vary the duty cycle on this board. Remove **R2**, and install **R3**, **R5**, **R6**, and **R8** as shown. The duty cycle shaping is achieved by adjusting the DC level presented to the inverting input of the comparator inside the 10EL125. The input sinewave is still AC-coupled onto the V_{BB} DC level, but by adjusting the resistors **R5** and **R8** the duty cycle may be modified. Note that the duty cycle will be sensitive to the sinewave amplitude, so this circuitry is not suitable for production. Preferred methods for producing a shaped clock include dividing down a higher speed clock, using tapped LC delay lines, or even configuring a one-shot.

The evaluation board also includes an option for providing a TTL or CMOS clock directly to the board. To use a TTL clock, remove the four jumpers labeled **OPT1A**, **OPT1B**, **OPT1C**, and **OPT1D**. Insert a zero ohm jumper at the points labeled **OPT2A** and **OPT2B**. Next, install a 50Ω resistor at the point labeled **OPT2C**. The TTL clock driver will now drive a 50Ω termination, the ADC, and one additional TTL load for the output register clock driver.

Analog Input

The analog input to the board is an SMA jack terminated with 55Ω to ground. The input impedance of the ADC chip is 500Ω, so the nominal cable termination is 1((1/55)+(1/500)) or 49.5Ω. The nominal input range of the ADC is ±0.512 Volts.

Data and Clock Outputs

The CLC952 evaluation board is equipped with 74AS174 latches which latch the CLC952 output data and drive the Eurocard connector. An inverted version of the latch clock is also provided on the Eurocard connector. Use this clock (pin 20B) to register the data into your system. The output data format of the CLC952 is two's complement, so a negative full scale input (nominally -0.512V) will produce the output code 100000000000, while full scale (+0.512V) produces 011111111111. This data is available at the Eurocard connector on pins 18B – 8B and 7A. Note that the labels on the MSB for both the ADC and at the edge connector reflect the nominal inversion of the MSB.

In offset binary coding, the MSB has the same polarity as the other bits, so that negative full scale is all zeros and positive full scale is all ones. We have provided an inverter on the board to provide this output coding. If you would prefer to see the data in offset binary coding, simply use pins 18B – 7B.

Parts List, Schematic, and Artwork:

The following pages show the full schematic for the evaluation board, the parts list, and the artwork for the board. Note that all artwork is shown from the top view of the four layer board. All artwork is not shown actual size (the actual size of the board is 2.5" X 4").

Part Number	Reference Designation					Description
392034	Ul					MC10ELT25 Differential to TTL Translator, 8-Pin SOIC
392035	U2					74AS04 Hex Inv, 14-Pin SOIC
392036	U3	U4				74AS174 Hex D Flip-Flop, 16-Pin SOIC
322033	C4	C5	C6	C7	C8	0.1 UFD SMD Cap Size 1206
		C9	C10	C11	C12	C13
		C14	C15	C16	C17	C18
		C19	C20		C22	
322034	C1	C2	C3			2.2 UFD SMD Cap
CL952ACMSA	DUT					12-bit, 41MS/S ADC, 28-Pin SSOP
220012	J1					64-Pin RT Angle DIN Connector Male, Hirose #PCN10-64P-2.54DS (Digikey)
270002	Z1	Z2	Z3	Z4	Z5	Noise Suppression Filter, Murata
			Z8			#NFM41P11C204
353035	OPT1A	OPT1B	OPT1C	OPT1D	R2	0Ω SMD Resistor Size 1206
353050	R15					6.81K SMD Resistor Size 1206
353036	R4	R7	R12	R13	R14	49.9 SMD Resistor Size 1206
	R17	R18	R19	R20	R21	
	R22	R23	R24	R25	R26	
	R27	R28	R29			
353051	RI					54.9 SMD Resistor Size 1206
OPEN	R3	RS	R6	R8	OPT2A	(Do not place anything in these places)
				OPT2B	OPT2C	
353052	R16					3.24K SMD Resistor Size 1206
220014	CLK	IN				PCB Mountable SMA
220013						64-Pin Female DIN Connector, Hirose #PCN10C-64S-2.54DSA (Digikey)

Figure 2: Parts List

CLC952 Evaluation Board (P/N 730064)

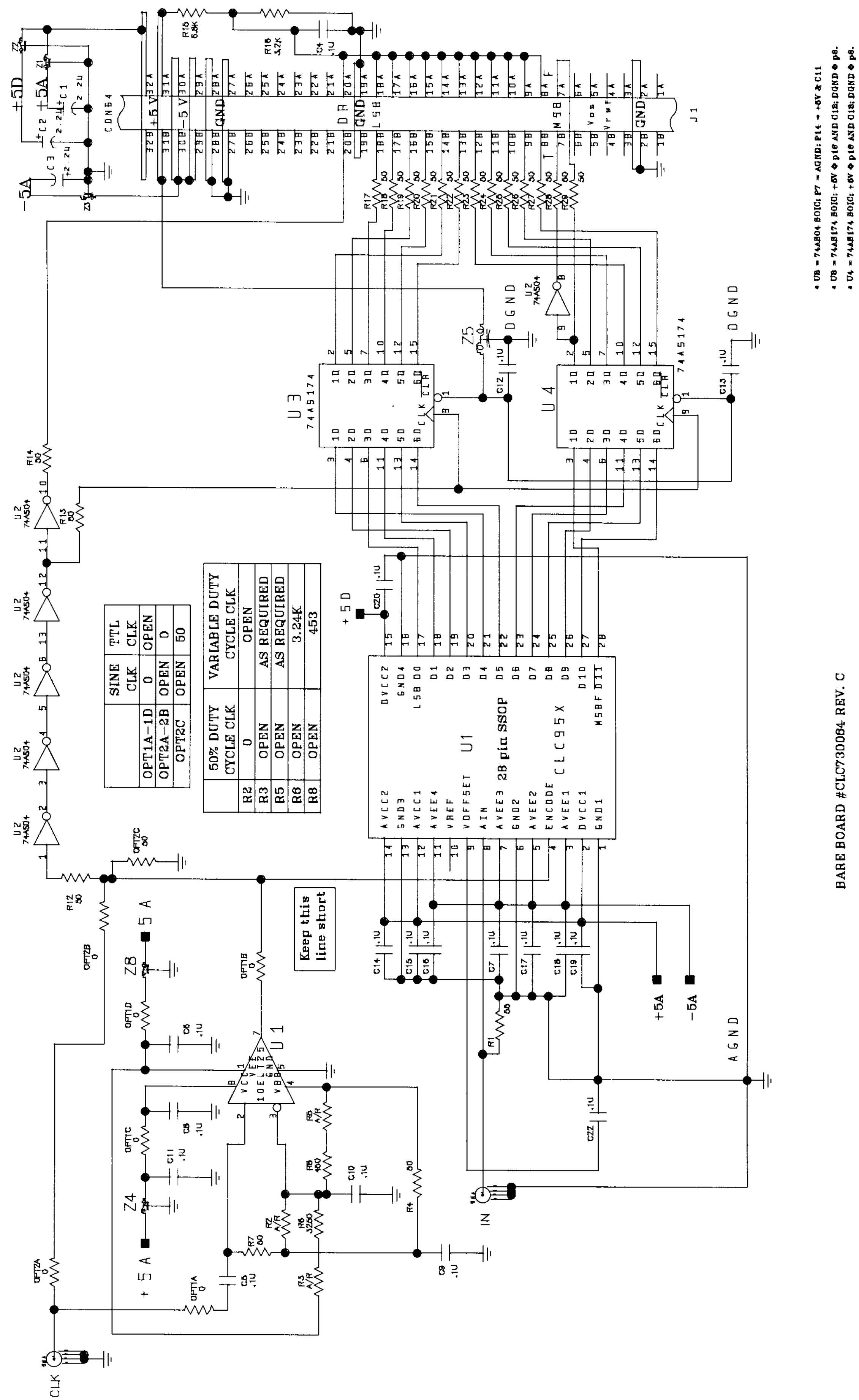

Figure 3: Evaluation Board Schematic

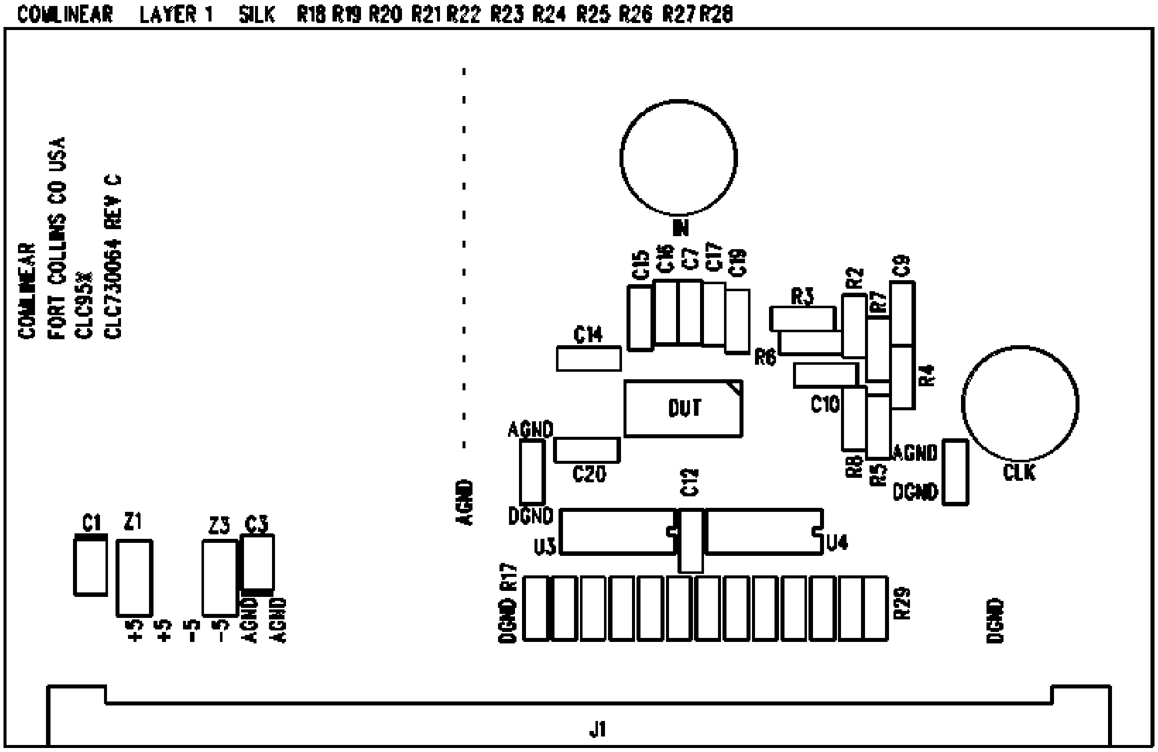

Figure 4: Top Layer Silk Screen

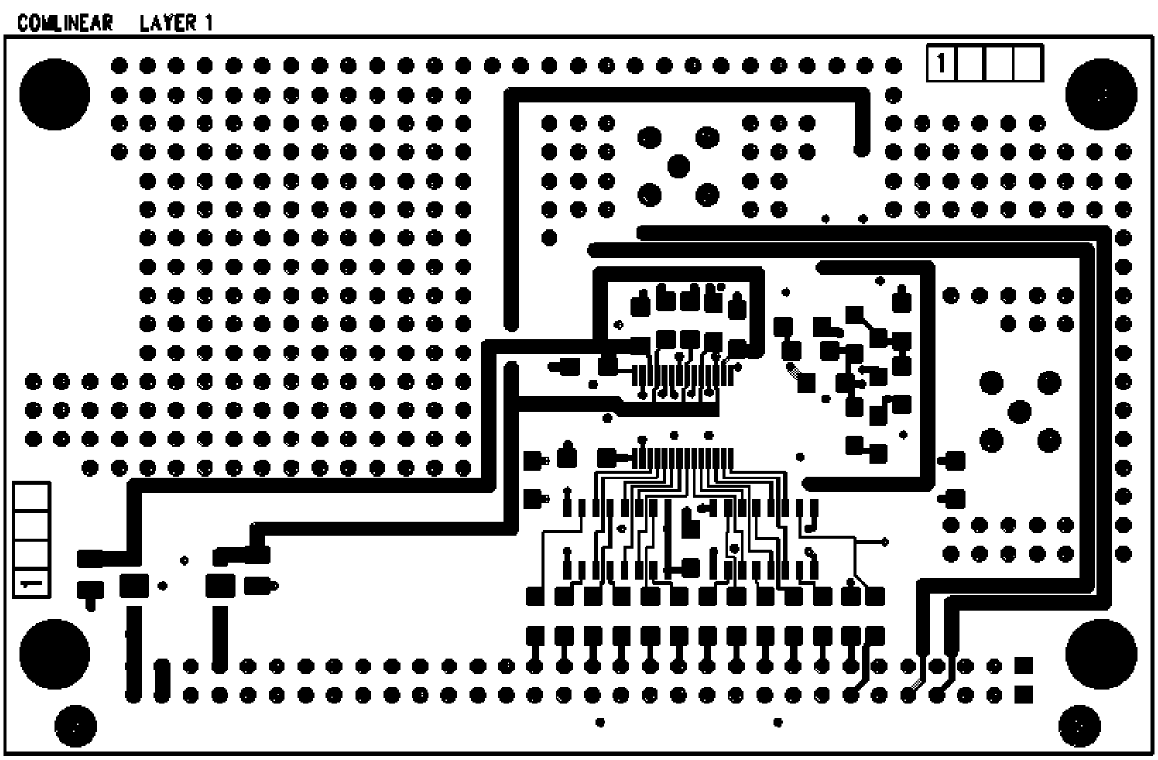

Figure 5: Layer 1 Copper (Positive)

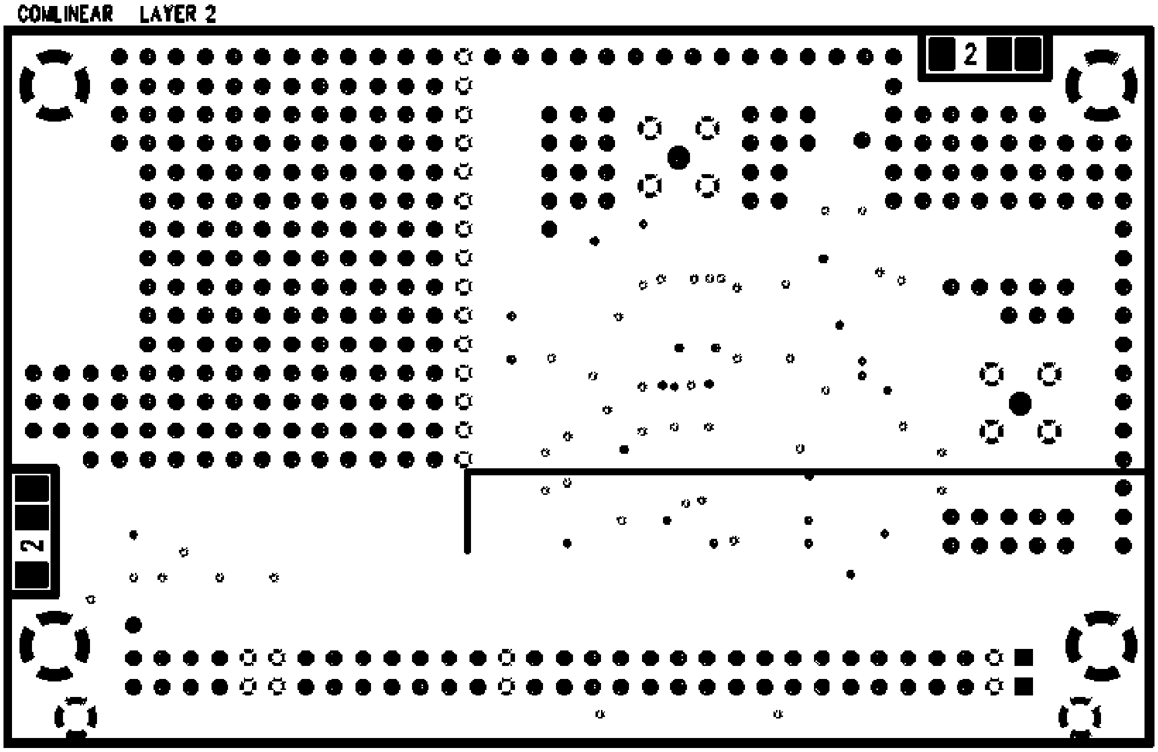

Figure 6: Layer 2 Copper Ground Plane (Negative)

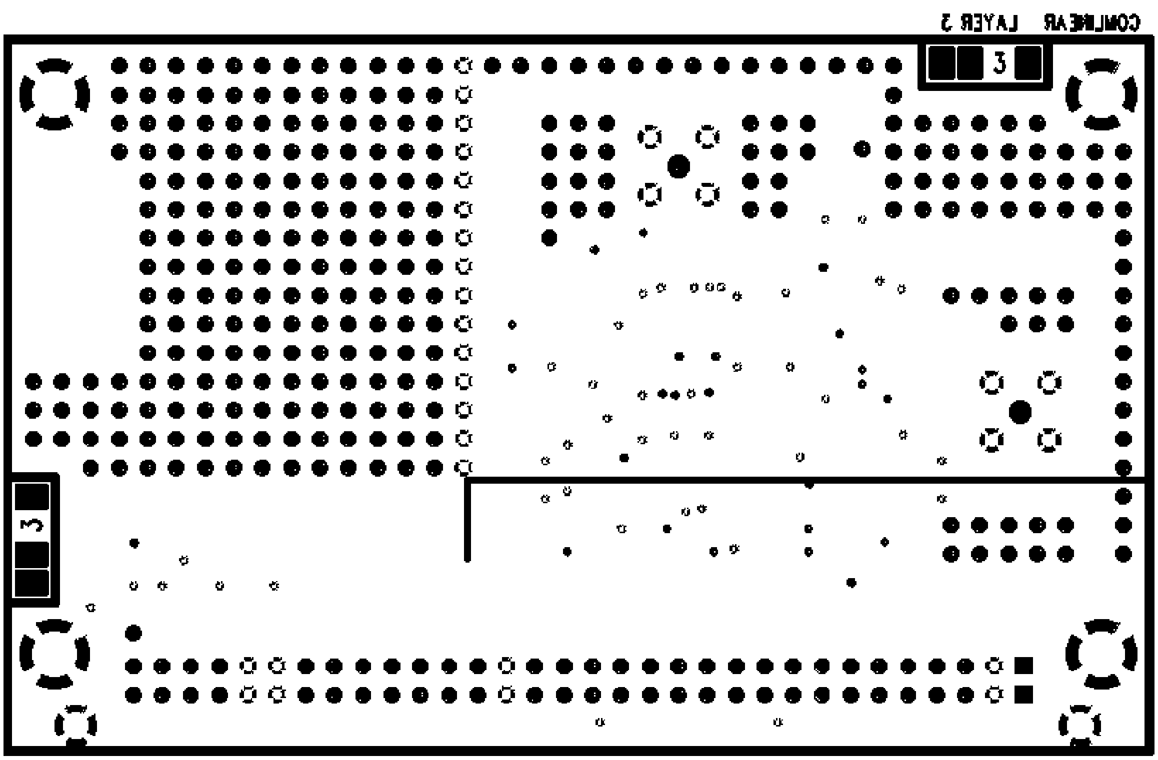

Figure 7: Layer 3 Copper Ground Plane (Negative)

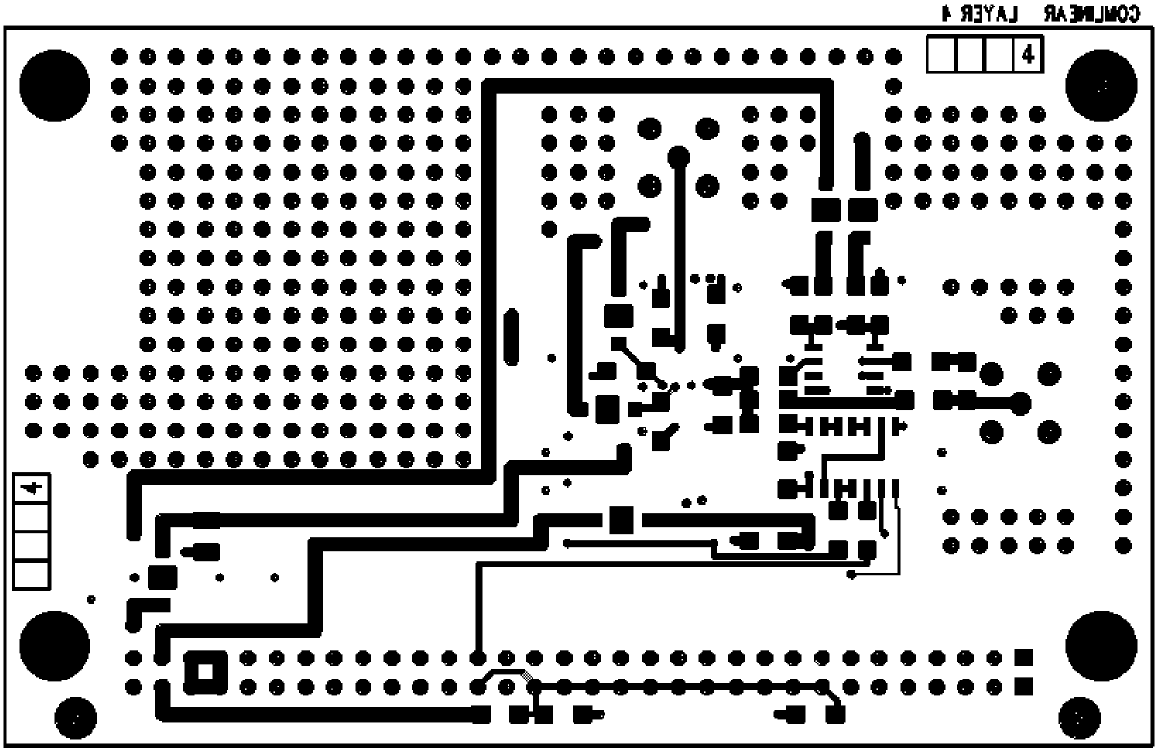

Figure 8: Layer 4 Copper (Positive)

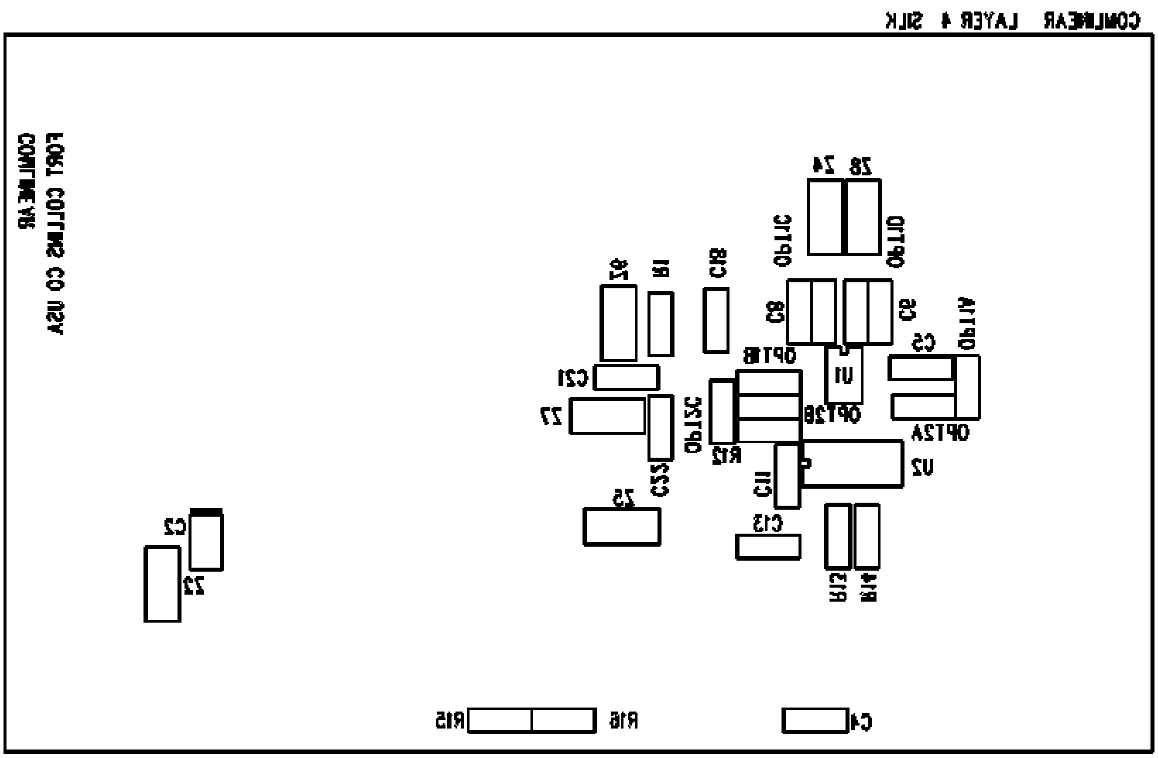

Figure 9: Layer 4 Silk Screen

Additional Information:
National has published three application notes which may help you in your evaluation of this ADC and with your system design as well. If you would like copies of these application notes, please call FaxCOM at **1-800-970-0102**. The FaxCOM service is an automated fax-on-demand service. International callers in Germany, France, Italy and the United Kingdom please dial **1-516-227-1310**. If you would like a printed copy of the applications notes or if you have any other questions about the ADC converter, please call the National Customer Response Group at **1-800-272-9959**. These documents are also available on the World Wide Web at **http://www.national.com**.

Application Note AD-01
FaxCOM #158
National Literature #350001-001
Designing with High-Speed Analog to Digital Converters
An overview of system design considerations, board layout, specifications, and interfacing techniques.

Application Note AD-02
FaxCOM #159
National Literature #350002-001
High Performance ADCs Require Dynamic Testing
A detailed look at the design and characterization of high speed ADCs.

Application Note AD-03
FaxCOM #201
National Literature #350003-001
Effects of Aperture Time and Jitter in a Sampled Data System
Definition of terms, mathematical framework, and prediction of errors resulting from sampling a signal.

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