

**Description**

The Comlinear E949PCASM Evaluation board is designed to support simple and effective evaluation of the CLC949 Analog-to-Digital Converter. To operate the converter you need only supply power, a clock and a signal to be digitized. The evaluation board uses a common Eurocard connector to make the power, ground and data connections with the rest of the evaluation system. Options exist on the board to use an amplifier based input to the converter, a transformer coupled input, or direct input, as well as options to generate a clock from a sinusoidal source or to use a suitable CMOS clock. The bias points for the converter can be selected via a DIP switch. For a complete description of these various options, please refer to the CLC949 datasheet.

**Default Configuration**

The CLC949 Evaluation board is shipped configured for options 2 and 4 (DC coupled input using amplifiers, CMOS clock generator enabled). The output data format is offset binary and the bias point is selected to be 200 $\mu$ A, allowing 20MHz operation.

**Clock Generation**

The evaluation circuitry includes a clock generation circuit that will convert a sinusoidal input to a CMOS clock for use by the CLC949. When using this option, the clock signal that is provided should be 2-3V<sub>pp</sub> (10-14dBm). For best results when digitizing high speed input signals, the converter must have a very low jitter clock. To generate this the sinusoidal input must have very low phase noise. In a laboratory environment, Comlinear suggests the use of a low phase noise synthesizer such as the HP8662 or the HP8643 as a clock source.

There is also an option that will enable you to provide a TTL or CMOS clock directly to the board. The clock is provided through an SMA connector, regardless of the clocking option chosen. To enable the input of a digital clock, remove the three jumpers labeled **OPT4** and insert a jumper at the point labeled **OPT1-3**. These jumpers can be found on the opposite side of the board to the CLC949 and a surface mount 0 $\Omega$  resistors.

**Analog Input Conditioning**

The CLC949 requires a differential input signal, centered around a bias point of approximately 2.25V. The evaluation board offers three options for providing this input:

- Option 1 uses a transformer to phase split the input signal and to provide the appropriate offset voltage. This option will result in the lowest distortion signal for input frequencies of 1MHz or higher. Since the transformer is not able to pass frequencies lower than about 50kHz, this option is not a good choice if your signal must be DC coupled. If you want to use this option, install the transformer and the two jumpers labeled **OPT1**, and remove the three jumpers labeled **OPT2**. All of these jumpers can be found on the back side of the board. The transformer shipped with the board is a 1:1 transformer, therefore the input to it should be 2V<sub>pp</sub> in order to obtain a full scale output.
- Option 2 uses an amplifier based circuit to perform the phase splitting and DC offset. This circuit is described in more detail in the CLC949 datasheet. Option 2 is the default condition in which the board is shipped. Using this option, a 2V<sub>pp</sub> signal, with no DC offset is applied to the input SMA to obtain a full scale output.
- Option 3 requires that you provide a differential input signal with the proper offsets to the SMA connectors labeled **+VIN** and **-VIN**. To enable this option, remove the three jumpers labeled **OPT2** and install the jumpers labeled **OPT3**.

**DATA and Clock Outputs**

The CLC949 Evaluation board is equipped with 74F574 latched which latch the CLC949 output data and drive the Eurocard connector. An inverted version of the A/D clock is also provided on the Eurocard connector. The output data format of the CLC949 is selectable between Offset Binary or Twos Complement via the Jumper **OPT6**. For Offset binary operation install the jumper in the location **OPT6A**, two's complement is achieved by use of **OPT6B**. These jumpers can be found on the front of the board, just above the CLC949 chip.

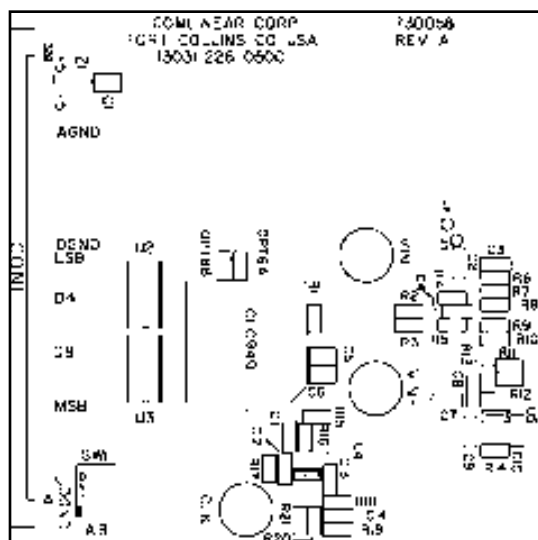
## Bias Control

The CLC949 offers you the ability to make a tradeoff between dynamic performance and power dissipation. This can be done by selecting one of three discrete bias points with the DIP switch on the board, or by selecting Option 5 which allows analog control of the bias current through the selection of R23. The bias point can be selected according to the following table:

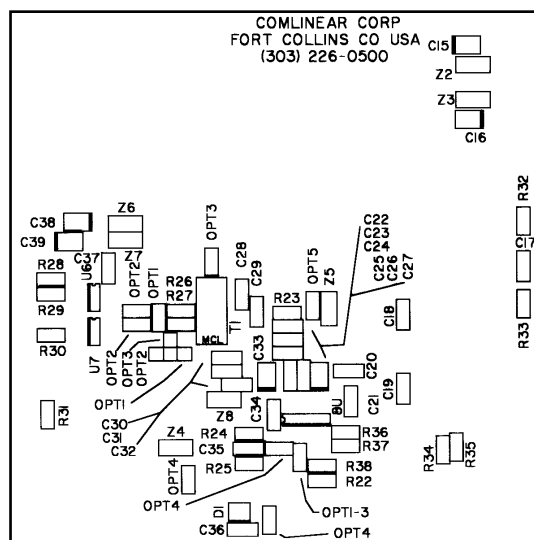
| SW1A | SW1B | Bias Point   |
|------|------|--------------|
| ON   | ON   | Low Bias     |
| OFF  | OFF  | Medium Bias  |
| ON   | OFF  | High Bias    |
| OFF  | ON   | Set with R23 |

If you select Option 5, you must install the jumper labeled **OPT5**. Please refer to the CLC949 datasheet for assistance in selecting an appropriate value for R23.

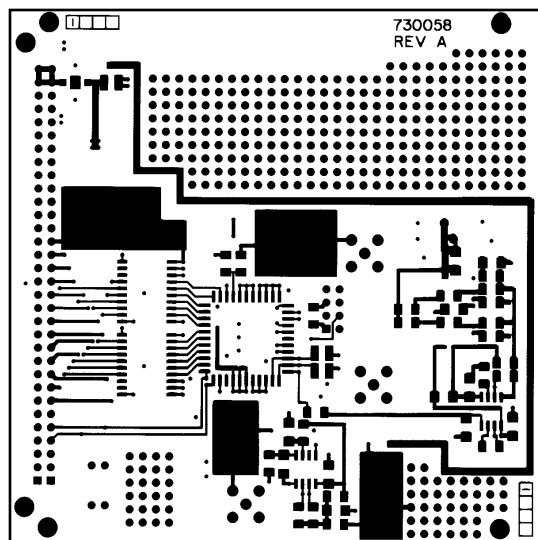
Top (Silk)



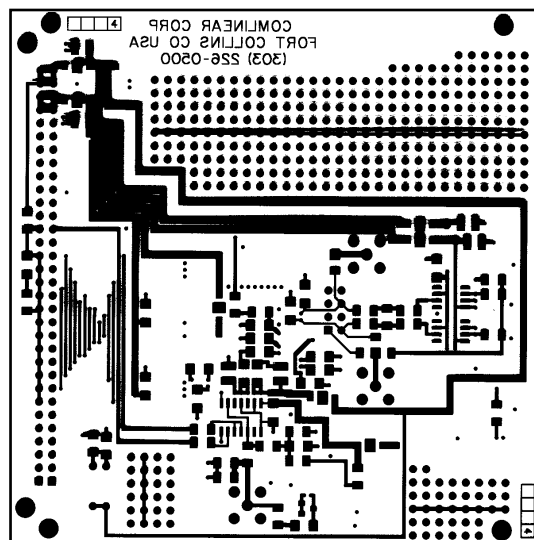
Bottom (Silk)



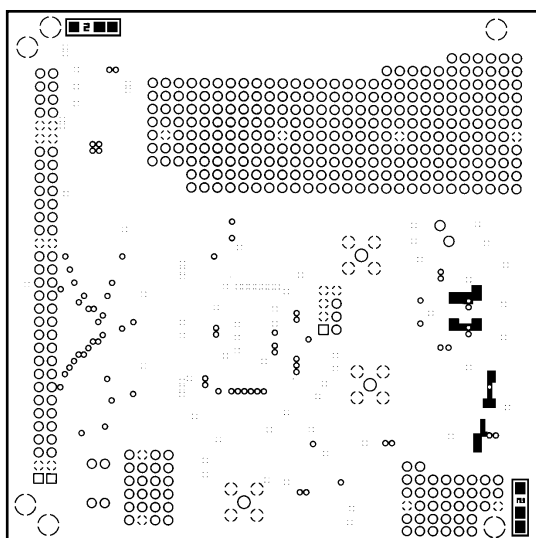
Top (Metal)



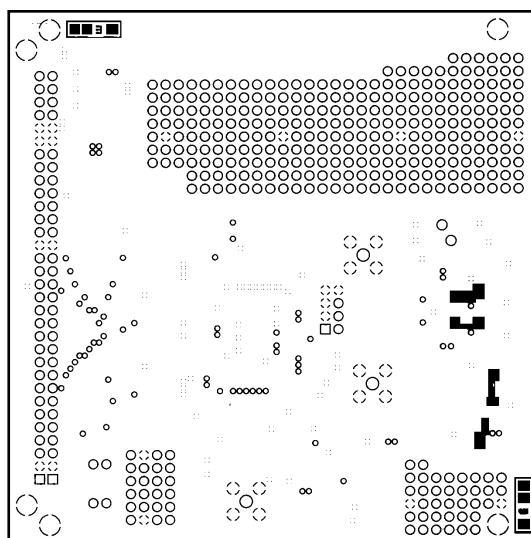
Bottom (Metal)



**Layer 2 (Negative)**



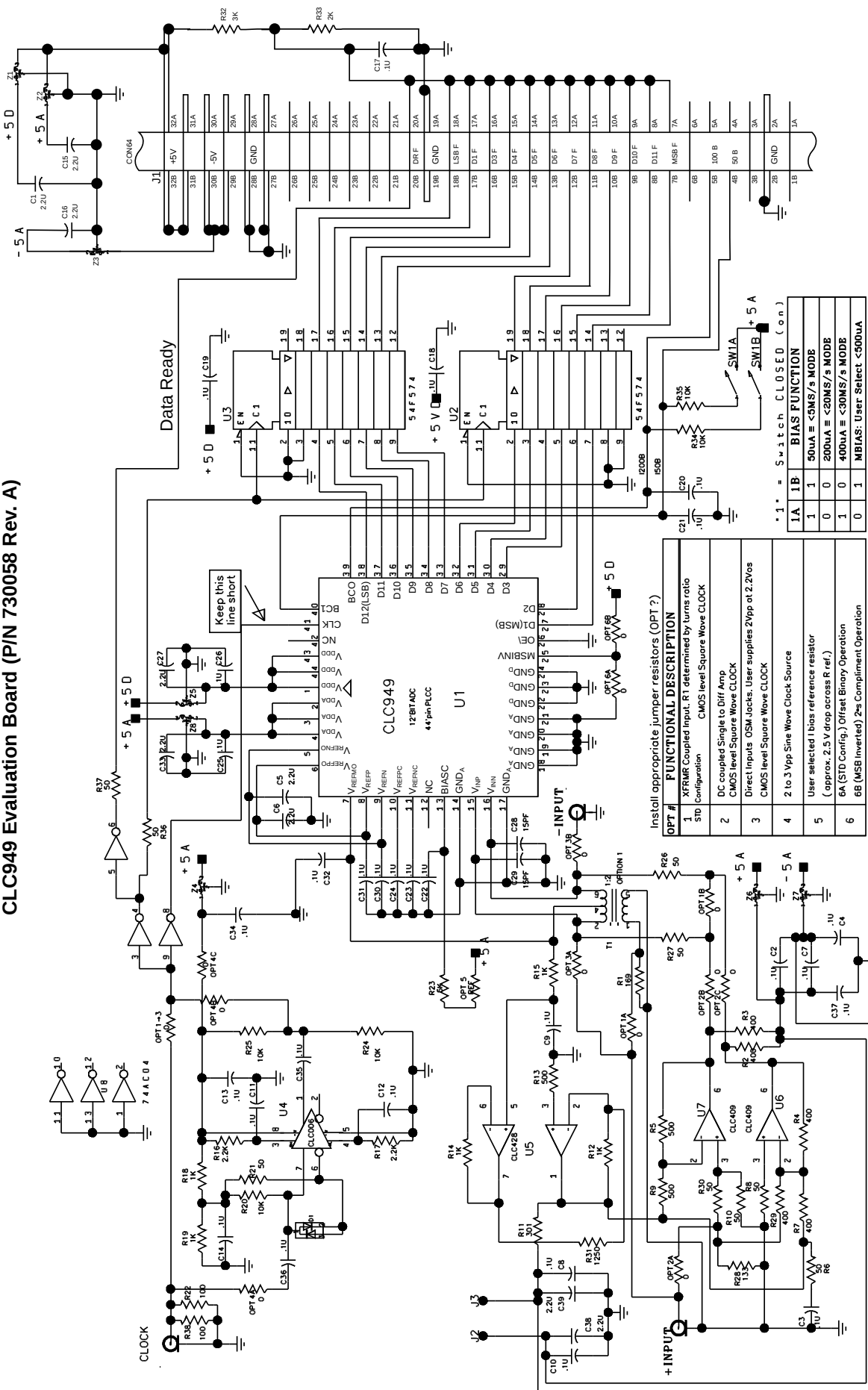
**Layer 3 (Negative)**



## PIN DESCRIPTIONS

| PIN# | Function | PIN# | Function | PIN# | Function | PIN# | Function  |
|------|----------|------|----------|------|----------|------|-----------|
| A1   | NC       | B1   | NC       | A17  | 2V BIAS  | B17  | D11       |
| A2   | GND      | B2   | GND      | A18  | 2V BIAS  | B18  | D12 (LSB) |
| A3   | NC       | B3   | NC       | A19  | GND      | B19  | GND       |
| A4   | NC       | B4   | BC1 (IN) | A20  | 2V BIAS  | B20  | DR        |
| A5   | NC       | B5   | BC0 (IN) | A21  | NC       | B21  | NC        |
| A6   | NC       | B6   | NC       | A22  | NC       | B22  | NC        |
| A7   | 2V BIAS  | B7   | D1 (MSB) | A23  | NC       | B23  | NC        |
| A8   | 2V BIAS  | B8   | D2       | A24  | NC       | B24  | NC        |
| A9   | 2V BIAS  | B9   | D3       | A25  | NC       | B25  | NC        |
| A10  | 2V BIAS  | B10  | D4       | A26  | NC       | B26  | NC        |
| A11  | 2V BIAS  | B11  | D5       | A27  | GND      | B27  | GND       |
| A12  | 2V BIAS  | B12  | D6       | A28  | GND      | B28  | GND       |
| A13  | 2V BIAS  | B13  | D7       | A29  | -5V (IN) | B29  | -5V (IN)  |
| A14  | 2V BIAS  | B14  | D8       | A30  | -5V (IN) | B30  | -5V (IN)  |
| A15  | 2V BIAS  | B15  | D9       | A31  | +5V (IN) | B31  | +5V (IN)  |
| A16  | 2V BIAS  | B16  | D10)     | A32  | +5V (IN) | B32  | +5V (IN)  |

# CLC949 Evaluation Board (P/N 730058 Rev. A)



\*1\* = Switch CLOSED (on)

| 1A | 1B | BIAS FUNCTION             |
|----|----|---------------------------|
| 1  | 1  | 50uA = <3MS/s MODE        |
| 0  | 0  | 200uA = <20MS/s MODE      |
| 1  | 0  | 400uA = <30MS/s MODE      |
| 0  | 1  | MBIAS: User Select <500uA |

Install appropriate jumper resistors (OPT ?)

| OPT # | FUNCTIONAL DESCRIPTION                                                     |
|-------|----------------------------------------------------------------------------|
| 1     | XFRMR Coupled Input, R1 determined by turns ratio                          |
| 2     | STD Configuration CMOS level Square Wave CLOCK                             |
| 3     | DC coupled Single to Diff Amp CMOS level Square Wave CLOCK                 |
| 4     | Direct Inputs OSM Jacks, User supplies 2Vpp at 2.2Vos                      |
| 5     | CMOS level Square Wave CLOCK                                               |
| 6     | 2 to 3Vpp Sine Wave Clock Source                                           |
| 7     | User selected 1 bias reference resistor (approx. 2.5 V drop across R ref.) |
| 8     | 6A (STD Config.) Offset Binary Operation                                   |
| 9     | 6B (MSB Inverted) 2m Complement Operation                                  |

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