

Part Number E935PCASM

August 1996

#### Description

The CLC935 evaluation board has been designed as an effective evaluation platform for the CLC935 (12-bit, 15MSPS) analog-to-digital converter. Connections are made using a standard Eurocard connector for digital and power signals, and standard SMA connectors for the sensitive conversion clock and analog signals.

The board is available blank (part number 730025) and fully assembled (part number E935PCASM). The E935PCASM includes a socket for the CLC935, but does not include the CLC935.

#### **Power and Ground**

Power supply and ground connections to the Eurocard connector should be kept as short as possible to minimize power supply resonances. Additionally, switching power supplies are strongly discouraged for applications requiring maximum performance.

The converters digital and analog grounds are connected via the analog ground plane. The DATA READY and D, D14 output drivers have a separate digital ground plane and -5.2V power feed. The two "GND" jumpers can be used to connect the converter and digital ground planes together (the E935PCASM is configured with both ground planes connected via the "GND" jumpers). This arrangement should facilitate ground-loop creation or elimination, as required, to minimize digital system noise corruption of the converter and any associated analog circuitry. Digital ground is available through the Eurocard connector at pins 2A/B and 19A/B. Analog ground in available through the Eurocard connector at pins 27A/B and 28A/B.

### Analog Input

The ANALOG INPUT is provided through the SMA connector J1. The E935PCASM employs a  $50\Omega$  input termination resistor. Values larger than  $200\Omega$  are not recommended unless driven by a low-impedance analog input source. Often in evaluating converters, the ANALOG INPUT is driven by a single-tone source. It should be noted that any jitter present in this source will undermine the apparent quality of the conversion process, specifically SNR (signal-to-noise ratio). То avoid this situation, a over flow noise (low jitter) signal source should be used to provide the ANALOG INPUT signal. Bandpass filtering will likely be required given the generally high harmonic content of very-low noise signal sources.

## **CONVERT Clock Source**

The evaluation board employs an ac-coupled sine-to-ECL converter. The input can come from either the Eurocard connector or the SMA connector J2. In normal operation, the circuit will function very well with a  $2V_{pp}$  input signal. To maintain the specified SNR performance, a very-low phase noise (low jitter) signal source is absolutely essential in providing the CONVERT signal. Bandpass filtered crystal oscillators or low phase noise synthesizers such as the HP8662 or Fluke T6160B are suitable choices.

The CONVERT clock can be supplied through the Eurocard connector at pins 1 A,B. U6 can be left incircuit if buffering of the CONVERT signal is desired. Some "patch" wiring will be required to provide adequate termination of the Eurocard derived signals. It should be noted that the converter references the CONVERT input to analog ground. Please refer to the schematic on the following pages.

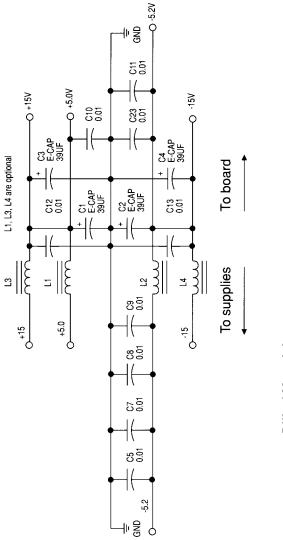
#### Outputs

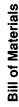
The CLC935 converters employ "constant current" ECL compatible outputs. This unique design minimizes noise inside the hybrid, but requires buffering, preferably near the converter. The evaluation board employs MC100E151 hex latches to perform this function.

Although no termination resistors are needed for the CLC935, the MC100E151's, however, do require standard ECL terminations. Having been setup as differential outputs through the Eurocard connector, it is expected that the user will provide suitable ECL terminations on the receiving side of the evaluation board connector. Simple 390W pull-down resistors to -5.2V have proven effective given the speed range of the CLC935 converter.

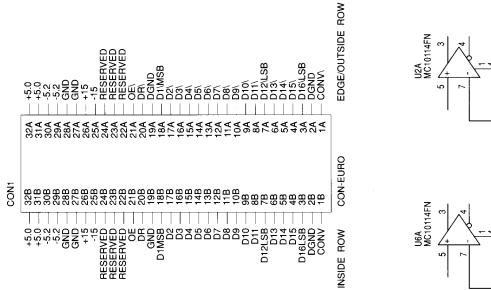
The DATA READY signal is also available from the Eurocard connector. This signal is derived in such a way as to minimize any loading or distortion effects on the CONVERT signal used for the converter itself. The DATA READY signal is also used to clock the output latches U3 to U5, and has been terminated on board. If desired, the DATA READY termination can be relocated to a more appropriate position in the evaluation system.

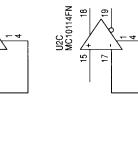
The output coding of the converter is controlled through two jumpers. The MSB and MSB jumper determines which of the converter's MSB outputs is presented to the latches, while JPI controls the inversion of the LSB's (D2 to D12). The E935PCASM comes configured for binary output with the MSB jumper installed. Please refer to the CLC935 data sheet for more details on output coding.



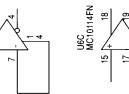


Quan.	Referency	Part
<del>~</del>	CON1	Eurocard Connector Male- Winchester 64P-6033-0431-0; Matching Female - Winchester
4	C1,C2,C3,C4	045-0000-0422-01. 39µF Tantalum (Sprague 150D series or equivalent)
19	C5,C6,C7,C8,C9,C10, C11,C12,C13,C14,C15, C16,C17,C18,C19,C20, C216,C23	0.01μF, Style 1206
4 N	JP1,JP2,JP3,JP4 J1,J2	JUMPER SMA, Amphenol 901-144 or
444	L1,L2,L3,L4 R1,R7,R9,R10 R2,R3,R11,R12	Phillips, VK-200-19 50Ω, Style 1206 270Ω, Style 1206
4 0 <del>-</del> 0	R4,R5,R13,R14 R6,R8 U1 U2.U6	182Ω, Style 1206 1.5kΩ, Style 1206 CLC935/6/7 MC10114FN
∞ <i>α</i> –	U3,U4,U5 Socket Strip PCB	MC100E151FN Samantec SL-120-T-30 730025

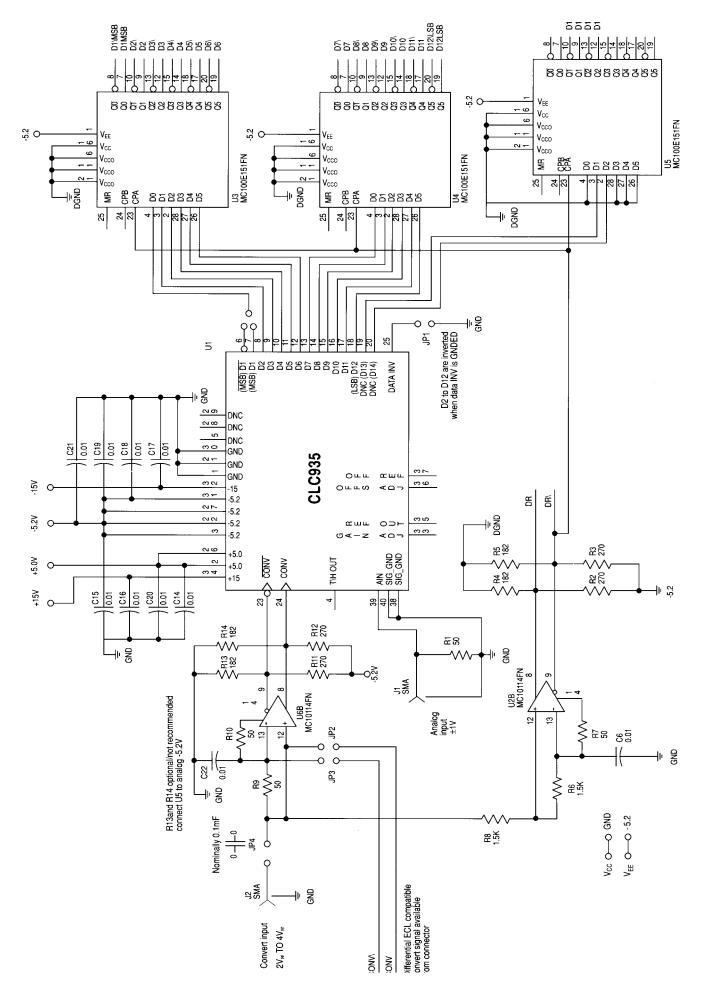




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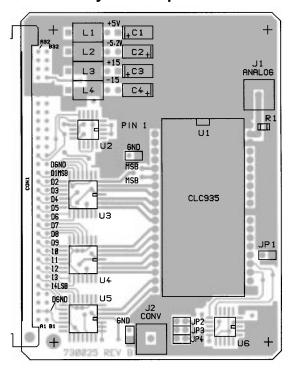






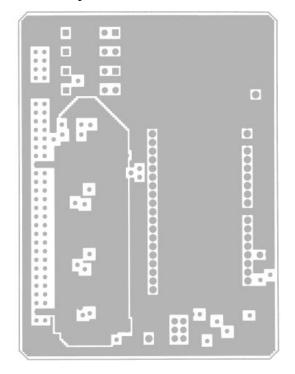
# Layout Information

The four layers which makeup the CLC935 evaluation board are detailed below. The top and bottom layers also include silk-screen data indicating component placement. All reductions are TOP VIEW. Actual board dimensions are 4.00"x3.00". The bare printed circuit board is available from National Semiconductor as part number 730025.

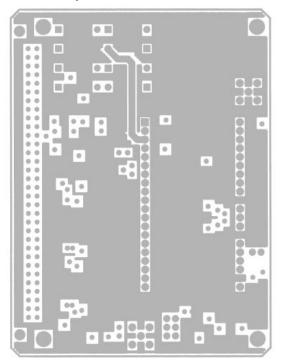


Layer 1 - Top Metal

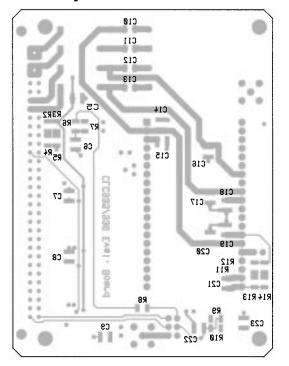
Layer 2 - Ground Plane



Layer 3 - Power Plane



Layer 4 - Bottom Metal



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