

# **Quad Op Amp Evaluation Boards**

Part Number CLC730024, CLC730031

August 1997

The CLC730024 is an evaluation board intended for the evaluation of quad Op-Amps in the DIP package. The CLC730031 is a similar board, but laid out for an SOIC package.

To obtain optimum performance from a high speed device, a good Printed Circuit Board (PCB) layout is essential. The importance of the layout becomes greater as the frequency of operation increases. Some of National Semiconductor's quad Op-Amps have bandwidths in excess of 100MHZ, therefore it is vital that sound PCB layout techniques be used when designing with these devices. The CLC730024 and CLC730031 are examples of good PCB layouts which designers are encouraged to copy.

To minimize capacitive feedthrough and noise, if there are op-amps not being used, they should be configured as unity gain buffers (with a resistor in the feedback path for current feedback devices) and the non-inverting inputs connected to GND. On devices that are being used, the ground plane should be removed from beneath the feedback and gain setting resistors, to minimize parasitic capacitance on sensitive nodes. Input and output traces should be laid out as transmission lines with the appropriate termination resistors very near the device. On a 0.0065" (FR4 or equivalent) a 0.1" wide trace over ground plane on the opposite side of the board will exhibit a characteristic impedance of  $50\Omega$ .

Parasitic or load capacitance directly on the output of an amplifier will introduce additional phase shift in the device. If excessive, this phase shift can lead to peaking in the frequency response or, in extreme cases, oscillation. A small series resistor in series with a capacitive load effectively decouples it from the buffer output and removes the undesirable effects of excess phase shift. Further detail on the selection of these resistors can be found in the individual amplifier data sheets.

#### **Parts List**

 $\begin{array}{lll} R_{IN1},\,R_{IN2},\,R_{IN3},\,R_{IN4}, & \text{select for desired input resistance} \\ R_{OUT1},R_{OUT2},R_{OUT3},\,R_{OUT4} & \text{select for desired output resistance} \\ R_{F1},R_{F2},R_{F3},R_{F4} & \text{select according to data sheet and application} \\ R_{G1},R_{G2},R_{G3},R_{G4} & \text{select according to data sheet and application} \\ C_{1},C_{2} & 0.1\mu\text{F capacitor} \\ C_{3},C_{4} & 6.8\mu\text{F capacitor} \\ L_{1},L_{2} & \text{Optional ferrite bead inductors} \end{array}$ 

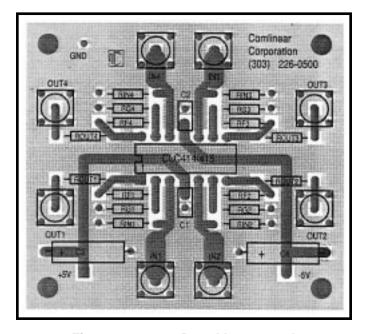


Figure 1: 730024 Board Layout and Component Placement

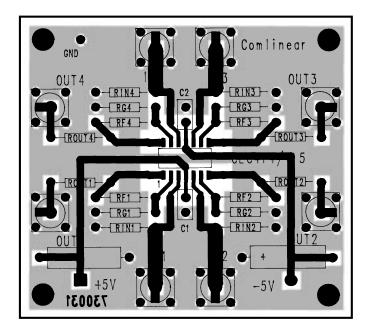


Figure 2: 730031 Board Layout and Component Placement

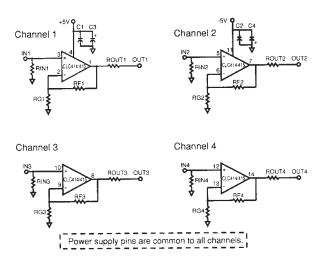


Figure 3: Evaluation Board Schematic

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#### National Semiconductor Corporation 1111 West Bardin Road

Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

#### National Semiconductor Europe

Fax: (+49) 0-180-530 85 86 E-mail: europe.support.nsc.com Deutsch Tel: (+49) 0-180-530 85 85 English Tel: (+49) 0-180-532 78 32

Francais Tel: (+49) 0-180-532 93 58 Italiano Tel: (+49) 0-180-534 16 80

#### National Semiconductor Hong Kong Ltd.

13th Floor, Straight Block Ocean Centre, 5 Canton Road Tsimshatsui, Kowloon Hong Kong

Tel: (852) 2737-1600 Fax: (852) 2736-9960

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