National Semiconductor

CLC561 Evaluation Board

Part Number CLC730019

August 1996

The CLC730019 PCB from National Semiconductor is intended to allow the easy evaluation of the CLC561. This hybrid DriveR amplifier is primarily intended to drive high signal levels into a matched load with excellent distortion and full power bandwidth capabilities. The CLC561 is optimized for the highest slew rate, and hence full power bandwidth, with some sacrifice in the long term pulse settling accuracy.

Figure 1 shows the circuit implemented by the board. Refer to the individual amplifier data sheets for a detailed description of operation. Briefly, however, the DriveR amp topology achieves an equivalent output impedance without the need for a discrete matching resistor in series with the output. The CLC561 is primarily intended for non- inverting applications with the input impedance set by R_{in}. R_f primarily determines the output impedance while R_g, having set a particular R_f, will set the no load gain. The actual voltage gain to the load must also include any voltage divider effect from the output impedance to the load. Figure 2 summarizes the design equations for achieving a desired output impedance and gain. Note that an external compensation capacitance, C_x, must be included for flat frequency response. The equation shown assumes a load matched to the output impedance.

Several optional features are included in the schematic of Figure 1. First, since reversed supplies will destroy the CLC561 amplifier, a provision for series diodes (type 1 N 4002 or equivalent.) has been provided on the board. If Dl and D2 are inserted into the board, the power supply traces in parallel should be cut. Dropping the power supply voltage through these diodes will slightly decrease the full scale output voltage swing and worsen the 2nd harmonic distortion by about ldB.

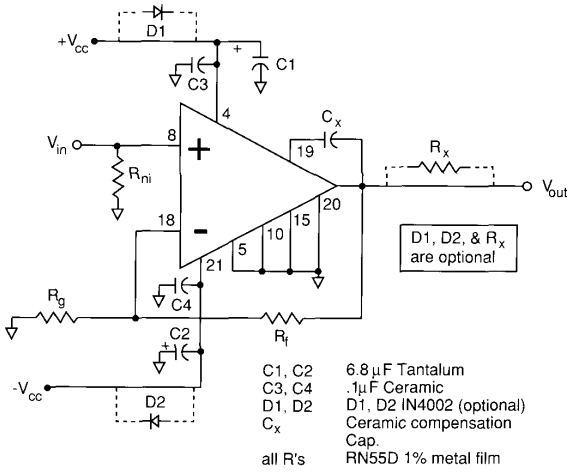

Figure 1

Second, it is sometimes advantageous to implement a portion of the desired output impedance with a discrete series resistor in the output, R_x. Inserting an R_x, into the board will require the output trace on the opposite side of the board from R_x to be cut. Using R_x. will decrease the achievable swing at the load, but will improve the output VSWR as shown in the data sheet plots and help protect the part from output short circuit damage.

Summary Design Equations and Definitions

$$R_f = (G + 1)R_o - A_v R_i$$

R_f - Feedback resistor from output to inverting input

$$R_g = \frac{R_f - R_o}{A_v - 1}$$

R_g - Gain setting resistor from inverting input to ground

$$C_x = \frac{1}{\frac{R_o}{300\left(1 - \frac{2}{R_g}\right)}} - .08$$

C_x - External compensation capacitor from output to pin 19 (in pF)

Where:

R_o - Desired equivalent output impedance

A_v - Non-inverting input to output voltage gain with no load

G - Internal current gain from inverting input to output = 10 ± 1%

R_i - Internal inverting input impedance = 14Ω ± 5%

Figure 2

The evaluation board has been layed out with careful attention to frequency response, distortion characteristics, and thermal management (see Figure 3, 4, and 5) Specially, a continuous ground plane beneath the part has been maintained to allow the use of thermally conductive pad beneath the part as described in the device data sheets. Using this pad to conduct heat into the board, greatly decreases the case temperature in operation. Also, the lAF supply decoupling capacitors have been carefully placed to achieve a very symmetric ground return path (through the ground plane under the part) to the output load. This is very critical to achieving the specified 2nd harmonic distortion. Finally, the compensation capacitor has been placed to achieve the broadest bandwidth capability for a single sided component loading scheme.

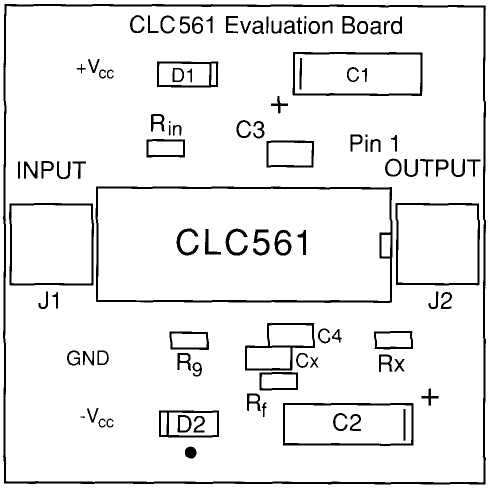

Figure 3: Top side component placement silkscreen J1, J2 - SMA connector Amphenol 901-144 (straight) or Amphenol 901-143 (right angled)

The CLC561 can be socketed using Cambion flush mount connection jacks: P/N 450-2548.

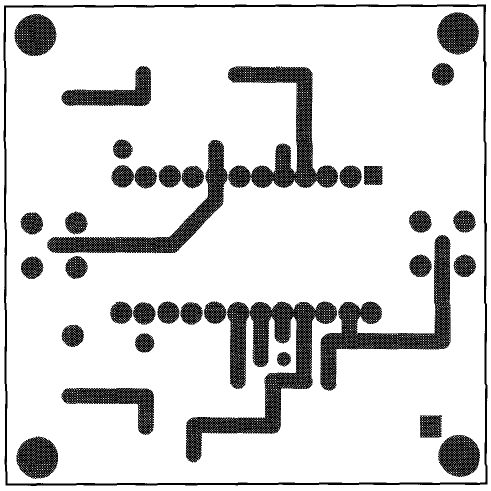

Figure 4: Botom side metal (viewed from top)

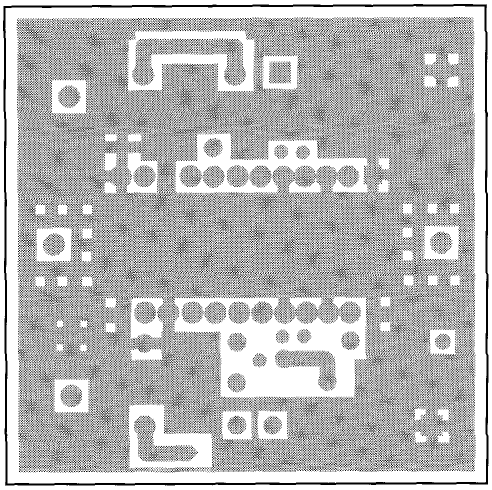

Figure 5: Top side metal

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