

The CLC533 is a high-speed 4:1 multiplexer with buffered inputs and outputs. This monolithic device has been designed using an advanced complimentary bipolar process. The CLC533 evaluation boards (two versions) have been designed as evaluation platforms for CLC533AJP (DIP package) and the CLC533AJE (SOIC package). The part number for the evaluation board supporting the DIP package is 730035, and that for the board supporting the SOIC is 730039.

Figure 1 shows the schematic of the circuit employed on the boards. For a detailed description of device performance please refer to the individual detail data sheet.

The evaluation board has been designed and layed out in a manner to maximize the isolation between the input channels. The steps that have been taken to aid in this include: separation of the inputs as much as is practical, strips of ground plane separating the input traces and the use of termination resistors that have been physically isolated from one another. A strip of ground plane has been placed between the two rows of pins to minimize the interference between the inputs and the outputs of the device.

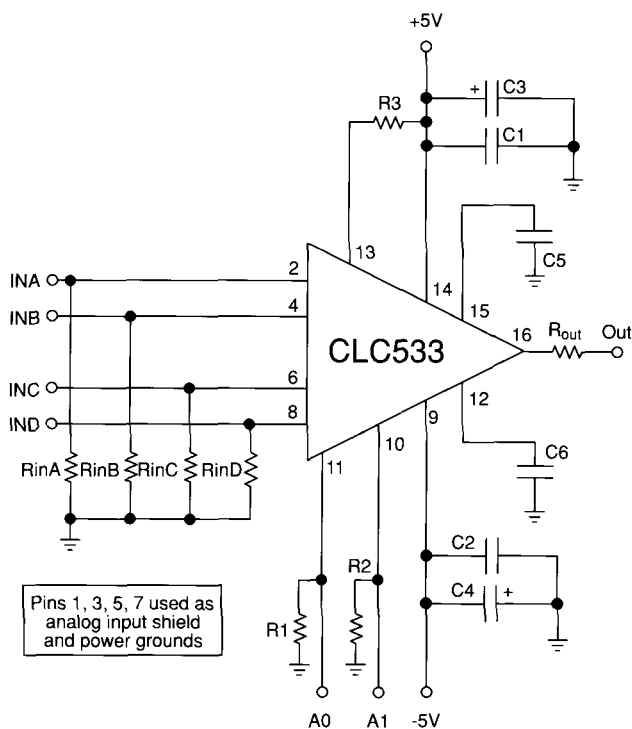


Figure 1: Schematic of CLC533 Evaluation Board

Digital Interface and Channel SELECT

The CLC533 functions with TTL, CMOS and ECL logic families. The D_{REF} pin determines logic compatibility. With D_{REF} left open (R_3 not inserted in board) A_0 and A_1 will respond to ECL level inputs. R_1 and R_2 can be used to set input termination networks as required by the driving gate logic family. If D_{REF} is tied to +5V through R_3 (approximately 1k Ω), then the select inputs will respond to TTL or CMOS input levels. Note that D_{REF} is internally isolated by a 2300 Ω resistor. R_1 and R_2 should be left open in TTL or CMOS mode.

Input Signal Termination

The analog inputs to the board are brought in through four SMA connectors. The input signals are terminated with R_{inA} , R_{inB} , R_{inC} , and R_{inD} , these resistors should be chosen to match the transmission line impedance of the cable bringing the signals to the board, typically 50 Ω or 75 Ω .

Power Supplies

The CLC533 operates off of two power supplies, nominally +5V and -5V. Use of an ECL -5.2V supply rather than the -5V supply is allowed/recommended for ECL. The supplies used should be capable of providing 100mA of current each.

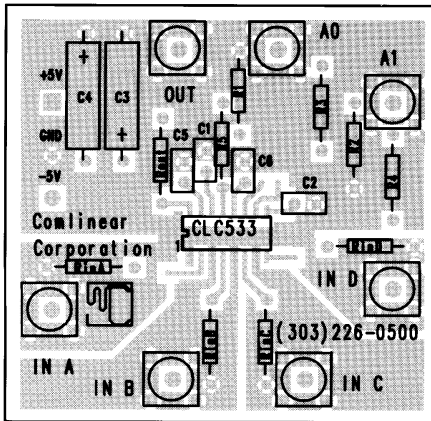


Figure 2: Top layer metal - circuit side (top view)
730039 SOIC version

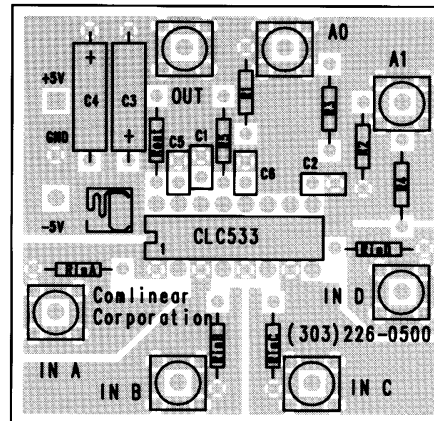


Figure 4: Top layer metal - circuit side (top view)
730035 DIP version

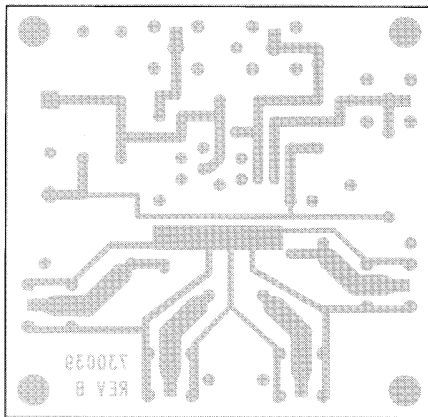


Figure 3: Bottom layer metal (top view)
730039 SOIC version

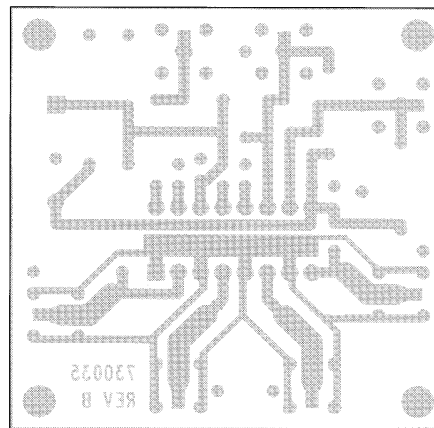


Figure 5: Bottom layer metal - (top view)
730035 DIP version

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