National Semiconductor

CLC532 Evaluation Board

Part Number CLC730028

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The 730028 (Rev. B) evaluation board is designed to aid in the evaluation and characterization of the CLC532, 2:1 analog multiplexer. Designed for very wide dynamic range systems, the CLC532 provides a wideband, unity gain, two-channel multiplexer with exceptional switching speeds. High channel isolation and fast pulse settling, make the CLC532 ideal for 12-bit ADC input-multiplexing applications. The CLC532 data sheet provides more detailed performance and applications information.

Basic Operation

The complete circuit schematic of the 730028 evaluation board, including components for optional circuit configurations, is illustrated in Figure 1. The primary connections are shown with solid lines while the optional input and digital interface connections are shown with dashed lines.

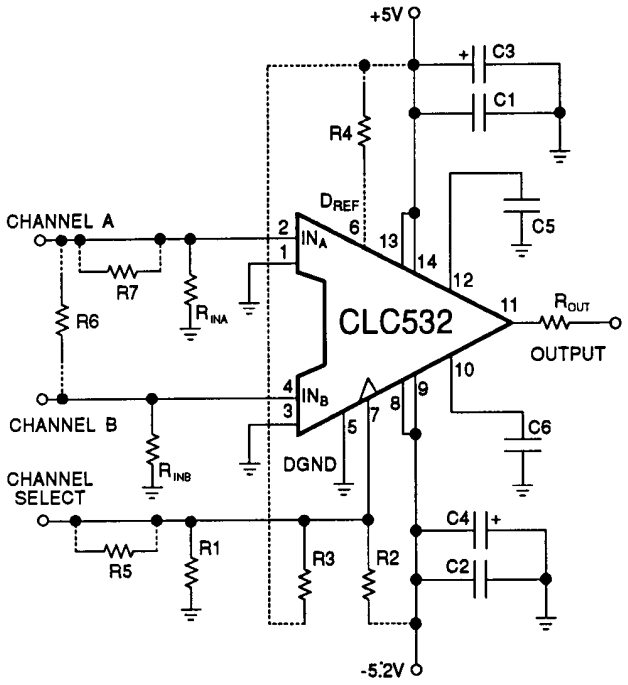

Figure 1: CLC532 Evaluation Board Schematic

The CHANNEL A and B (pins 2 & 4) analog inputs of the CLC532 are buffered high-impedance pins. The two input termination resistors (R_{INA} & R_{INB}) provide impedance matching for the analog sources; a 50Ω environment is assumed. The closed-loop active output of the CLC532 provides a very low output impedance, typically 1.2Ω. For driving 50Ω systems, a 48.7Ω series output resistor (R_{OUT}) will provide a close back matched impedance for 50Ω cables.

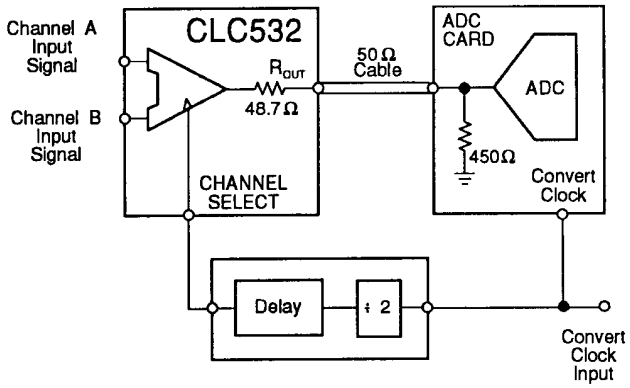

Figure 2: Driving Remote A/D Converter Inputs

Figure 2 illustrates the CLC532 evaluation board connections when driving the high-impedance input of a remote A/D converter. Most high quality, high-resolution, A/D converters employ a high-impedance input stage. This allows the CLC532 to operate with relatively high load resistors (>200Ω), greatly improving CLC532 distortion performance. When the CLC532 drives the A/D converter remotely from a separate board, a 48.7Ω series output resistor prior to a 50Ω connecting cable followed by a 450Ω termination resistor at the input of the A/D converter, results in an effective 500Ω load. When driving A/D converter inputs directly, a 500Ω termination load is recommended with no series resistance.

The CLC532 is capable of functioning with ECL, TTL, and CMOS logic families. Logic compatibility is controlled by D_{REF}. In normal operation, D_{REF} is left floating and the channel SELECT responds to ECL level signals. For TTL and CMOS level SELECT inputs, D_{REF} should be tied to +5V (the CLC532 D_{REF} input is internally buffered through a 2300Ω resistor). TTL and CMOS operation requires the use of a resistor input network for the channel SELECT. Without the input network, SELECT logic levels above 3V will cause internal junction saturation and slow switching speeds.

The CLC532 evaluation board is labeled for ±5V supplies. Normal ECL logic, and many A/D converters, employ a -5.2V V_{EE} supply rather than the indicated -5.0V supply. Either value is acceptable with negligible impact on performance.

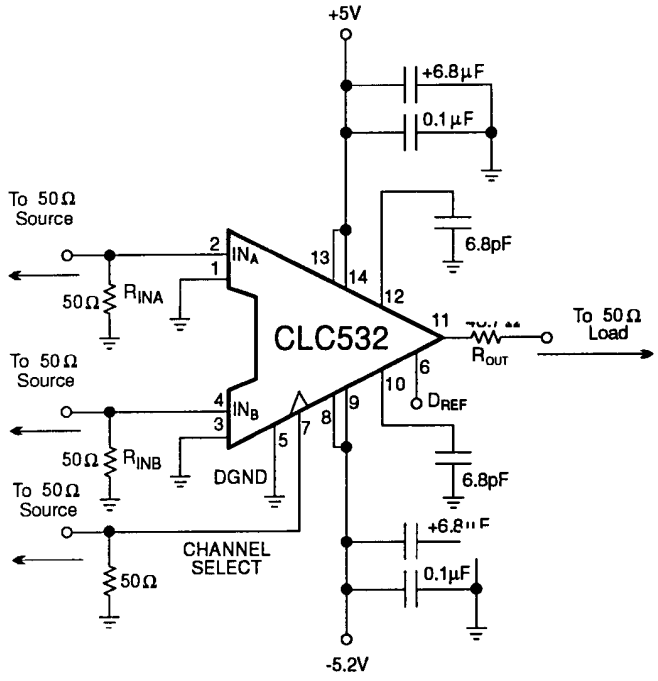

Figure 3: Basic Evaluation Schematic

Figure 3 illustrates the basic CLC532 multiplexer configuration. This configuration terminates both inputs with 50Ω and places a 48.7Ω back-terminating resistor (R_{OUT}) at the output. With D_{REF} left floating (ECL logic levels), the channel SELECT input is terminated with a 50Ω resistor to ground. This configuration assumes a 50Ω signal source provides the channel SELECT input. If standard ECL logic devices are available to drive the channel SELECT input directly, the evaluation board can be configured for standard Thevinen equivalent input terminations. A 50Ω termination resistor to a -2V bias supply can also be used. See *Channel SELECT Logic Interfaces section*. The overall gain seen at the matched load is 0.5V/V (-6dB). The compensation capacitors (C5 & C6) have been selected for a maximally-flat frequency response.

Compensation Capacitors

The compensation capacitors (C5 & C6) are used to *tune* the CLC532's frequency response for a given load. Figure 4 provides the compensation capacitor values for a maximally-flat frequency response. For symmetric slew rates, C5 and C6 should be equal. Figure 5 provides the -3dB bandwidth and slew rate vs. compensation capacitor values. The compensation capacitors can be used to limit the CLC532's noise-bandwidth. Given a single-pole frequency response, the noise bandwidth will be approximately ... (1.57)(f_{-3dB}).

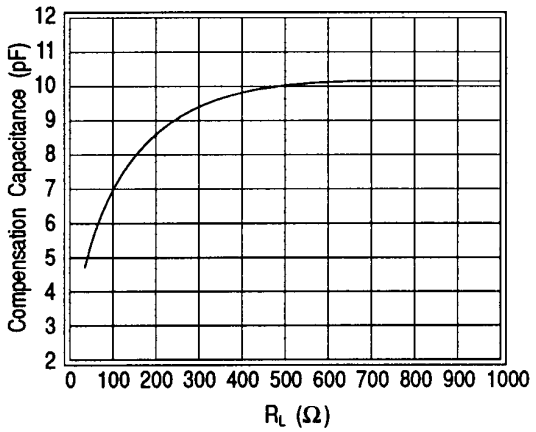

Figure 4: Maximally Flat Frequency Response

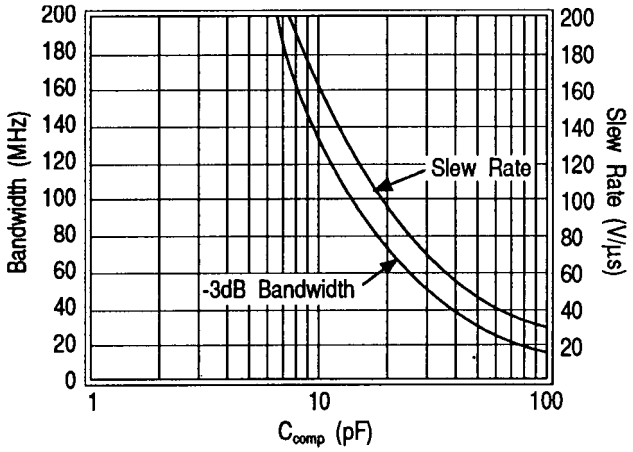

Figure 5: Slew Rate and Bandwidth vs. Compensation

Channel SELECT Logic Interfaces

The CLC532 accepts channel SELECT inputs from a variety of logic families and sources. During evaluation, a signal generator is commonly used to drive the channel SELECT input. Accordingly, the evaluation board has been initially configured with a 50Ω SELECT input termination resistor to ground. When driving channel SELECT with actual ECL, TTL or CMOS logic gates, it will be necessary to add an appropriate input network. The 730028 evaluation board provides the necessary component locations for these networks, and Figure 6 illustrates the recommended TTL and CMOS configurations.

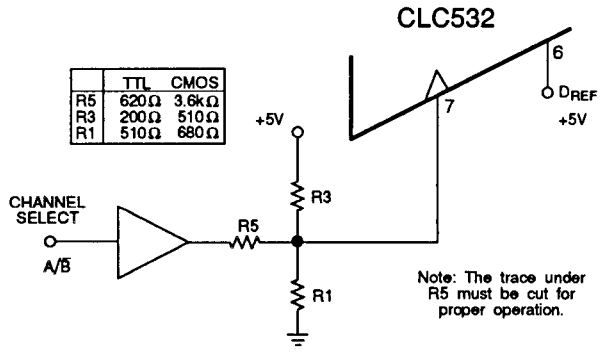

Figure 6. Recommended TTL/CMOS Interface Networks

The TTL and CMOS networks limit the maximum voltage swing at the channel SELECT input (pin 7) to less than 3.0V. Exceeding 3.0V will saturate the internal switching logic and cause slower switching speeds. If the input of the TTL or the CMOS networks is left floating, CHANNEL A will be selected. Use of the series resistor (R5) requires the cutting of the channel SELECT input trace below R5. This is easily accomplished on the back side of the evaluation board.

Driving the CLC532 with standard ECL logic gates requires one of the standard ECL terminations at the channel SELECT input. The network of Figure 7 provides a Thevinen equivalent termination of 50Ω to -2V. If a -2V bias supply is available, the standard 50Ω to -2V is certainly acceptable. Allowing the input to this network to float will select CHANNEL B.

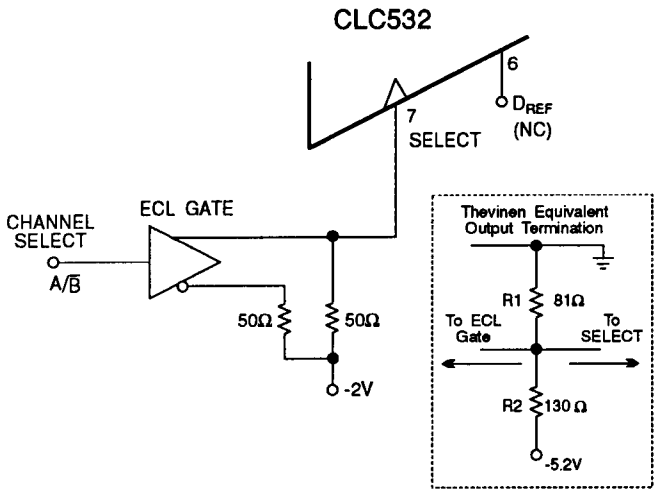

Figure 7: Standard ECL Terminations

Signal Input Options

The CLC532 evaluation board is capable of implementing a switched gain stage by driving CHANNEL B with an attenuated version of the CHANNEL A input signal. Illustrated in Figure 8, this circuit quickly switches between the full amplitude signal at CHANNEL A and the -6dB version of that signal at the input of CHANNEL B. This circuit provides a simple 50Ω termination for the channel SELECT input, although any of the previous circuits are equally acceptable. The series resistor at the input of CHANNEL A (R7) matches its source impedance to that of CHANNEL B (ie. R7=R6||R_{INB}), generating equal poles from the parasitic input capacitances . This type of source impedance matching will also minimize input bias current induced offset errors.

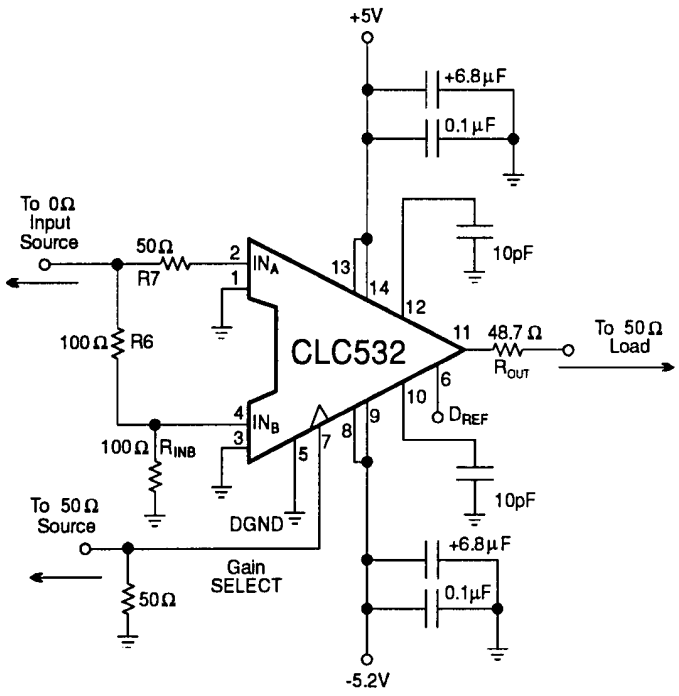

Figure 8: Basic Gain Select Configuration

The switched-gain circuit of Figure 8 should be driven from a low output impedance, wideband, amplifier. Figure 9 uses a CLC406 at a gain of +2V/V to drive both inputs of the CLC532 switched gain circuit. With CHANNEL A selected, the signal at V_{OUT} will be a 0dB (unity gain) version of the input signal. With CHANNEL B selected, the CLC532 will produce a -6dB (0.5V/V) representation of the input signal at V_{OUT}. Figure 10 shows the signal at V_{OUT} using a 10MHz analog input signal, with the channel SELECT toggled at 500kHz. This approach can be easily extended to different gain settings.

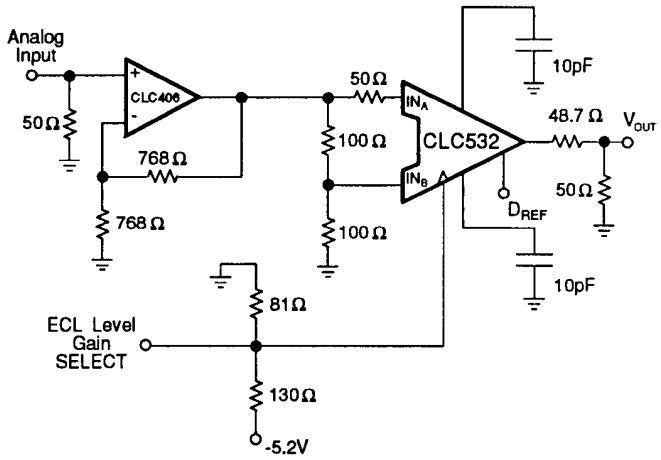

Figure 9: CLC406 Driver for the Switched Gain Configuration

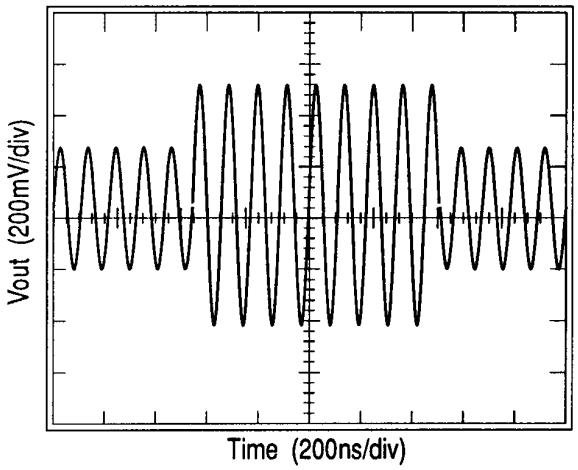

Figure 10: Gain Select Output with 500kHz Toggle Rate

Board Layout Suggestions

The 730028 board has been designed to provide the maximum channel isolation and best fine-scale pulse-settling performance. Channel isolation requires good trace separation between the two inputs, while a ground plane placed between the inputs and the output will serve to isolate the unselected channel from the output.

On the CLC532 evaluation board, the ground connections for the analog input terminating resistors play a strong role in channel isolation performance. The input termination resistor ground connection for CHANNEL B has been placed immediately adjacent to its input SMA connector. The input termination resistor ground connection for CHANNEL A has been placed at right angles to the input trace, and away from the CHANNEL B input. The optimum geometry for input termination resistor ground connections will likely vary from design to design. Some empirical testing may be required.

To achieve high-speed 14-bit settling accuracy, careful attention must be given to ground currents and the electrolytic power supply bypass capacitors. The ground connections of the electrolytic bypass capacitors must have a short and symmetric path to the ground connection of the CLC532 output load. In the case of the 730028 evaluation board, the output SMA connector provides the ground connection for the output load/return currents. Figures 11 and 12 illustrate the layout for the 730028 evaluation board.

The I/O connectors are SMA (straight) Amphenol 901-144 and SMA (right angled) Amphenol 901-143

The device thru holes are large enough to accommodate flush mount socket pins if socketing is desired. These should be - Cambion P/N 450-2598 or equivalent. Standard DIP sockets are specifically not recommended; the relatively long socket leads will severely degrade the ac performance of the CLC532.

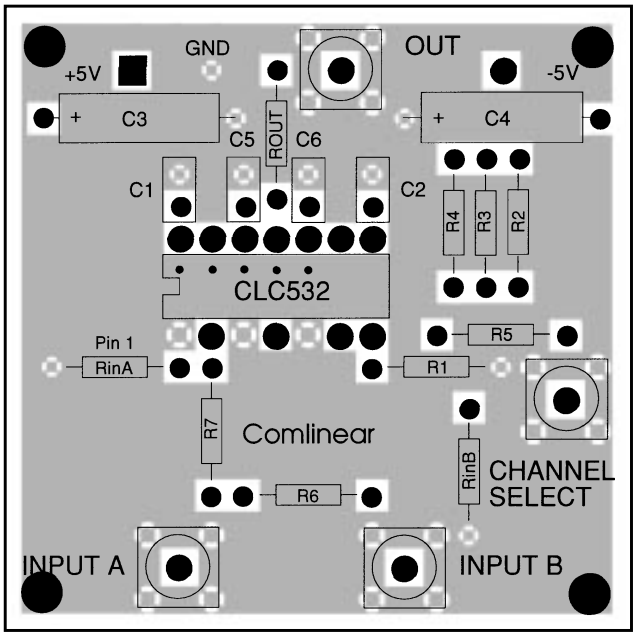

Figure 11: 730028 Top Metal - Ground Plane (top view)

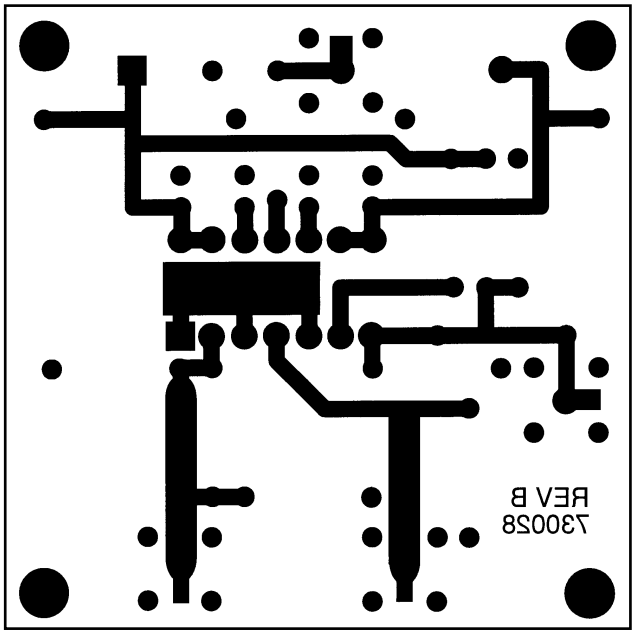

Figure 12: 730028 Bottom Metal (top view)

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