National Semiconductor

CLC520/522 Evaluation Boards

Part Numbers CLC730029, CLC730033

August 1996

The CLC730029, Rev. B (through-hole) evaluation board provides an easy means of testing the operation and performance of both the CLC520 and the CLC522 in their 14-pin DIP packages. **Note, this board obsoletes an earlier CLC520 evaluation board - part CLC730021.** A similar board, CLC730033, Rev. B, (SOIC) accommodates the CLC520 and CLC522 surface mount versions. Please refer to the CLC520 and the CLC522 data sheets for complete performance information.

I. Basic Operation

Figure 1 shows the complete evaluation circuit implemented on this board. The primary connections are shown with solid lines, while several optional circuit connections are shown with dashed lines.

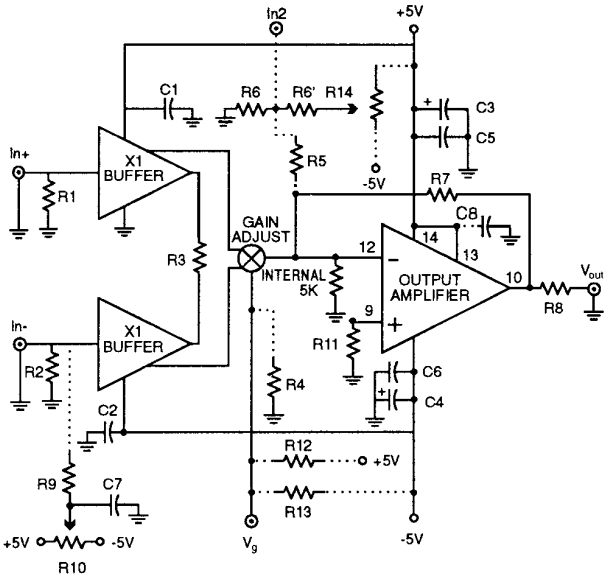

Figure 1: External components & amplifier internal block diagram

The CLC520 and the CLC522 have the same pin definitions with the only exception of an additional $+V_{CC}$ connection on pin 13 of the CLC522, whereas pin 13 is a no-connection the CLC520. The evaluation board hard-wires pin 13 and pin 14 together, applying $+V_{CC}$ to both pins allowing the board to accommodate both devices. The key operational differences between the CLC520 and the CLC522 are found with the gain-adjust input (V_g: pin 2). The gain-adjust input voltage range of the CLC520 is 0-2V while that for the CLC522 is ±1.0V. Also the gain-adjust input resistance (pin 2 to ground) is typically 750Ω for the CLC520 and typically 100kΩ for the CLC522. One wiring difference should be noted, the ground connection from pin 9 (R11 on the evaluation board) of the output amplifier's non-inverting input should be a very low inductance short to ground for the CLC520 and 20Ω for the CLC522.

II. Basic CLC520 Connection

Figure 2 represents the simplest board configuration for the CLC520. The specific resistor values depicted here configure the CLC520 with a maximum gain of +10V/V; this is the condition used to specify the part in its data sheet.

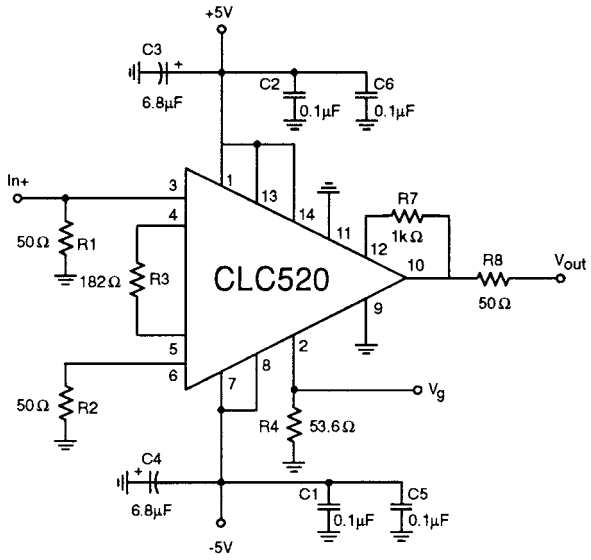

Figure 2: Basic CLC520 Connection

The circuit of Figure 2 implements a non-inverting variable-gain amplifier with a 50Ω input impedance (R1), a 50W output impedance (R8), and a maximum gain of +10V/V (1.85*(R7/R3)). Recognizing the combination of the 50Ω series output resistor and the 50Ω load results in a voltage divider, the gain to this matched load is one half of the maximum device gain setting, i.e. +5 (14dB). The gain adjust input has a 0-2V range with V_g > 2.0V yielding the maximum gain while V_g = 0V yields the maximum signal attenuation. Note, the CLC520's parallel combination of R4 (53.6Ω) and its internal 750Ω resistor to ground on pin 2 results in a 50Ω input impedance for V_g. The inverting input (In-) is ground-referenced through 50Ω while the output amplifier's non-inverting input is ground-referenced at pin 9. The evaluation board provides a component location at pin 9 (R11) used as a ground connection for the CLC520. This ground connection should be very short from the hole for R11 directly to the top-side ground plane, not a long wire in place of R11. In an application board layout, the CLC520's pin 9 should be taken directly into a very low-

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inductance ground plane with as little lead length as possible. This will prevent the possibility of a high-frequency resonance (>400 MHz) in the output amplifier's input stage from causing any stability or frequency response problems. Earlier discussions of the CLC520 implied that pin 9 could be used to introduce a DC offset into the output amplifier. Due to its limited input voltage range and the need for a broadband low source impedance on pin 9, this method of introducing a DC offset is not recommended. As will be discussed later, an additional signal or DC offset can be more effectively introduced through the inverting input (pin 12).

III. Basic CLC522 Connection

Figure 3 shows the simplest configuration for evaluating the CLC522. The specific resistor values depicted here configure the CLC522 with a maximum gain of +10V/V; this is used to specify the part in its data sheet.

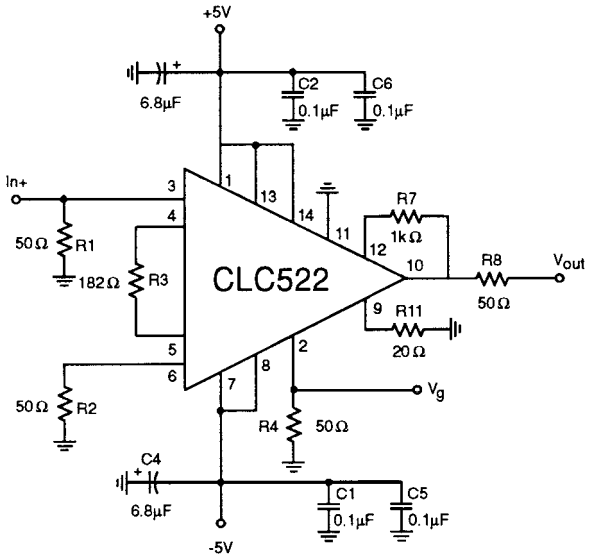

Figure 3: Basic CLC522 connection

This circuit is nearly identical to that of the CLC520. The only two circuit changes are seen at the gain-adjust input (pin 3), terminated here in 50Ω as opposed to the CLC520's 53.6W (the difference lies in the fact that the CLC522 has a much greater input impedance through pin 2 than the CLC520) and the ground-reference of the output amplifier (pin 9) is taken to ground through a 20Ω resistor (R11). The input gain-adjust voltage range of the CLC522 is ±l V. -1V for minimum gain (maximum attenuation) to +1V for maximum gain set by 1.85-(R7/R3). Again, the ground connection on inverting input of the pin 9 is very critical to the high-frequency stability of the amplifier. In this case the 20Ω resistor acts to stabilize a high frequency (>400 MHz) resonance in the output stage. An optional power-supply decoupling capacitor (C8) is shown with the CLC522 on pin 13 of Figure 1. A 0.01µF capacitor located at C8 can be used to slightly improve the device's fine scale pulse settling time, however, in most cases this capacitor is not required for evaluation.

IV. Gain Control Input Resistor Options

Two additional resistor locations (R12 & R13) are included on the gain-adjust line. The resistor locations may be used to introduce a DC bias on pin 2. Figure 4 provides an example of how R12 and R13 can be used to fix the CLC520 and the CLC522 at their maximum gains by applying a resistive DC-bias voltage on pin 2 in the absence of an applied V_g input. Note, the CLC520 presents an approximate 750Ω resistance on pin 2 while the CLC522 is typically 100kΩ.

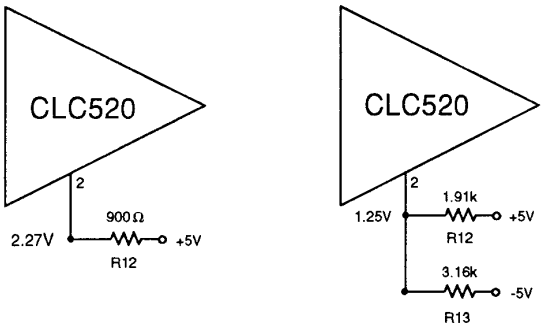

Figure 4: Setting up for the fixed maximum gain

One CLC520 application (shown above) is a fixed maximum-gain connection combined with an open-collector pull-down (not shown) to disable the gain channel. If an open-collector gate is used to pull pin 2 low, the signal would see its maximum attenuation. While this arrangement will greatly improve the down-stream signal isolation, it will not cause the CLC520's output to rise to a high impedance nor reduce its quiescent current.

A related CLC522 application (shown above) reverses the positions of the two resistors, resulting in a negative DC bias on pin 2. This arrangement will place the part into a default maximum-attenuation mode and therefore, in the absence of an applied V_g voltage, isolate the part from signal transmission. Since the resistors used here are relatively large, any DC source for V_g can be used to drive pin 2 to the desired gain-control voltage.

V. Summing Signals and Offsets into the Output Stage

The output amplifier's inverting node (pin 12) is available to introduce any additional signals or offsets into the output. Since pin 12 is a virtual ground, additional signals may be summed into this node without a substantial impact of the signal current flowing from the adjustable-gain path. Briefly, adding an additional impedance on the output amplifier will result in a slight bandwidth reduction of the output amplifier and an increase in the noise gain for the output amplifier's non-inverting input noise voltage. Refer to application note OA-13 for a more thorough discussion of current feedback amplifiers in inverting summing applications. Figure 5 shows an example of using the optional components on the board to sum in a high-speed signal with a gain of -2 to the output pin (or -1 to the matched 50Ω load).

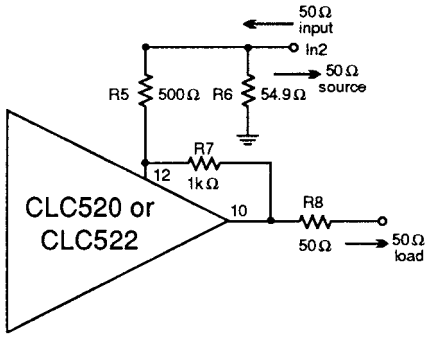

Figure 5: Summing a high-speed signal into the output

Note, R6 can be used in either of two locations on this board. In Figure 5 R6 is positioned as part of the output op amp's inverting input (In2) termination. Alternatively, it can be positioned to pick off the wiper voltage of an offset-adjust pot (R14 Figure 1) which is to be fed into the inverting node of the output amplifier. Figure 6 shows this application where an output offset, independent of the gain adjustment stage, is introduced into the inverting node of the output amplifier.

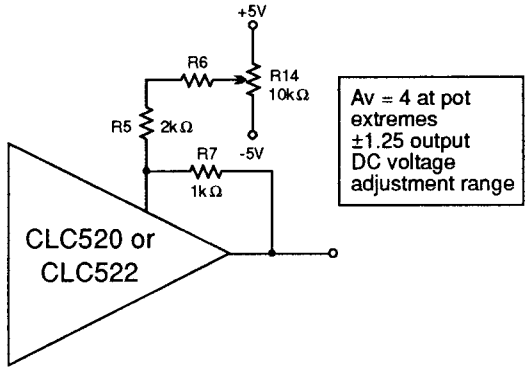

Figure 6: Summing in an output DC offset

VI. Nulling the Output DC Offset

Both the CLC520 and the CLC522 consist of three major functional sections each of which contributes a DC offset voltage to the output of the device; the differential input buffer, the multiplier core and the output amplifier. The offsets produced by the input buffer and the output amplifier can be nulled with the appropriate external circuitry. It will not be possible to completely null the offset effects of the multiplier core because of its non-linear nature. As a result, a small non-linear DC offset voltage gain over the adjustment range will always be present at the output of the device. Figure 7 shows the required external circuitry necessary to add the appropriate nulling offsets at both the input buffer and the output amplifier.

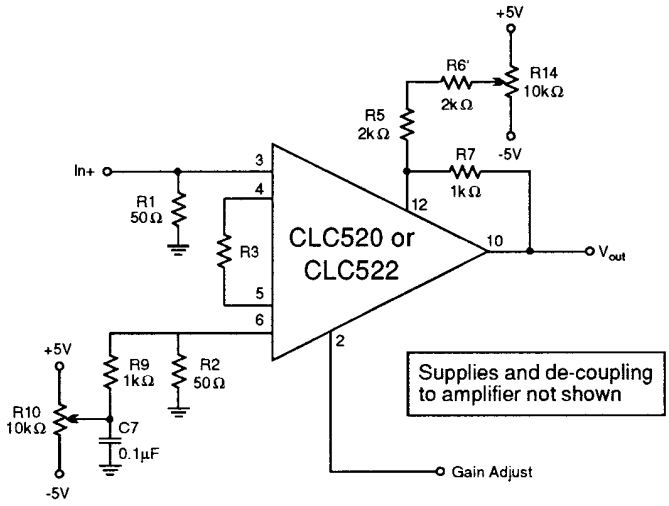

Figure 7: Input and output stage DC nulling

The output stage offset should be trimmed prior to the input stage. With the gain adjust pin set at minimum gain (maximum attenuation), the output stage offset may be nulled independently from the input stage. R14 should be adjusted to yield the desired output error voltage (typically <1 mV). Having corrected for the input offset voltage and bias current errors of the output amplifier, returning the gain adjust pin to the maximum gain voltage will allow the input buffer stage DC offset errors to be corrected. With no input signal present, but with matched source impedances at each of the two buffer inputs, R10 in Figure 7 can be adjusted to bring the output to within the desired error band.

Adjusting the input and the output stage offsets at the two gain extremes will hold the output DC error at a minimum at these two points in the gain range. If a more limited gain range is anticipated, the adjustments should be made at these operating points. The non-linear DC error introduced by the multiplier core will cause a residual, gain dependent, offset to appear at the output as the gain is swept from minimum to maximum. Also, neither the input nor the output offset adjustments described here will improve temperature drift effects. Please see the CLC522 data sheet for a more complete discussion of DC offset control.

VII. Printed Circuit Board Layout

The CLC520/522 evaluation boards show a careful attention to parasitic effects in the layout. Generally, any parasitic it coupling path to an AC ground (this includes both power and ground planes) should be avoided at any of the signal input and output pins. At the same time, a very good, close proximity, ground plane needs to be provided for the power supply de-coupling capacitors.

These boards show the ground plane totally opened up around the part, but close enough to provide minimum parasitic inductance for the the de-coupling capacitor connections. The ground plane on the evaluation boards is also part of a 50Ω transmission line impedance implemented on the two buffer input and gain adjust traces.

Best frequency response flatness is obtained if there is minimal parasitic capacitance to ground on the output of the two input buffers, pins 4 & 5. The gain setting resistor (R3 on these boards) should be in very close proximity to these pins with short, symmetric, PC board traces connecting to pins 4 & 5. As application note OA-16 describes, this trace symmetry to the gain setting resistor will improve the high frequency CMRR in differential amplifier applications.

All of the I/O pins associated with the output stage amplifier are particularly sensitive to parasitic capacitance to an AC ground. The non-inverting input pin (pin 9) should be tied directly to the ground plane for the CLC520, while a 20Ω resistor to ground (R11) should be used for the CLC522. The output amplifier's feedback resistor,(R7), should also be connected between the output and the inverting input (pins 10 & 12) with minimum trace length and parasitic coupling to any AC ground. And finally, the output pin should be buffered from the load by a resistor, (R8), that is acting as either an impedance matching resistor, for driving a doubly terminated transmission line, or as an isolation resistor, when driving capacitive loads. Please see the amplifier data sheets for the recommended series resistor value vs. capacitive load.

Figures 8 and 9 show the board layouts for these two evaluation boards.

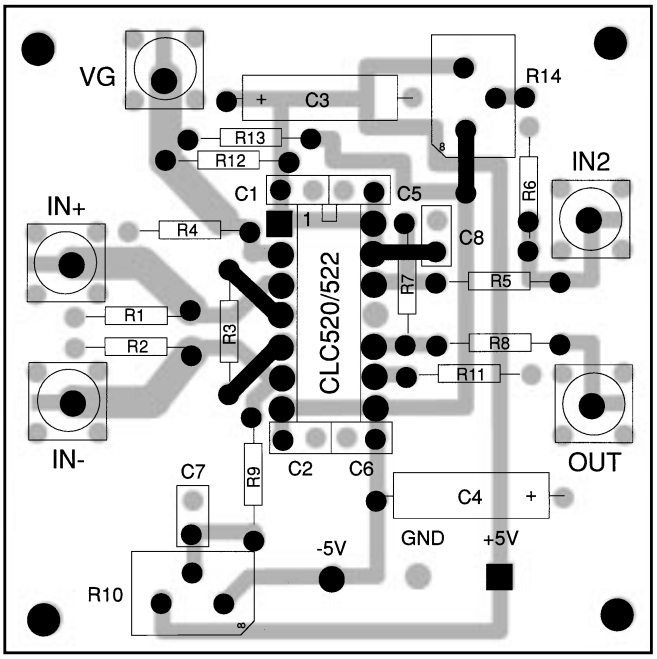

Figure 8: 730029, Rev. B

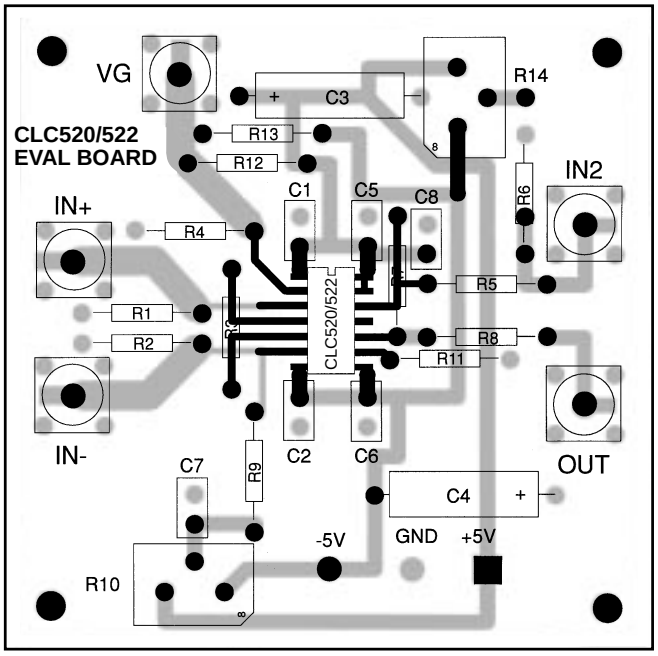

Figure 9: 730033, Rev. B

Evaluation Board Parts List - See the device data sheets along with the discussion and examples shown here when selecting component values.

		Recommended Type
R1,R2	Input terminating resistors	RN55D 1% metal film
R3	Gain setting resistor	RN55D
R4	Gain adjust termination res.	RN55D
R5,R6	Output signal summing	RN55D
R7	Output amp. feedback res.	RN55D
R8	Output imped. matching res.	RN55D
R9	Input offset injection res.	RN55D
R10	Input offset adjustment pot	Bournes 10k cermet pot
R11	Output non-invert. gnd. res.	RN55D
R12,R13	Gain adjust default setup	RN55D
R14	Output offset adjustment pot	Bournes 10k cermet pot

Notes: R11 should be a simple grounding strap for the CLC520. Slightly improved AC response can be obtained by using very low reactance resistors (Precision Resistive Products type PRP-8351) for R7 & R3.

Cl, C2, C5, C6, C7	0.1µF Ceramic capacitor
C8	0.01µF Ceramic capacitor
C3,C4	6.8µF Tantalum capacitor (Sprague 150D or equivalent.)

The 1/0 connector styles are:

-SMA (straight) Amphenol 901-144

-SMA (right-angled) Amphenol 901-143

The device through-holes on the 730029 board are large enough to accommodate flush-mount socket pins if it is desired to socket the part. These should be Cambion P/N 450-2598 or equivalent. It is important not to use a standard 14-pin socket since the relatively long connector distance above the board will severely degrade the AC performance of the CLC520 and CLC522.

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

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Fax: 81-043-299-2408