National Semiconductor

CLC503 Evaluation Board

Part Number E503PCASM

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Description

The Comlinear E503PCASM evaluation board is designed to support simple and effective evaluation of the CLC503 as a front end driver to the CLC949 Analog-to-Digital Converter. To operate the evaluation board you need only supply power, a clock and a signal to be digitized. The evaluation board uses a common Eurocard connector to make the power, ground and data connections with the rest of the evaluation system. There are options on the board to generate a clock from a sinusoidal source or to use a suitable CMOS clock. The bias points for the converter can be selected via a DIP switch. For a complete description of these various options, please refer to the CLC949 datasheet.

Clock Generation

The evaluation circuitry includes a clock generation circuit that will convert a sinusoidal input to a CMOS clock for use by the CLC949. When using this option the clock signal that is provided should be 2-3V_{pp} (10-14dBm). For best results when digitizing high speed input signals, the converter must have a very low jitter clock. To generate this the sinusoidal input must have very low phase noise. In a laboratory environment, Comlinear suggests the use of a low phase noise synthesizer such as the HP8662 or the HP8643 as a clock source.

There is also an option that will enable you to provide a TTL or CMOS clock directly to the board. The clock is provided through an SMA connector, regardless of the clocking option chosen. To enable the input of a digital clock, remove the three jumpers labeled OPT4 and insert a jumper at the point labeled OPT1-3. These jumpers can be found on the opposite side of the board to the CLC949 and a surface mount 0 resistors.

Analog Input Conditioning

The CLC949 requires a differential input signal, centered around a bias point of approximately 2.25V The CLC503 takes a single ended, ground referenced input, and the midpoint bias output from the CLC949 and conditions the input signal to provide the CLC949 an acceptable input. For more information on the CLC503, please refer to the CLC503 datasheet. There are other ways of generating the appropriate input signal (discrete circuitry, transformer coupling etc.) Options for these types of input conditioning can be found on the E949PCASM evaluation board which is similar to the E503PCASM board except for the analog input conditioning section.

DATA and Clock Outputs

The E503PCASM Evaluation board is equipped with 74F574 latched which latch the CLC949 output data and drive the eurocard connector. The an inverted version of the A/D clock is also provided on the Eurocard connector. The output data format of the CLC949 is selectable between Offset Binary or Twos Complement via the jumper OPT6. For Offset binary operation install the jumper in the location OPT6A, two complement is achieved by use of OPT6B. These jumpers can be found on the front of the board, just above the CLC949 chip.

Bias Control

The CLC949 offers you the ability to make a tradeoff between dynamic performance and power dissipation. This can be done by selecting one of three discrete bias points with the DIP switch on the board, or by selecting option 5 which allows analog control of the bias current through the selection of R23. The bias point can be selected according to the following table:

SW1A	SW1B	Bias Point
ON	ON	Low Bias
OFF	OFF	Medium Bias
ON	OFF	High Bias
OFF	ON	Set with R23

If you select option 5, you must install the jumper labeled OPT5. Please refer to the CLC949 datasheet for assistance in selecting an appropriate value for R23.

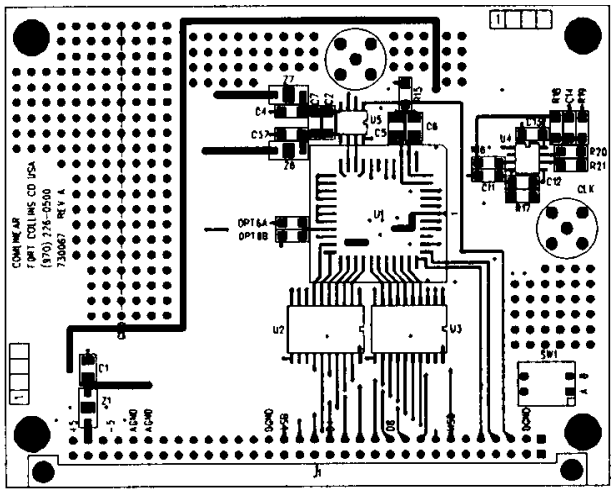


Figure 1: Top layer metal and silk screen

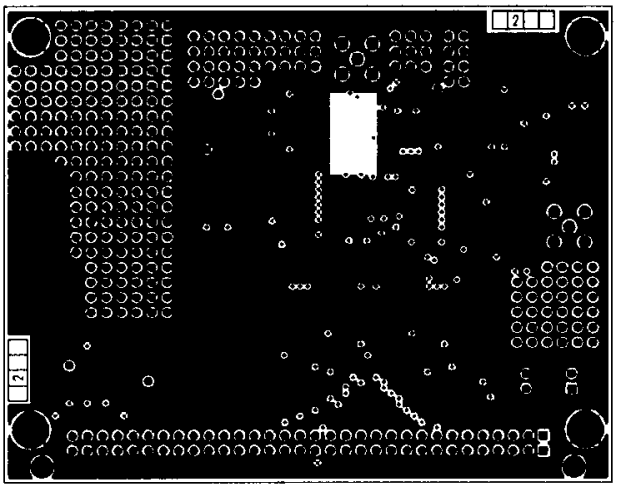


Figure 2: Layer 2 metal (internal ground plane)

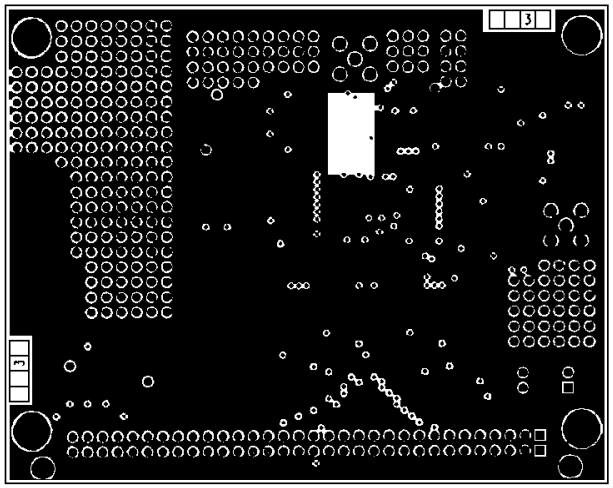


Figure 3: Layer 3 metal (internal ground plane)

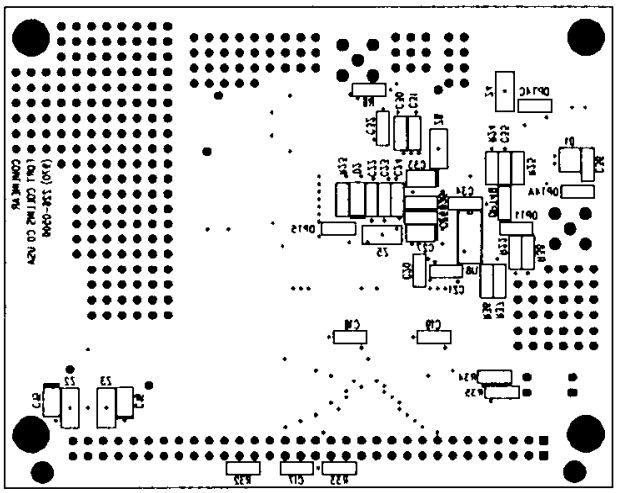
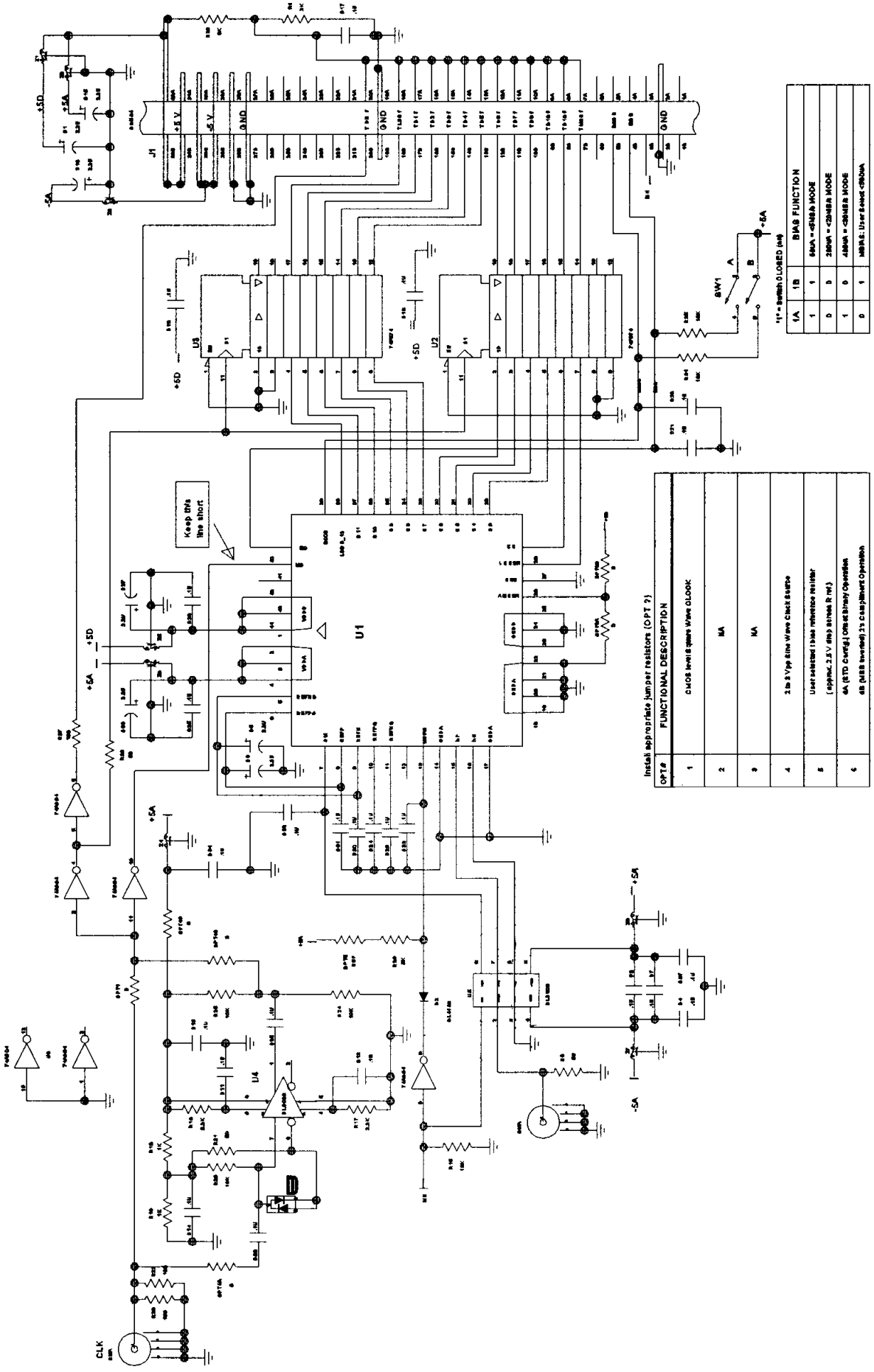


Figure 4: Bottom layer metal and silk screen

CLC503 Evaluation Board (P/N 730067 Rev. A)



Install appropriate jumper resistors (OPT 7)

OPT#	FUNCTIONAL DESCRIPTION
1	CMOS level square wave CLOCK
2	NA
3	NA
4	2 to 5 Vpp sine wave clock source
5	User selected bias reference resistor (approx. 2.5 V drop across R ref.)
6	4A (STD Config) Offset Binary Operation 4B (MSB Inverted) 2's Comp/Invert Operation

1A	1B	BIAS FUNCTION
1	1	5MHz = <5MHz MODE
0	0	20MHz = <20MHz MODE
1	0	40MHz = <20MHz MODE
0	1	MSB/E: User Select <20MHz

"1" = switch CLOSED (to)

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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