National Semiconductor

CLC114/115 Evaluation Boards

Part Number CLC730023

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The 730023 is an evaluation board designed to aid in the evaluation and characterization of the CLC114 and CLC115 closed-loop quad buffers. The CLC114 is intended for use in applications requiring lower power operation while the CLC115 is intended for use in systems requiring wider bandwidth and higher output drive capability. Both of these quads offer four unity gain buffers in one 14-pin package. The individual data sheets provide more detailed information on applications and specifications.

The 730023 evaluation board allows for the construction of a number of different circuits utilizing both the CLC114 and the CLC115. Two of the four channels on the board are arranged for the evaluation of signal buffering in a 50Ω environment while two other channels integrate on-board , user-selected, RC active filters. Each type of filter, low pass or bandpass, can be implemented by selecting the appropriate RC component. The filters are designed to use all four of the buffers configured in series: an input buffer, one or two cascaded active filter stages and an output buffer.

The complete schematic of the 730023 evaluation board, showing all component locations, is shown in Figure 3. The parallel resistor/capacitor locations are intended for use with either a resistor or a capacitor with the choice of component depending upon the type of filter. Figure 4 shows the component placement for a cascaded bandpass filter and Figure 5 shows the component placement for the cascaded low pass filter. Each of the two low pass filter sections can be configured as either a second or a third order filter. Configuration of the third order filter requires the placement of additional components. Channel 1 requires R_1, C_1 and channel 4 requires R_6, C_6. It will be necessary to cut the 50Ω strip line from the input of channel 3 (pin 5) in order to evaluate the active filter circuit. Separate evaluation of the buffer circuits requires a 50Ω resistor to be placed at the input of channels 1 and 4 (R_4 and R_9) to insure stability of the unused buffers.

Low Pass Filter Design with the 730023 Evaluation Board

Figure 5 shows the schematic for a low pass filter. The two filter sections may be configured as either a second or a third order filter and therefore, configured in series, provide for a fourth or fifth order low pass filter.

Low Pass Filter Design Equations

It is a common practice in filter design to begin with the synthesis of a filter normalized in frequency and impedance. This method simplifies the derivation of design equations and allows for the convenient calculation of component values. Circuit resistors are normalized to 1Ω and resonant, or cut-off frequencies, are normalized to 1rad/sec [3]. Now, the design effort is reduced to the calculation of capacitor values in an RC active filter. For simplicity, the filter design equations below use the component designations of channel 1, shown in Figure 5.

Second-Order Filter

Using $R_2, R_3 = 1\Omega$ ($R_1 = 0$, $C_1 = 0$ for second order), the normalized transfer function is

$$H(s) = \frac{1}{C_3 C_5 s^2 + 2C_3 s + 1}$$

The roots of this transfer function are a complex pole-pair at $s = \alpha \pm j\beta$.

H(s) can then be expressed in terms of this pole-pair.

$$H(s) = \frac{1}{\frac{s^2}{\alpha^2+\beta^2} + \frac{2\alpha s}{\alpha^2+\beta^2} + 1}$$

equating coefficients in these two equations for the two capacitors yields

$$C_5 = \frac{1}{\alpha}, \quad C_3 = \frac{\alpha}{\alpha^2+\beta^2}$$

The pole locations (values for α and β) for all filter types (Butterworth, Bessel, Chebyshev etc.) can be found in the references listed at the end of this application note.

Third-Order Filter

Using $R_1, R_2, R_3 = 1\Omega$, the normalized transfer function is

$$H(s) = \frac{1}{As^3 + Bs^2 + Cs + 1}$$

where

$A = C_1 C_4 C_5$; $B = 2C_4(C_2 + C_5)$; $C = C_1 + 3C_4$

Solving for the capacitor values in terms of the pole locations is cumbersome. As a practical matter, the capacitor values have been tabulated [2] for this filter topology. The design of an n^{th} order filter is done by looking up capacitor values for a filter normalized to a −3dB frequency of 1rad/sec.

Once the normalized capacitor values have been found, the actual component values are found by scaling for frequency and impedance. The normalized capacitor values are frequency scaled by dividing them by the desired cut-off frequency ω_c, $\omega_c = 2\pi f_c$. Impedance scaling is then performed by dividing the frequency scaled capacitor values by a resistor of value R. This resistor value is chosen such that impedance scaling produces reasonable capacitor values. All resistances have been assumed equal for a particular filter section. The resistors (normalized to 1Ω) are then impedance

scaled by multiplying by the impedance scaling factor R. The following equation summarizes these two steps for calculating actual capacitor values.

$$C = \frac{C_{normalized}}{2\pi f_c R}$$

Design Example. Fifth-Order Bessel Low Pass, $f_c = 1MHz$.

A fifth-order Bessel (maximally flat delay) low pass filter can be built from a cascade of a third and a second-order filter section. A fifth-order polynomial must first be factored into second and third order polynomials (whose product is the desired fifth-order Bessel polynomial). The cascade of a second and a third-order Bessel polynomial does not yield a fifth-order Bessel polynomial. For a fifth-order circuit, the following normalized capacitor values are found [2].

third-order section: $C_5 = 1.010F$; $C_4 = 0.3095F$; $C_1 = 0.8712F$

second-order section: $C_5 = 1.041F$; $C_4 = 0.3100F$

Scaling for frequency and impedance, the calculated component values are as follows:

third-order section:

$R = 2.37k\Omega$; $C_5 = 68pF$; $C_4 = 20.8pF$; $C_1 = 58.8pF$

second-order section:

$R = 1.82k\Omega$; $C_5 = 91pF$; $C_4 = 27.1pF$

Due to buffer input capacitance, C_1 and C_4 were slightly decreased in value. A circuit was built according to Figure 5 with these component values:

R_{in1}, R_{in2}, $R_{11} = 50\Omega$; R_1, R_2, $R_3 = 2.37k\Omega$;
R_7, $R_8 = 1.82k\Omega$

C_{11}, $C_{14} = 6.8\mu F$; C_{12}, $C_{13} = 0.1\mu F$; $C_1 = 56pF$,
$C_4 = 18pF$; $C_5 = 68pF$, $C_9 = 24pF$, $C_{10} = 91pF$;
R_6, $C_6 = 0$

In the passband, the group delay (τ) for a fifth-order Bessel lowpass filter [1] is

$$\tau = \frac{2.4}{2\pi f_c sec} \quad \text{for } f_c = 1MHz,\ \tau = 382nsec.$$

Figure 1 shows the frequency response of the magnitude, phase and group delay. The group delay can be approximated from the phase from the equation

$$\tau = \frac{\Delta\varphi(degrees)}{360^\circ(\Delta f)}$$

where Δ is the delay aperture, $\Delta\varphi$ is the phase change over the delay aperture. In this filter, the group delay was constant within 3% to 1.3MHz, using a delay aperture of 25kHz.

Figure 5. Fifth-Order Bessel Low Pass Response

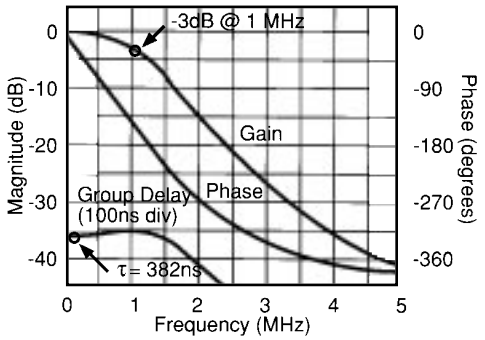


Figure 1

Second-Order Bandpass Filter Performance Equations

The circuit of Figure 4 is a cascade of two second-order bandpass filters to yield a fourth-order bandpass filter. This circuit is often simplified [4] by choosing R_2, R_4, $R_5 = R$ and C_2, $C_3 = C$. This approach is adequate when the gain of the amplifier, K, can be chosen by the designer. When K is fixed (as in the case of a unity-gain buffer) only the resistor and capacitor values are left to determine circuit performance. Furthermore, it can be shown [3] that the equal-R, equal, equal-C design has poor performance sensitivity to component variation. For example, making $C_2 > C_3$ will increase the Q of the circuit (other components remaining the same as the equal-C case) while simultaneously decreasing the Q-sensitivity to other circuit parameters.

Below are equations for ω_o, Q and midband gain for two extremes of circuit component constraints. The equal-R, equal-C equations offer the simplest circuit design with the most restricted performance. Conversely, allowing free choice of all component values allows the designer to optimize any design parameter. These parameters cannot, however, be chosen independent of one another. An example of trade-offs to be considered is the C_2/C_3 ratio. Increasing this ratio (while other component values remain the same) raises the circuit Q, but it also reduces the midband gain (increases the insertion loss) of the filter. Finding the best compromise is left as a challenging exercise for the motivated designer.

$$H(s) = \frac{\frac{K}{R_2C_2}s}{s^2 + s\left(\frac{1}{R_2C_2} + \frac{1}{R_4C_4} + \frac{1}{R_4C_2} + \frac{1-K}{R_5C_2}\right) + \frac{R_2+R_5}{R_2R_4R_5C_2C_3}}$$

$$\omega_o^2 = \frac{R_2+R_5}{R_2R_4R_5C_2C_3}; \quad Q = \frac{\sqrt{\frac{R_5C_2(R_2+R_5)}{R_2R_4C_3}}}{1 + \frac{R_5}{R_2} + \frac{R_5}{R_4}\left(1 + \frac{C_2}{C_3}\right) - K}$$

$$\text{midband gain } (\text{at } \omega_o) = \frac{\frac{K}{R_2C_2}}{\frac{1}{R_2C_2} + \frac{1}{R_4C_3} + \frac{1}{R_4C_2} + \frac{1-K}{R_5C_2}}$$

where K is the gain of the CLC114/CLC115.
For the equal-R, equal-C case:

$$\omega_o^2 = \frac{2}{RC},\ Q = \frac{\sqrt{2}}{4-K},\ \text{midband gain } (\text{at } \omega_o) = \frac{K}{4-K}$$

References

1) A.I. Zverev, "Handbook of Filter Synthesis", John Wiley and Sons, New York, 1967.
2) A.B. Williams, and F.J. Taylor, "Electronic Filter Design Handbook, Second Edition", McGraw-Hill, New York, 1981.
3) R. Schaumann, M.S. Ghausi, and K.R. Laker, "Design of Analog Filters", Prentice Hall, Englewood Cliffs, 1990.
4) A. Budak, "Passive and Active Network Analysis and Synthesis", Houghton Mifflin Company, Boston, 1974.

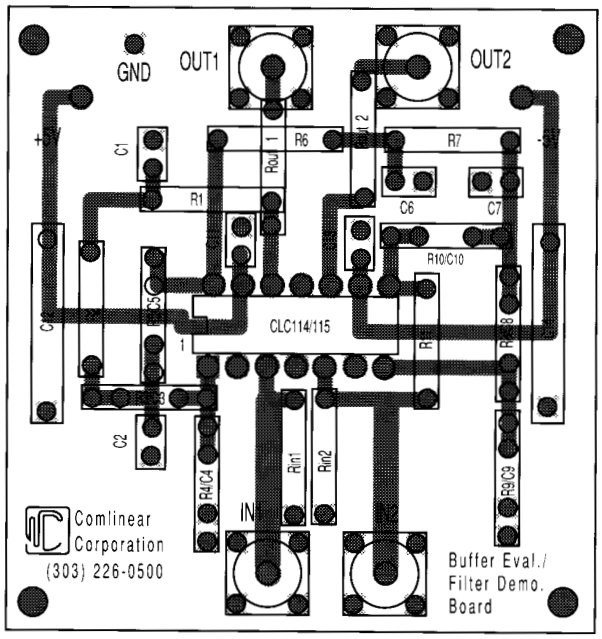


Figure 2
Board Layout and Component Placement

Figure 3
Board Schematic

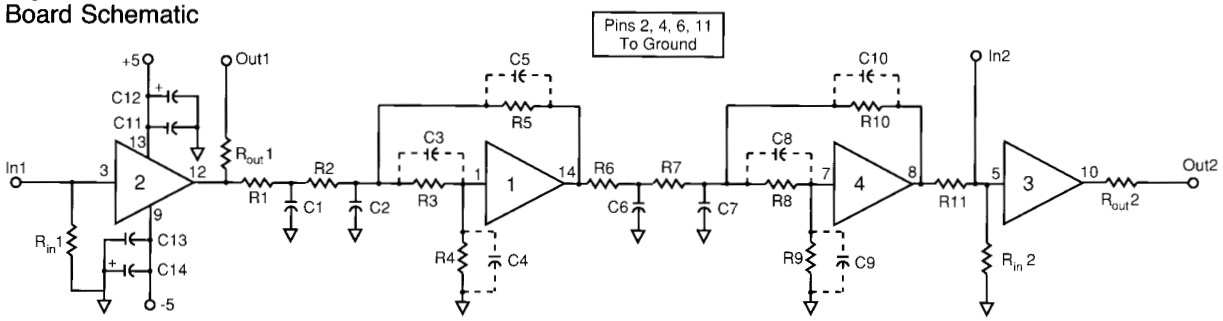


Figure 4
Bandpass Filter Schematic

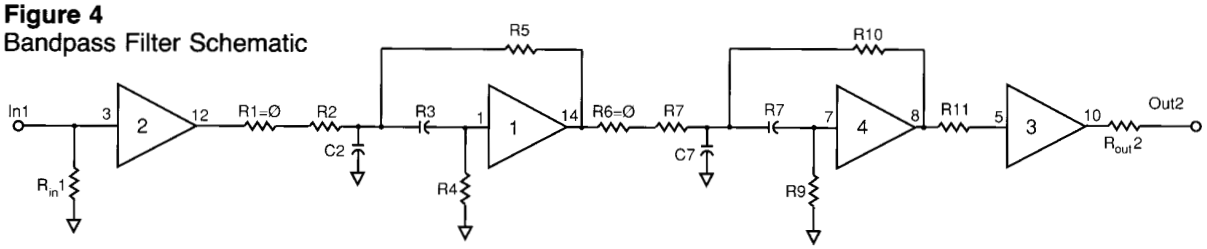
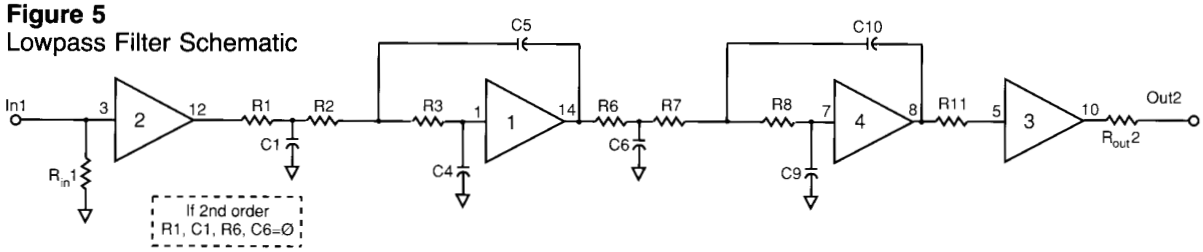


Figure 5
Lowpass Filter Schematic



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