National Semiconductor

February 1998

CLC018 Evaluation Board

Overview

National's Comlinear CLC018PCASM evaluation board is designed for evaluation of the National Serial Digital Video products: CLC006 cable driver, CLC014 Equalizer, CLC016 clock recovery and CLC018 crosspoint switch. The board is configured with 8 differential inputs. Input channel 7 is configured as a 75Ω input connected to a CLC014 equalizer. All other inputs are terminated in 50Ω and fed directly into the CLC018. BNC connectors are installed on DI0, DI6 and DI7. Outputs DO0–DO5 are differential 50Ω source terminated outputs. The nominal signal swing is 250 mV_{pp}. Output D6 is buffered by a CLC006 cable driver and has 75Ω outputs which provide an A.C. coupled 800 mV swing to a 75Ω load connected to the output. Output DO7 is connected via a CLC016 retimer and a CLC006. The retimer chip is configured to automatically select between 143, 177, 270 and 360 Mbps rates.

Inputs

The inputs to the CLC018 are differential with a 50Ω termination to ground. They can be driven by any differential input with at least 200 mV swing and a common mode voltage of 0 to −2V. Note that this includes standard ECL levels. To drive an input single-ended, bias the unused input to a voltage between the logic levels that are being used. This is done by adding a resistor to V_{EE} on the input. A place to put this resistor is on the board and is left open in the standard configuration. For standard ECL, a −1.2V bias on the unused input will allow good operation. To provide the input to DI0, install a 160Ω resistor at R13 and leave the complementary input open.

Equalizer

DI7 is connected to the CLC018 via a CLC014 cable equalizer. This allows signals sent through 300m of Belden 8281 coax cable to be received. The inputs are terminated in 75Ω and are AC coupled. Please refer to the CLC014 datasheet for further details about the cable equalizer and its function.

Outputs

DO0 through DO5 are 50Ω differential outputs with a 250 mV_{pp} swing. If only one side of the output is used, the other should be terminated properly to assure optimal performance. The output swing can be increased by removing the source termination resistors (R6, R17, R20, etc.) which serve to back terminate the transmission lines. Removing these resistors (and replacing them with shorts), will cause jitter to increase slightly at data rates above 500 Mbps.

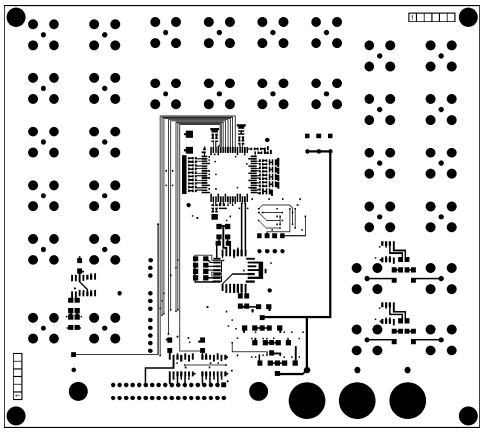
D6 is buffered with a CLC006 cable driver which will provide an 800 mV swing to a 75Ω load. The outputs are AC coupled. Please refer to the CLC006 datasheet for further information .

D7 is reclocked through a Comlinear CLC016 data retimer circuit configured to auto- rate-select between the four standard SDV data rates. Please refer to the CLC016 data sheet for further information on the data retimer.

Control

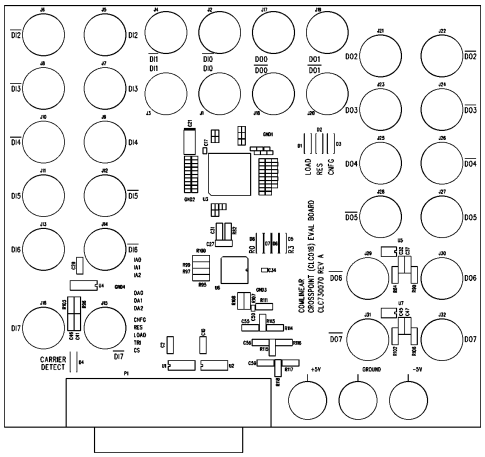
The board is controlled through a Centronics compatible port (standard PC printer port). The program XPOINTP is used to configure the crosspoint switch. XPOINTP should be run from an MSDOS prompt. It may not operate properly if run from an MSDOS window under Windows. Press F1 for instructions on operating the program.

Control (Continued)



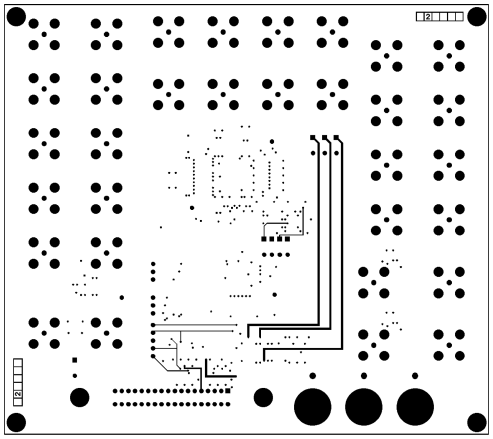
MS100090-1

730070 Layer 1



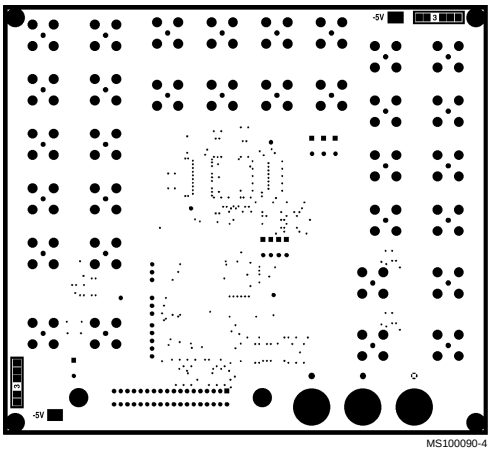
MS100090-2

730070 Layer 1 (silk)



MS100090-3

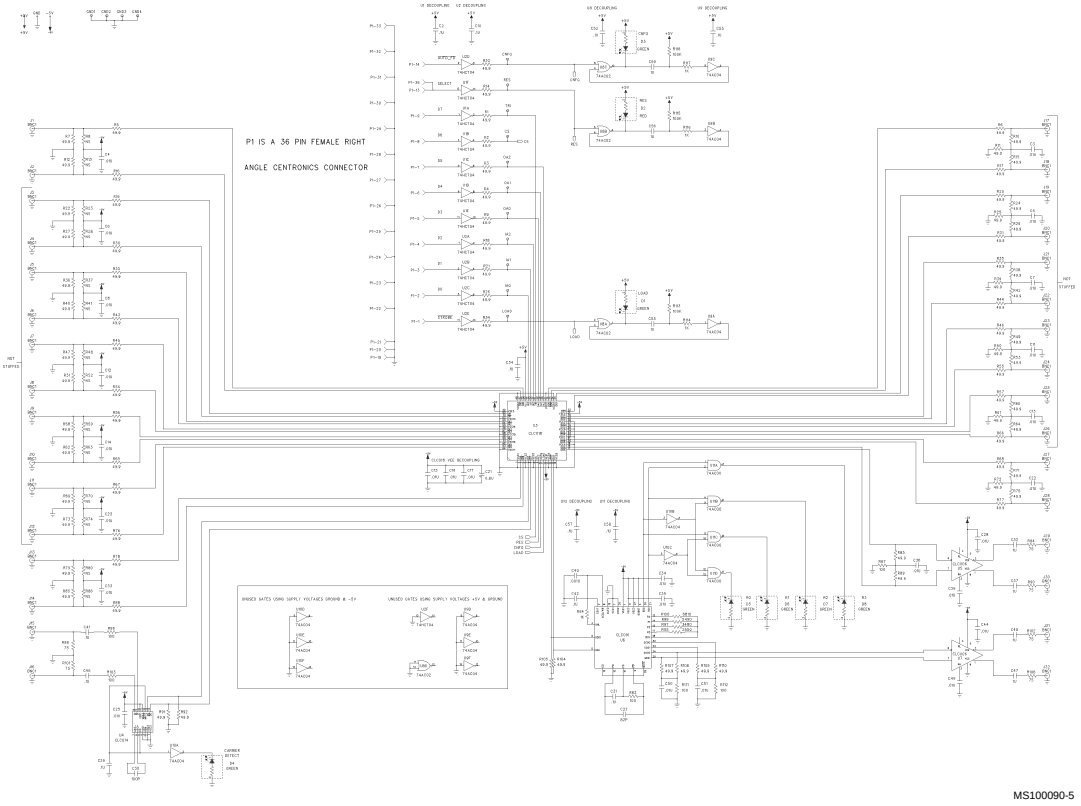
730070 Layer 2



MS100090-4

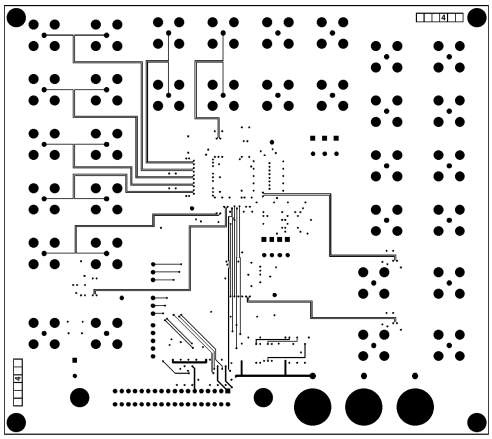
730070 Layer 3

Control (Continued)



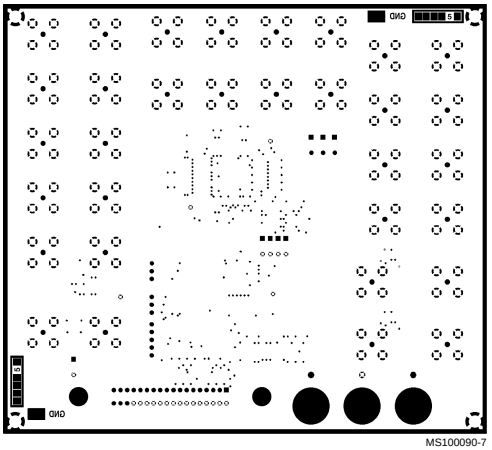
MS100090-5

CLC018 Evaluation II (P/N 730070 Rev. A)



MS100090-6

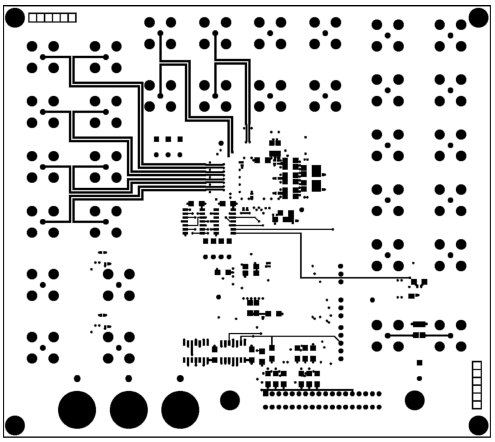
730070 Layer 4



MS100090-7

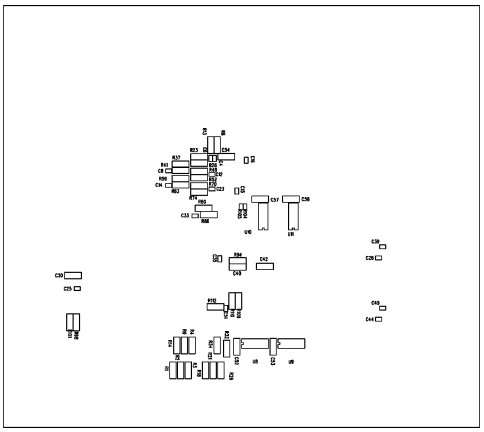
730070 Layer 5

Control (Continued)



MS100090-8

730070 Layer 6



MS100090-9

730070 Layer 6 (silk)

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