National Semiconductor

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CLC011 Evaluation Board

Overview

National's Comlinear CLC011PCASM evaluation board is designed for evaluation of the National Serial Digital products: CLC014 equalizer, CLC016 clock recovery and CLC011 decoder. The board has a differential input which feeds the CLC014 equalizer. After equalization, the signal goes to the CLC016 data retimer. Between the CLC014 and CLC016 are a pair of BNC connectors that can be used to monitor this intermediate signal or, after appropriately configuring the board, can be used to inject an SDV signal into the board. The outputs of the CLC016 are differential clock and data signals which feed the CLC011 data decoder. Once again, there are BNC connectors that can be used either to monitor these signals or to inject signals into the board. The output of the CLC011 is 10-bit parallel data and a clock. The logic levels are CMOS, and these are converted by 10ELT22 translators from CMOS levels to ECL and PECL. The board can be configured to operate from either a single +5V supply, in which case the outputs are PECL compatible, or a single −5V supply, in which case the outputs are ECL.

Configuring the Board for a −5V Power Supply

As shipped, the CLC011PCASM is configured for a +5V supply. To use a −5V supply, remove the two jumpers located near the power jacks and re-insert them in the spaces labeled −5V. Apply −5V to the red jack and GND to the black jack. In either configuration the BNC connectors shields and the input termination resistors are connected to GND.

Equalizer Operation

The CLC014 adaptive equalizer will compensate for the effects of up to 300m of Belden 8281 or similar cable. The adaptive servo mechanism functions assuming that the input to the cable is a valid SMPTE 259M signal: i.e., 800 mV_{pp} into a 75Ω load. For details on the CLC014 adaptive equalizer, please refer to the CLC014 datasheet. The outputs of the equalizer feed a CLC016 data retimer through jumpers JB3 and JB4. The BNC connectors labeled DDI0 and DDI1 can be used to monitor the equalized data that is input to the CLC016. To bypass the equalizer function, cut the traces connecting JB3 and JB4 and feed a SMPTE standard signal to the DDI0 and DDI1 BNC connectors.

Retimer Operation

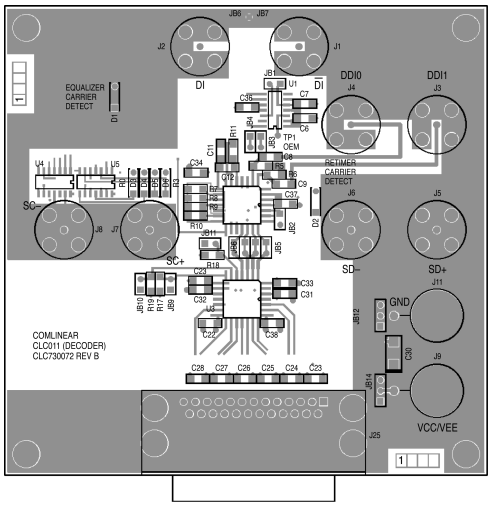
The data retimer on the CLC011 evaluation board is configured for auto-rate-selection between the four standard SMPTE 259M data rates: 143,177,270 and 360 Mbps. The selected rate is indicated by the LED display located between the DI/ and SC+ connectors. The output of the CLC016 retimer are a clock and a retimed data signal, both of which are differential. These can be monitored via the SD+, SD−, SC+ and SC− connectors. To bypass the retimer on the board, cut the traces in the JB5, JB65, JB7 and JB8 locations and provide clock and data through the SC+, SC−, SD+ and SD− connectors.

Decoder Operation

The CLC011 decoder converts the serial clock and data from the CLC016 into parallel data and clock. In the default configuration, no jumpers are installed in JB9, JB10 and JB11. In this configuration FE is enabled. The data is descrambled and is assumed to be NRZI input data. These controls can be pulled low by installing the appropriate jumper. Please refer to the CLC011 datasheet for full details on the operation of the CLC011 and its control signals. The outputs of the CLC011 are CMOS compatible. These signals are converted by 10ELT22's into ECL (if operating from −5V) or PECL (if operating from +5V) and are output on connector J25. The pinout of connector J25 is that specified in SMPTE 125M and shown in the table below. SMPTE 125 specifies that the signals are to be ECL. The output is SMPTE 125M compliant only if the board is configured for a −5V supply.

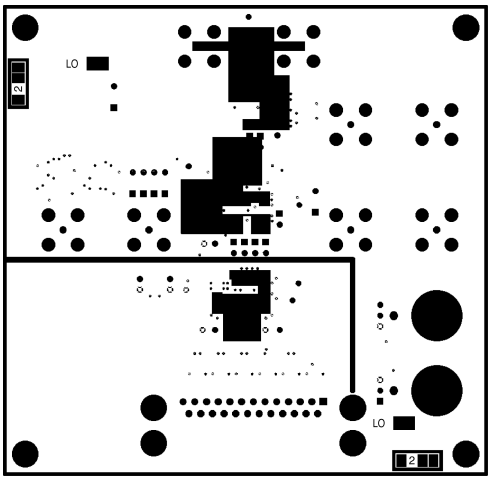
Pin	Signal Line	Pin	Signal Line
1	Clock	14	Clock return
2	System GND A	15	System GND B
3	Data 9	16	Data 9/
4	Data 8	17	Data 8/
5	Data 7	18	Data 7/
6	Data 6	19	Data 6/
7	Data 5	20	Data 5/
8	Data 4	21	Data 4/
9	Data 3	22	Data 3/
10	Data 2	23	Data 2/
11	Data 1	24	Data 1/
12	Data 0	25	Data 0/
13	Cable shield		

Decoder Operation (Continued)



MS100089-1

730072 Layer 1



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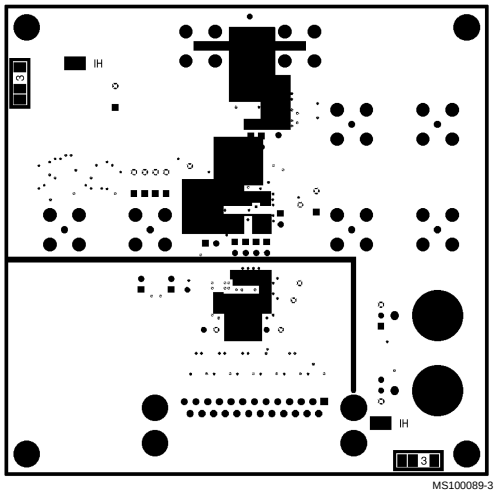
730072 Layer 2



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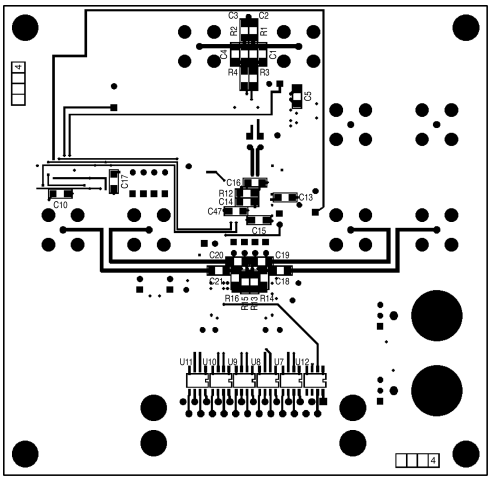
730072 Layer 3



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730072 Layer 4

Decoder Operation (Continued)

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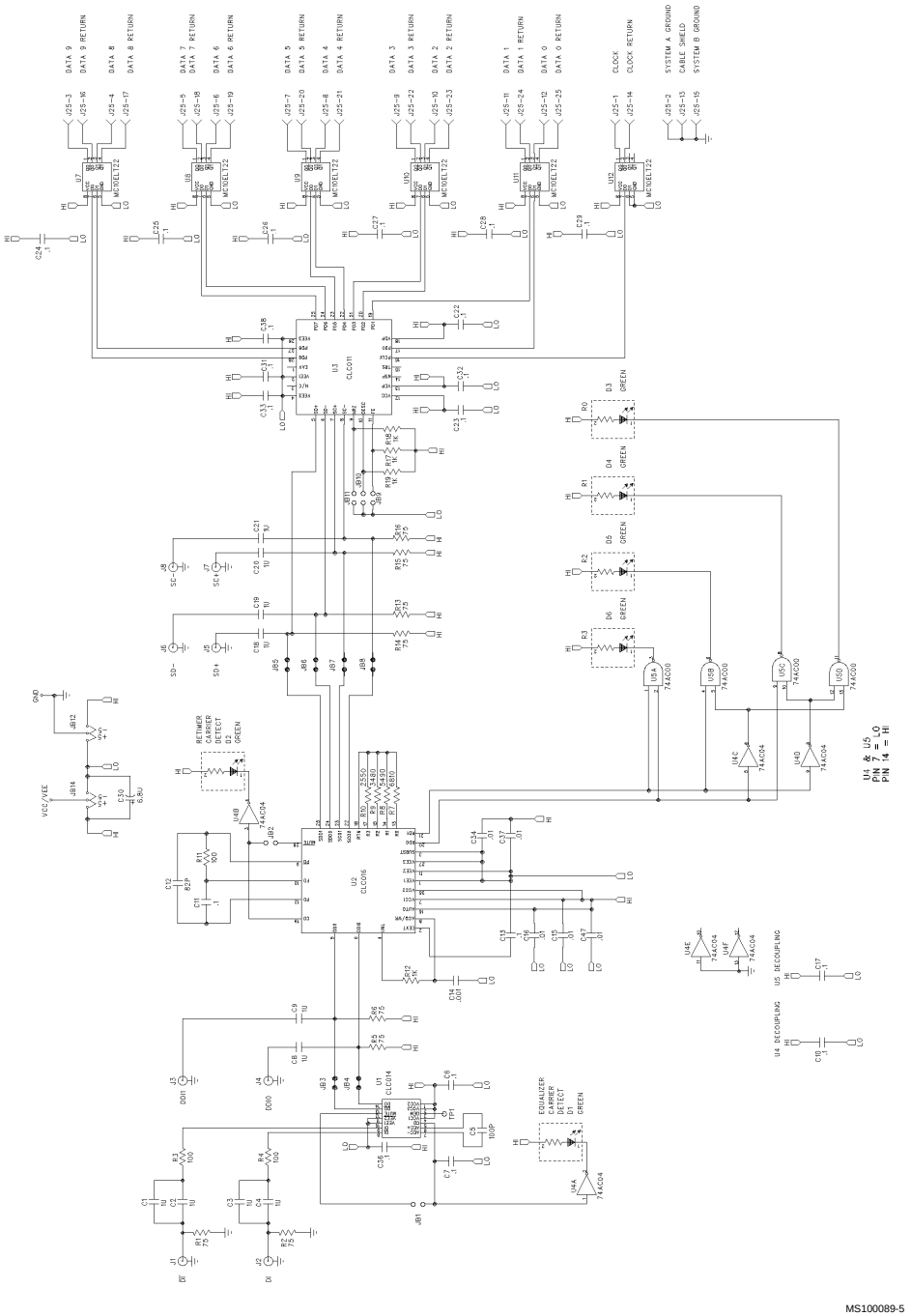

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